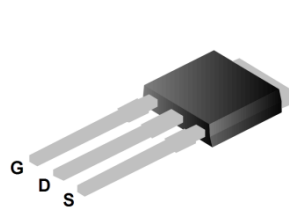
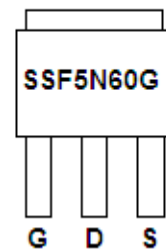
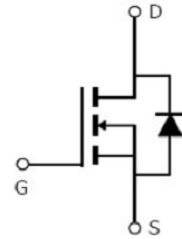


Main Product Characteristics:

V_{DS}	600V
$R_{DS(on)}$	1.88Ω (typ.)
I_D	5A


TO-251

Marking and pin Assignment

Schematic diagram
Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute max Rating:

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V①	5	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V①	3.1	
I_{DM}	Pulsed Drain Current②	20	
P_D @ TC = 25°C	Power Dissipation③	125	W
	Linear Derating Factor	1.00	W/°C
V_{DS}	Drain-Source Voltage	600	V
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy @ L=27.5mH	209	mJ
I_{AS}	Avalanche Current @ L=27.5mH	3.9	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

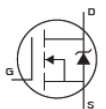
Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ^③	—	1.00	°C/W
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ^④	—	110	°C/W

Electrical Characterizes @ $T_A=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	600	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	1.88	2.15	Ω	$V_{GS}=10V, I_D = 2A$
		—	4.21	—		$T_J = 125^\circ\text{C}$
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		—	1.90	—		$T_J = 125^\circ\text{C}$
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 600V, V_{GS} = 0V$
		—	—	50		$T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 30V$
		—	—	-100		$V_{GS} = -30V$
Q_g	Total gate charge	—	10.26	—	nC	$I_D = 4A,$ $V_{DS}=300V,$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source charge	—	3.64	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	2.94	—		
$t_{d(on)}$	Turn-on delay time	—	10.8	—	ns	$V_{GS}=10V, V_{DS}=300V,$ $R_{GEN}=5\Omega, I_D=4A$
t_r	Rise time	—	6.8	—		
$t_{d(off)}$	Turn-Off delay time	—	15.2	—		
t_f	Fall time	—	6.8	—		
C_{iss}	Input capacitance	—	506.1	—	pF	$V_{GS} = 0V$
C_{oss}	Output capacitance	—	66.65	—		$V_{DS} = 25V$
C_{rss}	Reverse transfer capacitance	—	1.99	—		$f = 1MHz$

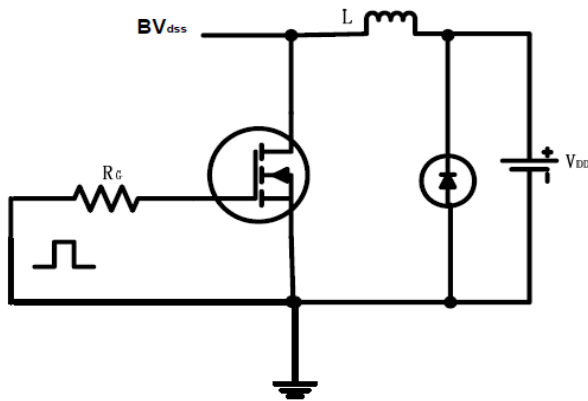
Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)	—	—	20	A	
V_{SD}	Diode Forward Voltage	—	0.87	1.4	V	$I_S=4A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	441	—	ns	$T_J = 25^\circ\text{C}, I_F = 4A,$ $di/dt = 100A/\mu s$
Q_{rr}	Reverse Recovery Charge	—	1964	—	nC	

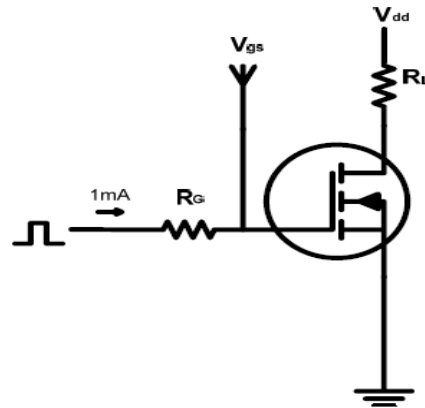


Test circuits and Waveforms

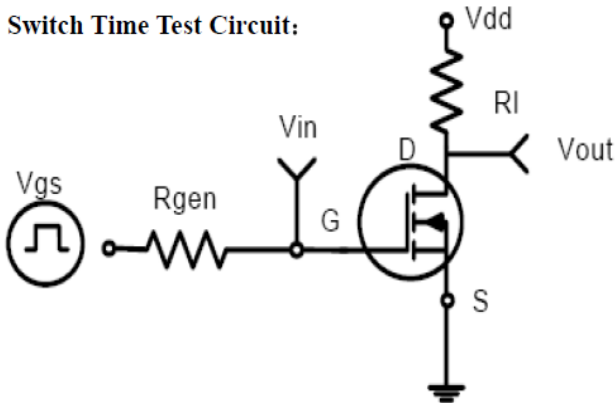
EAS test circuits:



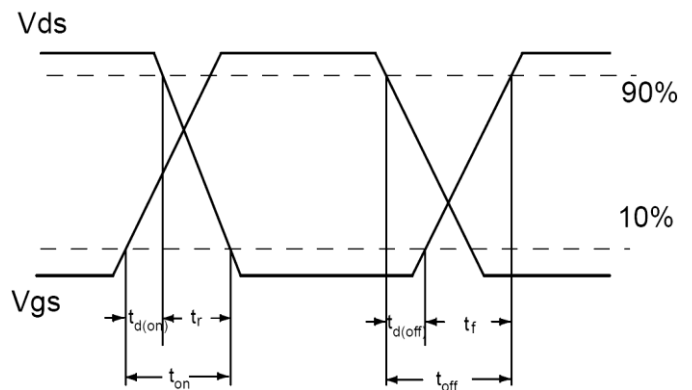
Gate charge test circuit:



Switch Time Test Circuit:



Switch Waveforms:



Notes:

- ①The maximum current rating is limited by bond-wires.
- ②Repetitive rating; pulse width limited by max. junction temperature.
- ③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$
- ⑤These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)} = 150^\circ\text{C}$.

Typical electrical and thermal characteristics

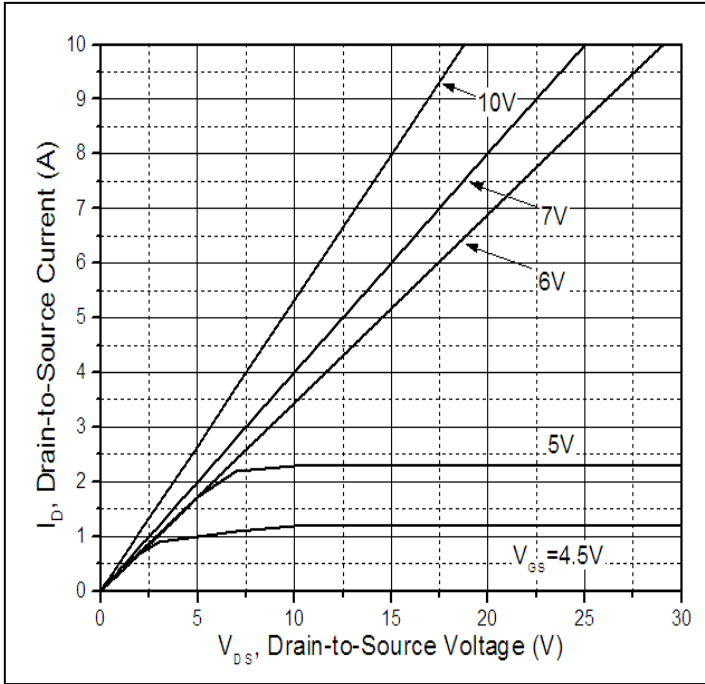


Figure 1: Typical Output Characteristics

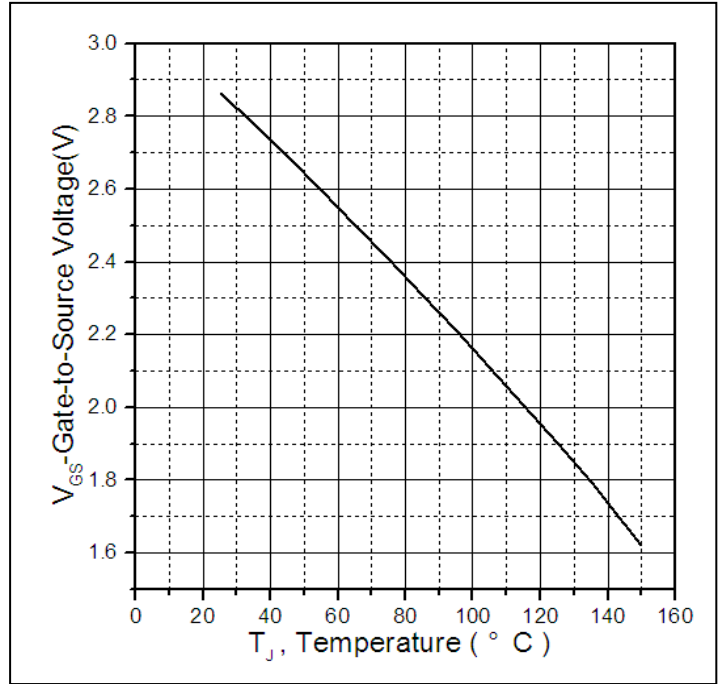


Figure 2. Gate to source cut-off voltage

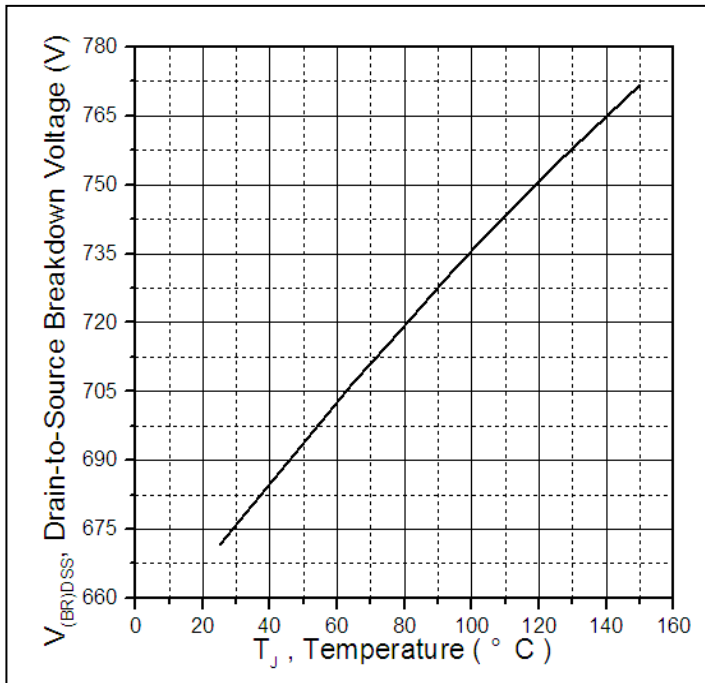


Figure 3. Drain-to-Source Breakdown Voltage vs. Case Temperature

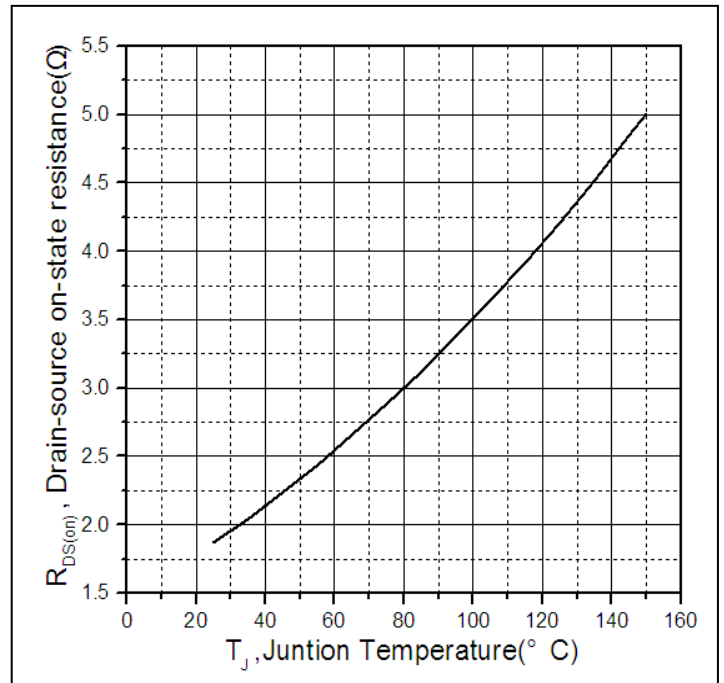


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

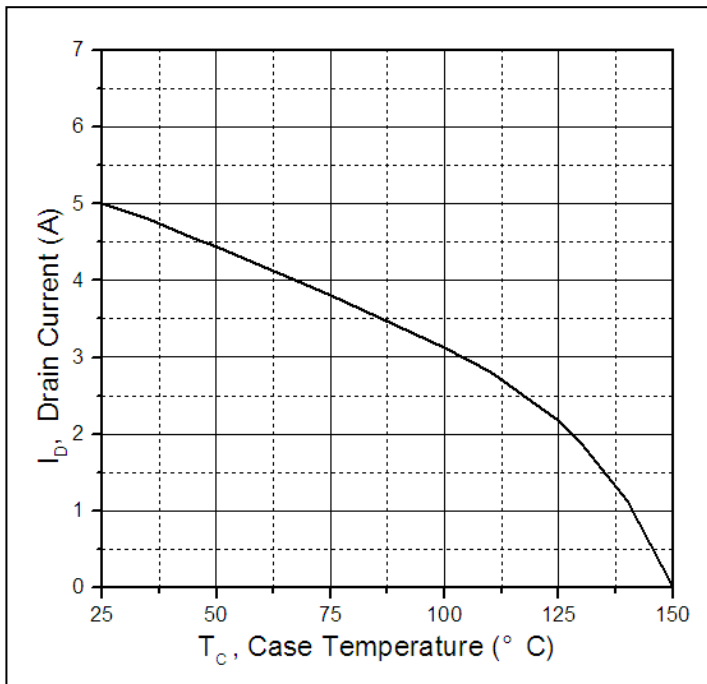


Figure 5. Maximum Drain Current Vs. Case Temperature

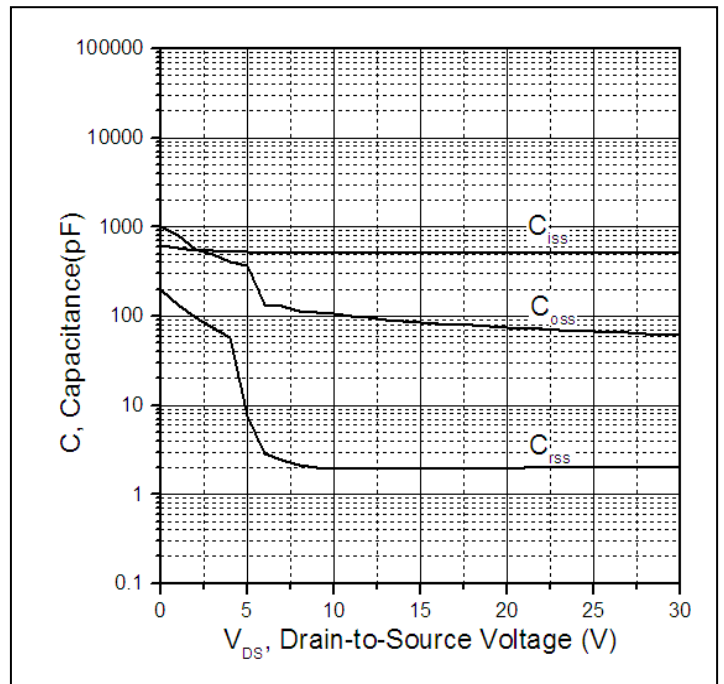


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

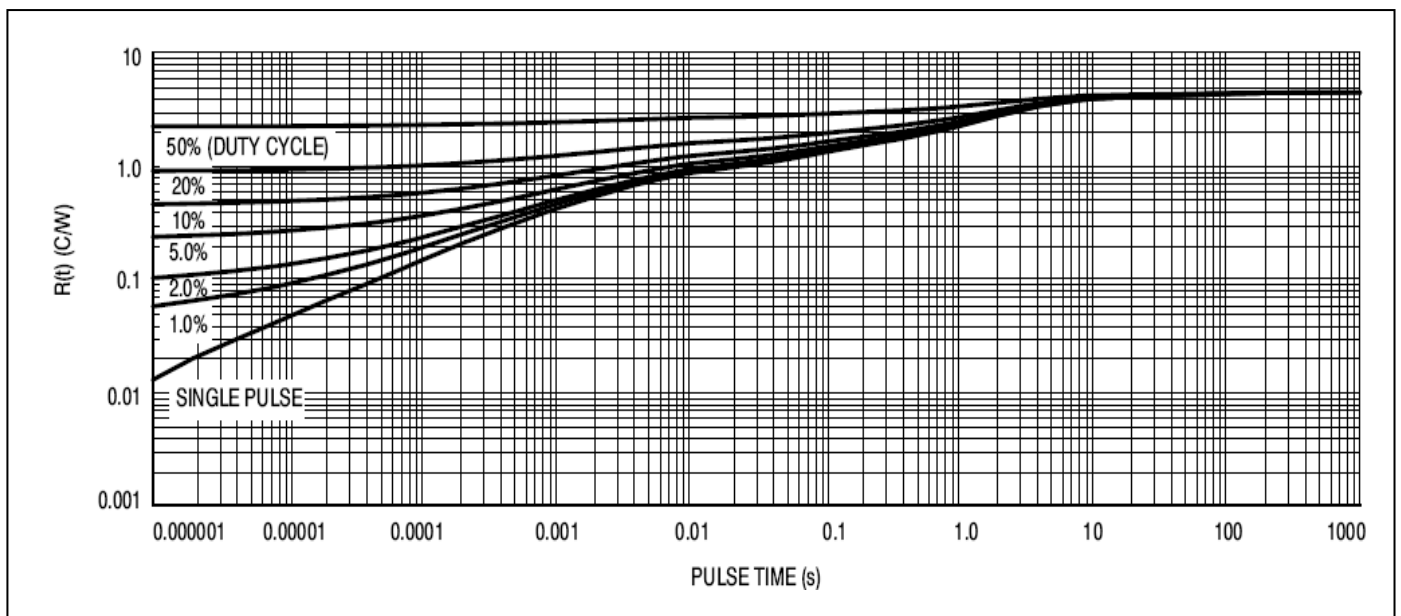
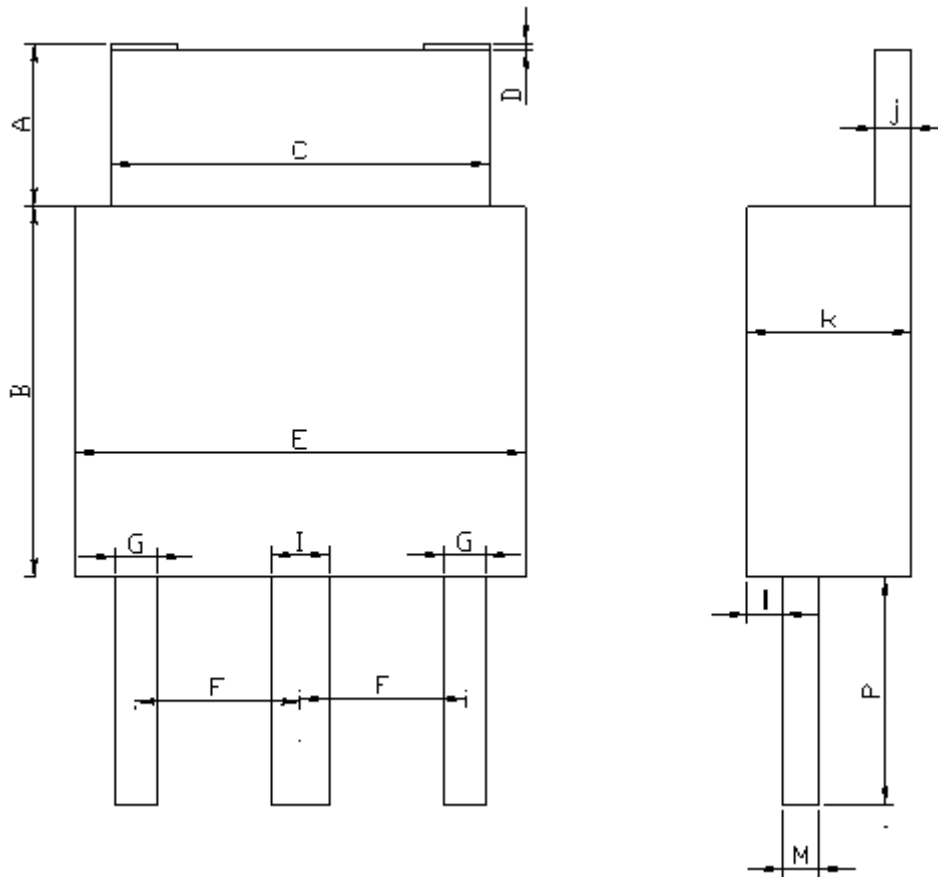


Figure7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data:
TO-251 PACKAGE OUTLINE DIMENSION


Unit: mm

A: 0.9 ± 0.5	B: 5.85 ± 0.5	C: 5.3 ± 0.5	D: 0.1 ± 0.02
E: 6.3 ± 0.5	F: 2.3 ± 0.1	G: 0.7 ± 0.1	I: 0.8 ± 0.1
J: 0.508 ± 0.1	K: 2.3 ± 0.25	L: 0.8 ± 0.25	M: 0.508 ± 0.1
P: 8.5 ± 0.5			

Ordering and Marking Information**Device Marking: SSF5N60G**

Package (Available)
TO-251 (IPAK)
Operating Temperature Range
C : -55 to 150 °C

Devices per Unit

Package Type	Units/ Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-251	80	60	4800	5	24000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 150°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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Customer Service**Worldwide Sales and Service:**

Sales@silikron.com

Technical Support:

Technical@silikron.com

Suzhou Silikron Semiconductor Corp.

11A, 428 Xinglong Street, Suzhou Industrial Park, P.R.China

TEL: (86-512) 62560688

FAX: (86-512) 65160705

E-mail: Sales@silikron.com