ASIX AX88860

10/100BASE-TX/FX Repeater Controller Data Sheet(11/03/'97)

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FIGURES

1.0 AX88860 Overview

The AX88860 10/100Mbps Repeater Controller is design for low cost dumb HUB application. The AX88860 directly supports up-to night 10/100Mbps links with its shared 8 ports MII interfaces and 1 dedicated MII interface. Maximum up-to 72 ports can be constructed when using expansion bus cascades 8 AX88860s. The AX88860 is designed base on IEEE 802.3u clause 27 " Repeater for 100Mb/s base-band networks" . It is fully compatible with IEEE 802.3u standard†.

1.1 General Description

The AX88860 Repeater Controller is a subset of a repeater set containing all the repeater-specific components and functions, exclusive of PHY components and functions. The AX88860 has only Media Independent Interface (MII) to connect to PHY devices. Other then AX88850 serial chips that has 2 kinds of interfaces. There are Physical coding sub-layer (PCS) interface and Media Independent Interface (MII).

The AX88860 supports one shared bus (8 ports) MII interfaces, 1 dedicated MII ports interface, a port expansion interface and LED display interface.

The AX88860 dedicated MII ports can connect to PHY or optional directly connect to 2 ports bridge, switch or MAC that has standard MII interface.

The AX88860 has two application modes.

Mode 0	Single chip repeater application.
Mode 1	Multiple chips cascaded repeater application.

† Note : To simplify the design of 10BASE Ethernet repeater. The portion of 10Mb/p repeater will follow the specification as below :

(1) The PHY interface defines as standard MII interface with 2.5MHz transmit and receive clock and 4 bits data format.

(2) The repeater core state machine follow IEEE 802.3u clause 27 "Repeater for 100 Mb/s baseband networks" with ten times of time scale. It is important that it is no longer follows the legacy 10BASE repeater state machine.

1.2 Features

- IEEE 802.3u repeater compatible
- Supports 10/100 Mbps alternative
- Supports 8+1 network connections
- 8 ports share MII interfaces direct interface to PHY chip with MII interface
- 1 dedicated MII interfaces can also support 100BASE-T4/FX PHY interfaces
- The 1 dedicated MII interfaces can also easily connect to bridging device with MII interface
- Up-to 8 repeater chips can be cascaded for large HUB application
- Low latency design supports Class II repeater implementation with large port number
- All ports can be separately isolated or partitioned in response to fault condition
- Separate jabber and partition state machines for each port
- Encoded or direct LED drivers
- Per-port LED display for Jabber, Partition, Activity. Global collision, utilization and collision (%) presentation
- Power on LED diagnosis. All the LED display will follow the “ON-OFF-ON-OFF-Normal” operation procedure during/after power on reset (mode 1 only).
- 100-pin PQFP

1.3 Block Diagram

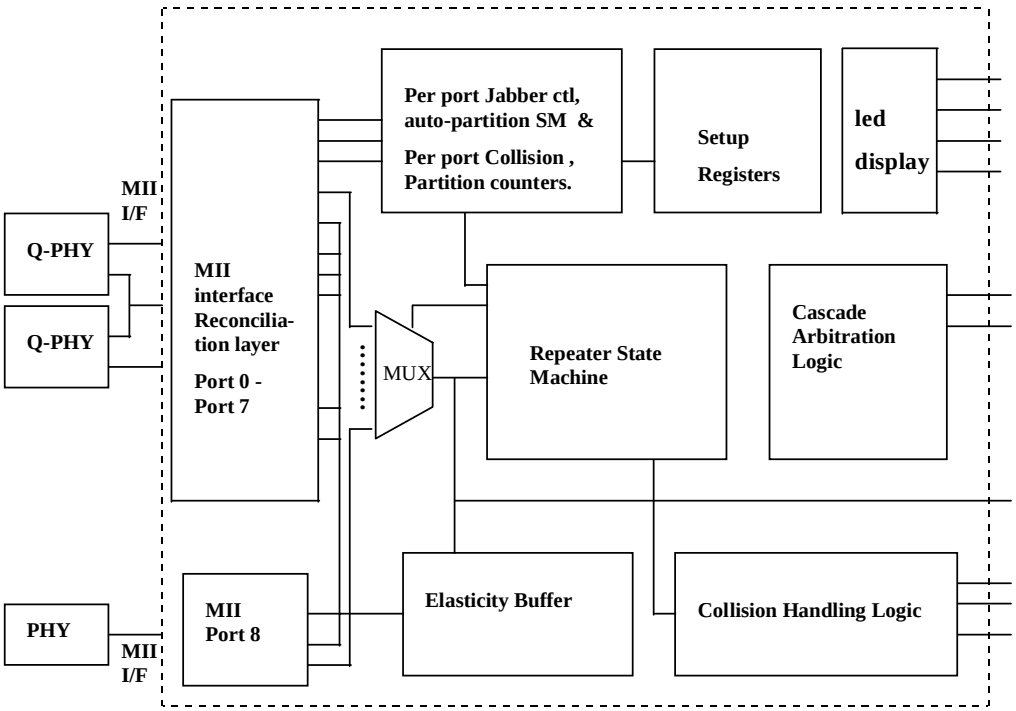


Fig - 1 Chip Block Diagram

1.4 Pin Connection Diagram (mode 0)

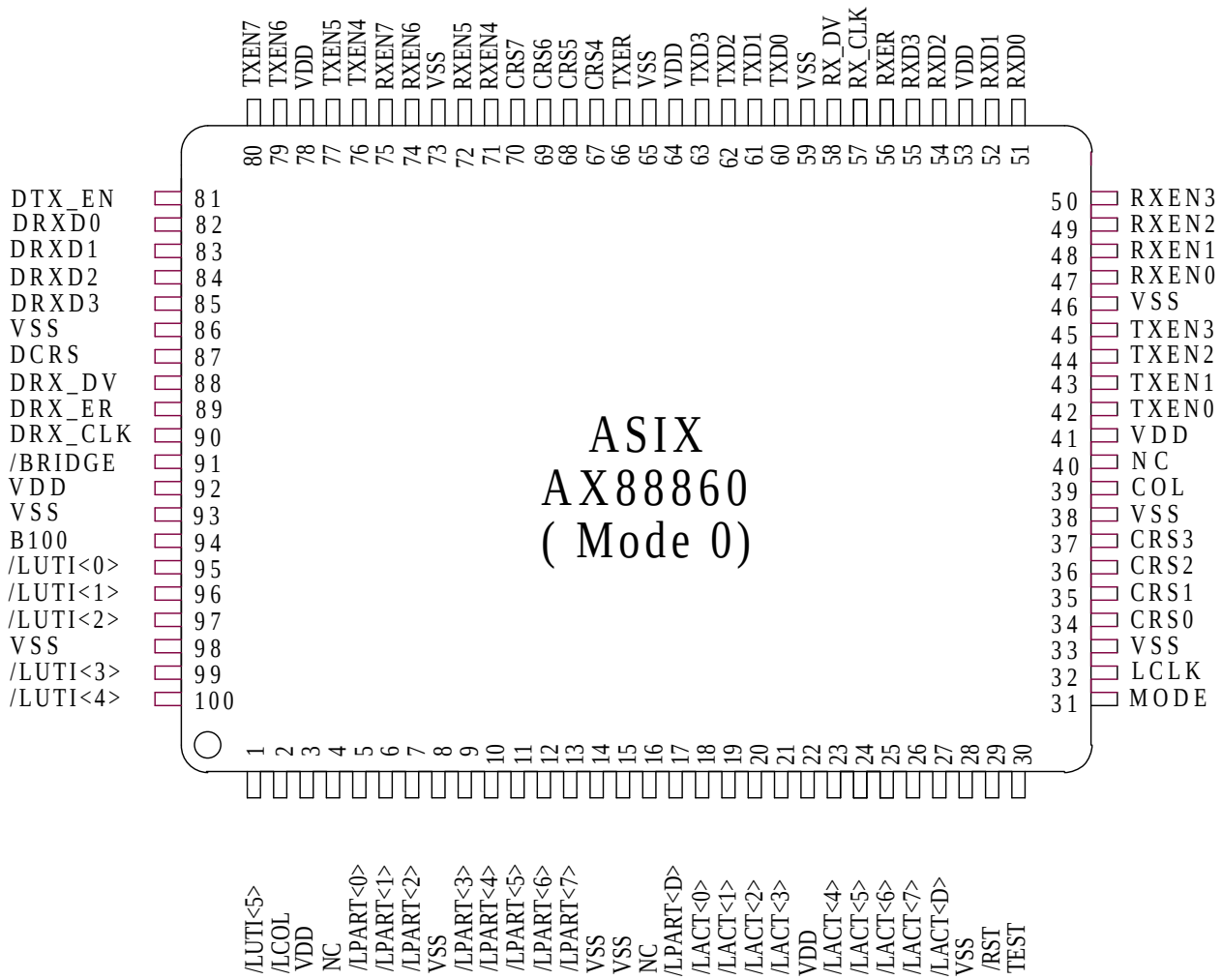


Fig - 2 Pin Connection Diagram for mode 0

1.5 Pin Connection Diagram (mode 1)

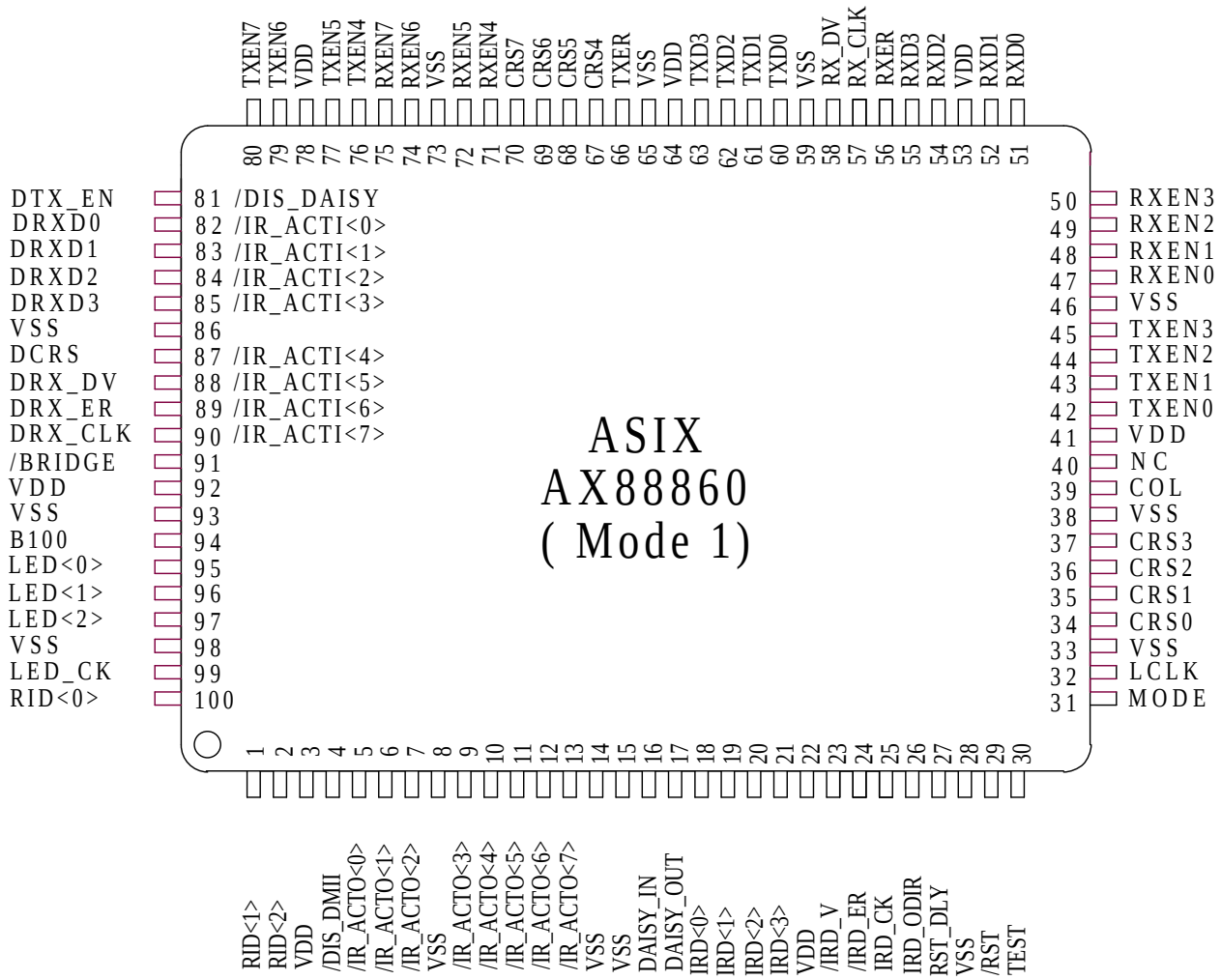


Fig - 3 Pin Connection Diagram for mode 1

2.0 Pin Description

2.1 Shared MII interface

Signal Name	Type	Pin No.	Description
TX_ER	O/MH	66	Transmit Error : TX_ER is transition synchronously with respect to the rising edge of TX_CLK . Asserted high when a code violation is request to be send
TXD[3:0]	O/MH	63-60	Transmit Data : TXD[3:0] is transition synchronously with respect to the rising edge of TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD[3:0] are accepted for transmission by the PHY.
TX_EN[7:0]	O/L	80-79 77-76 45-42	Transmit Enable : TX_EN is transition synchronously with respect to the rising edge of TX_CLK. TX_EN indicates that the port is presenting nibbles on TXD [3:0] for transmission.
RXD[3:0]	I/PU	55-54 52-51	Receive Data : RXD [3:0] is driven by the PHY synchronously with respect to RX_CLK.
RX_ER	I/PD	56	Receive Error : RX_ER ,is driven by PHY and synchronous to RX_CLK, is asserted for one or more RX_CLK periods to indicate to the port that an error has detected.
RX_CLK	I	57	Receive Clock : RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV,RXD [3:0] and RX_ER signals from the PHY to the MII port of the repeater.
RX_DV	I/PD	58	Receive Data Valid : RX_DV is driven by the PHY synchronously with respect to RX_CLK. Asserted high when valid data is present on RXD [3:0].
CRS[7:0]	I/PD	70-67, 37-34	Carrier Sense : Asynchronous signal CRS is asserted by the PHY when either the transmit or receive medium is non-idle.
RX_EN[7:0]	O/L	75-74 72-71, 50-47	Receive Enable : Assert high to the respective PHY chip to enable its receive data.

Note : "Type" has the following attributes

I : Input
O : Output
I/O : Bi-direction
PU : Pull Up
PD : Pull Down
H : Driving High Current 16mA
MH : Driving Middle High Current 12mA
ML : Driving Middle Low Current 8mA
L : Driving Low Current 4mA

2.2 Dedicated MII interface

Signal Name	Type	Pin No.	Description
DRXD[3:0] or /IR_ACTI[3:0]	I/PU	85-82	Receive Data : DRXD [3:0] is driven by the PHY synchronously with respect to DRX_CLK. INTER REPEATER ACTIVITY IN: These pins perform the same function as /IR_ACTO[3:0] when they serve as input function. Then the /IR_ACTO[7:0] insert external buffers the input function must be replaced with /IR_ACTI [3:0].
DCRS or /IR_ACTI[4]	I/PD	87	Carrier Sense : Asynchronous signal DCRS is asserted by the PHY when either the transmit or receive medium is non-idle. /IR_ACTI[4] : See above /IR_ACTI[3:0] descriptions.
DRX_DV or /IR_ACTI[5]	I/PD	88	Receive Data Valid : DRX_DV is driven by the PHY synchronously with respect to DRX_CLK. Asserted high when valid data is present on DRXD [3:0]. /IR_ACTI[5] : See above /IR_ACTI[3:0] descriptions.
DRX_ER or /IR_ACTI[6]	I/PD	89	Receive Error : DRX_ER ,is driven by PHY and synchronous to DRX_CLK, is asserted for one or more RX_CLK periods to indicate to the port that an error has detected. /IR_ACTI[6] : See above /IR_ACTI[3:0] descriptions.
DRX_CLK or /IR_ACTI[7]	I	90	Receive Clock : DRX_CLK is a continuous clock that provides the timing reference for the transfer of the DRX_DV,DRXD [3:0] and DRX_ER signals from the PHY to the MII port of the repeater. /IR_ACTI[7] : See above /IR_ACTI[3:0] descriptions.
DTX_EN /DIS_DAISY	I/O /PU/L	81	Transmit Enable : DTX_EN is transition synchronously with respect to the rising edge of TX_CLK(LCLK). DTX_EN indicates that the port is presenting nibbles on TXD [3:0] for transmission. /DIS_DAISY : Default pull-up to enable daisy chain function. To disable daisy chain function pull the pin down external.
/DIS_DMII or NC	I/PU	4	Disable Dedicated MII port: When MODE="1" , The dedicated MII port will be disable (perform /IR_ACTI function) when low and will be enable when high while the TEST pin is low. When TEST pin go high will latch the /DIS_DMII signal and this pin perform test mode selection function. NC : When MODE="0" , This pin keep no connection or pull-up.

2.3 Expansion Bus Interface

Signal Name	Type	Pin No.	Description
IRD[3:0] or /LACT[3:0]	I/O/Z /MH /PU	21-18	INTER REPEATER DATA : When MODE="1" , Nibble data input/output. Transfer data from the "active" AX88860 to all other "inactive" AX88860s. The bus-master of the IRD bus is determined by IR_VECT bus arbitration. /LACT[3:0] : When MODE="0" , Those pins drive activity[3:0] LEDs directly.
/IRD_V or /LACT[4]	I/O/Z /MH /PU	23	INTER REPEATER DATA VALID : When MODE="1" ,This signal reflect the RX_DV status of the active port across the inter repeater bus. Used to frame good packets. /LACT[4] : When MODE="0" , This pin drives port 4 activity LED directly.
/IRD_ER or /LACT[5]	I/O/Z /MH /PU	24	INTER REPEATER DATA ERROR: When MODE="1" ,This signal reflect the RX_ER status of the active port across the inter repeater bus. Used to track receive errors from the PHY in real time. /LACT[5] : When MODE="0" , This pin drives port 5 activity LED directly.
IRD_CK or /LACT[6]	I/O/Z /MH /PU	25	INTER REPEATER CLOCK VALID : When MODE="1" ,All inter repeater signals are synchronized to the rising edge of this clock. /LACT[6] : When MODE="0" , This pin drives port 6 activity LED directly.
IRD_ODIR or /LACT[7]	O/ML	26	INTER REPEATER DATA IN/OUT DIRECTION : When MODE="1" ,This pin indicates the direction of data for external transceiver. "High" = IRD[3:0], /IRD_ER, /IRD_V , IRD_CK are Output. "Low" = IRD[3:0], /IRD_ER, /IRD_V , IRD_CK are Input. /LACT[7] : When MODE="0" , This pin drives port 7 activity LED directly.
/IR_ACTO[7:0] or /LPART[7:0]	I/O/OC /H	13-9 7-5	INTER REPEATER ACTIVITY IN/OUT: When MODE="1" ,When the local repeater activity appearance, the signal of the related RID (Repeater ID) will be asserted and as a output pin. All other pins serve as input pins but except the collision conditions. When collision occurred all of the signal of related (RID-1) pins will served as outputs and will active during local collision period. The exception case is when RID = 0, then (RID-1) is replaced with (RID+1)=1. /LPART[7:0] : When MODE="0" , Those pins drive partition[7:0] LEDs directly.

2.4 LED Display

<table>
<tr><th>Signal Name</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>LED[2:0]
or

/LUTI[2:0]</td><td>O/ML</td><td>97-95</td><td>LED Display Information : When MODE=”1” , Those signals indicate each port‘s Partition, Jabber, Activity, Collision (global), Repeater ID, Utilization % (global), Collision % (global) in sequence. For detail , see the LED timing specification
/LUTI[2:0] : When MODE=”0” , Those pins drive utilization[2:0] LEDs directly.

The Utilization % display define as following :

<table>
<tr><th>Utilization %</th><th>LED0</th><th>LED1</th><th>LED2</th><th>LED3</th><th>LED4</th><th>LED5</th><th>LED6</th><th>LED7</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>5</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>15</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>30</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>40</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>60</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>80+</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
The Collision % display define as following :

<table>
<tr><th>Collision %</th><th>LED0</th><th>LED1</th><th>LED2</th><th>LED3</th><th>LED4</th><th>LED5</th><th>LED6</th><th>LED7</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>5</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>10</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>15</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>20</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>30</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>60+</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>LED_CK
or

/LUTI[3]</td><td>O/ML</td><td>99</td><td>LED clock signal : When MODE=”1” , The signal is a discontinue clock for LED signals serial shift out. The clock period width is 40nS and last 16 cycle with every 125ms repeated.
/LUTI[3] : When MODE=”0” , This pin drive utilization[3] LED directly.</td></tr>
</table>

NOTE : The Utilization % display define as following for Mode 0 LED direct driving.

Utilization %	/LUTI0	/LUTI1	/LUTI2	/LUTI3	/LUTI4	/LUTI5
0	1	1	1	1	1	1
1	0	1	1	1	1	1
5	0	0	1	1	1	1
10	0	0	0	1	1	1
15	0	0	0	0	1	1
30	0	0	0	0	0	1
60	0	0	0	0	0	0

2.5 Miscellaneous

Signal Name	Type	Pin No.	Description
LCLK	I	32	Local Clock : Must be run at 25Mhz . Used for transmit data to PHY devices,
/RST	I	29	Reset : The chip is reset when this signal is asserted Low.
RST_DLY or /LACT[D]	O/ML	27	Reset Delay : When MODE="1" , The signal is active high when reset and delay /RST signal about 2 LCLK cycle. It is useful for power on configuration setup control of /IR_ACTI[7:0]. /LACT[D] : When MODE="0" , This pin drives dedicated MII port activity LED directly.
DAISY_IN or NC	I/PU	16	Repeater Identification Number Daisy-Chain In : When MODE="1" , This pin is a daisy chain serial input for Repeater ID. A state machine always monitor the input if a correct data (RID) present at the pin, the (RID+1) will be written to RID register and override the power on setup RID for the chip. NC : When MODE="0" , This pin keep no connection or pull-up.
DAISY_OUT or /LPART[D]	O/ML	17	Repeater Identification Number Daisy-Chain Out : When MODE="1" , This pin is periodically shift out the RID of itself to the next chained chip to inform that this ID has already been occupied. The RID is shift out periodically every about 200us. /LPART[D] : When MODE="0" , This pin drives dedicated MII port partition LED directly.
TEST	I/PD	30	Test Pin : The pin is just for test mode setting purpose only. Must be pull low when normal operation. When in test mode , GEP pins will be force to test input signals.
RID[2:0] or /LCOL, /LUTI[5:4]	I/O /ML /PU	2-1 100	Repeater ID: When MODE="1" , Repeater ID real time input when TEST pin is low. When TEST pin go high will latch the RID signals and those pins perform test mode selection function. /LCOL , /LUTI[5:4] : When MODE="0" , Those pins drive collision and utilization[5:4] LEDs directly.
B100	I/PU	94	B100: When logic high 100BASE-T is selected (default), otherwise 10BASE-T is selected.
MODE	I/PU	31	MODE: Repeater chip application mode. MODE="0" is for single chip repeater application. MODE="1" is for multiple chips cascaded repeater application.
/BRIDGE	I/PU	91	/BRIDGE : Option for external device type to connect to dedicated MII port. Default 'high' is for PHY type device. Otherwise, 'low' for bridge, switch or MAC type device.
NC		40	NC : Those pins must keep no connection.
VDD	I	3,22,41 53,64 78,92	POWER : +5V +/-5%
VSS	I	8,14,15 28,33,38 46,59,65 73,86,93 98	POWER: 0V

3.0 Functional Description

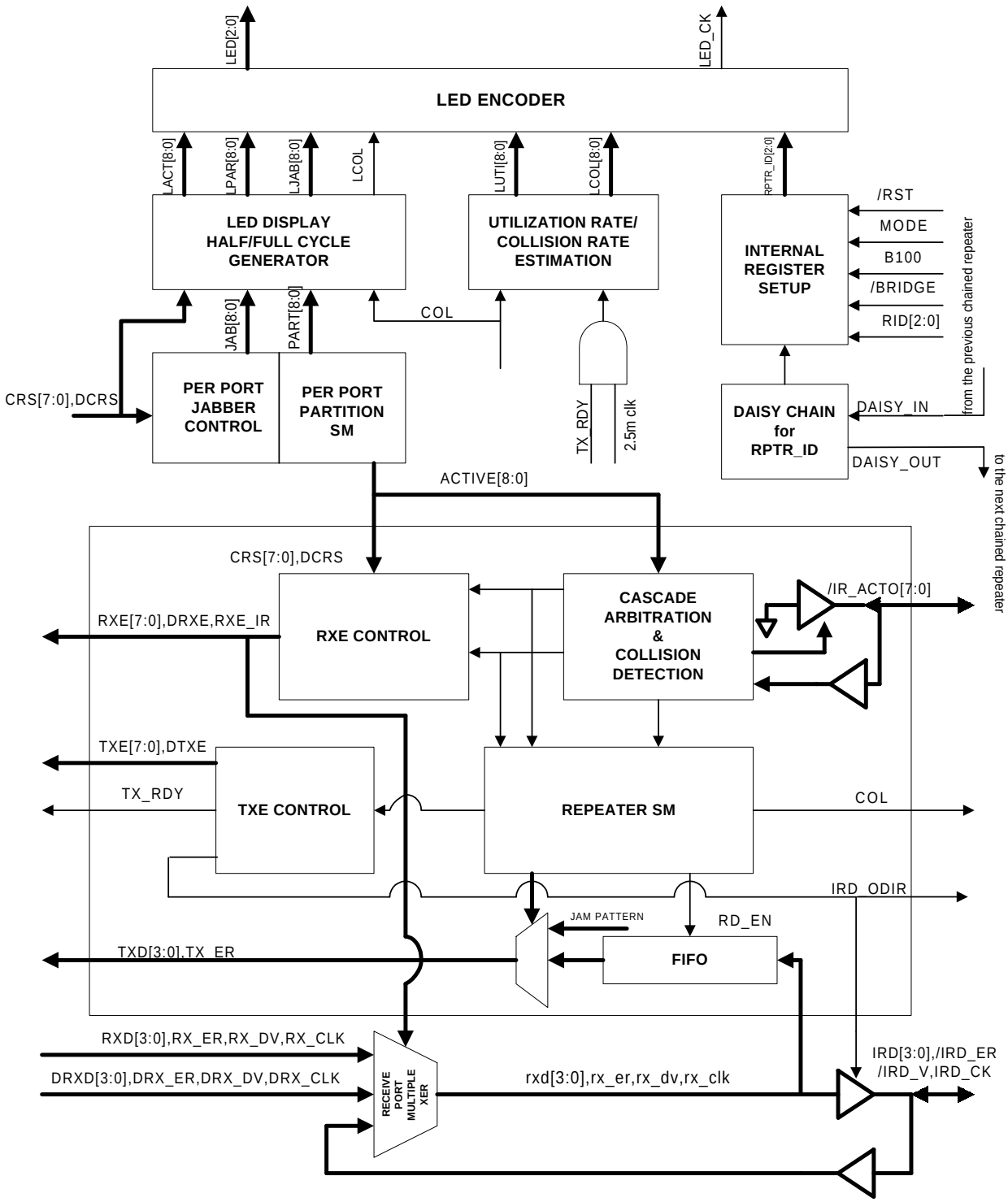


Fig - 4 Functional Block Diagram

3.1 Repeater State Machine

The repeater state machine is used to control repeater behavior, generates right signal in corresponding states. The repeater state machine is in Idle state when there is no carrier presented on any ports **.** When there is only one port has receive activity, the repeater state machine will enter Data - forwarding State to ensure correct data forwarding to other connected ports. If collision happens anytime, The repeater state machine detects collision then send jam pattern to all ports until collision ceases.

idle State

The idle state happens when these conditions exists:

a. /RST is low.
b. All CRS[7:0] and DCRS are not asserted high in single chip application.
c. Repeater sense no inter repeater active signal in cascade application, that is, all /IR_ACTO[7:0] remains high.

Data Forwarding State

The state happens when these conditions exists:

a. Only one signal asserted among CRS[7:0] and DCRS in single chip application.
b. Only one of IR_ACTO[7:0] become low if in cascade application.

The repeater state machine stores receiving packet and transmits to all other ports except for

1. The port is jabbered.
2. The port is isolated.

Collision State

The Collision State happens when these conditions exists:

a. There are two or more signals asserted high among CRS[7:0] and DCRS in single chip system.
b. There are two or more signals asserted low among /IR_ACTO[7:0] in cascade system.
c. Only one carrier exists but RXDV still low exceeds 4 clock cycles.The repeater sends collision pattern to all ports.

One Port Left State

The state happens only when there is no collision but still one port which experienced collision has receive activity. The repeater remains send collision pattern to all ports except the port.

3.2 RXE /TXE CONTROL

Idle state

The repeater sends no data to any port.
RXE(ALL) = 0, RXE_IR = 0.
TXE(ALL) = 0, TXE_IR = 0.

Data Forwarding state

If ACTIVE(X) = 1, X is the local connected port,
RXE(X) = 1, RXE(ALL-X) = 0, RXE_IR = 0.
TXE(X) = 0, TXE(ALL-X) = 1, TXE_IR = 1.

If ACTIVE(X) = 1, X is the inter repeater port,
RXE(ALL) = 0, RXE_IR =1.
TXE(ALL) = 1, TXE_IR = 0.

Collision state

The repeater sends jam pattern to all ports.
RXE(ALL) = 0, RXE_IR = 0.
TXE(ALL) = 1, TXE_IR = 0.

One Port Left state

The repeater sends jam pattern to all other port except for the still activity port.
RXE(ALL) = 0, RXE_IR = 0.
TXE(ALL-X) = 1, TXE_IR = 0. Suppose X is the one left port.

3.3 Jabber State Machine

To prevent an illegally long reception of data from reaching the repeater unit, each port has its own jabber timer. If a reception exceeds this duration (64K bit times for AX88860), the jabber condition will be detected. In this condition, repeater unit will disable receive and transmit packets for the jabbered port and the other ports remain the normal operation.

When the carrier is no longer detected for the jabbered port or reset the repeater, the jabber function will be clear and re-enable reception and transmission.

3.4 Partition State Machine

The partition state machine is used to protect network from being upset when a port suffer continuous collision, each port uses a partition state machine to detect and prevent this condition. When a port suffer from continuous 64 times of collision events, then it goes to partition state. The partitioned port will be not released until a packet without collision be transmitted(more than 512 bit times for AX88860) or reset the repeater.

3.5 Expansion Logic(Cascade Interface)

The expansion logic is used to stack numerous repeaters to expend the number of connected ports. The expansion logic can be divided into two types:

Expansion Logic without Buffer (minimum mode)

In this mode, use /IR_ACTO[7:0] to cascade repeaters in back plane. Just connect /IR_ACTO[7:0] of all repeaters without using buffer. This mode is supposed to cascade repeaters on the same board. In this application, the stackable system can reach to 4 repeaters.

Expansion Logic with Buffer (maximum mode)

This mode is entered with the setting of /DIS_DMII = 0, the dedicated port isn‘t existed again in this mode. Now the dedicated pins DRXD[3:0], DCRS, DRX_DV, DRX_ER, DRX_CLK play a role as IR_ACTI[7:0]. Use /IR_ACTO[7:0] and /IR_ACTI[7:0] to cascade repeaters in back plane. Buffers are used both in /IR_ACTO[7:0] and /IR_ACTI[7:0]. The mode is supposed to cascade repeaters on different boards via cables. In this application, the stackable system can reach to 8 repeaters.

/IR_ACTO<7:0> are driven according to repeater ID and receive activity of local connected ports as follows:

Repeater ID	IDLE state	Only One Port Activity	More than One Port Activity
000	11111111	11111110	11111100
001	11111111	11111101	11111100
010	11111111	11111011	11111001
011	11111111	11110111	11110011
100	11111111	11101111	11100111
101	11111111	11011111	11001111
110	11111111	10111111	10011111
111	11111111	01111111	00111111

Note: All /IR_ACTO[7:0] will be in open-drain status when they aren‘t driven. These signals present high via external pull high resister.

3.6 Data Flow control

The signals on the IR bus (such as IRD[3:0], IRD_V_N, IRD_ER_N, IRD_CK) flow either into or out of the repeater depending upon the repeater‘s state. Only if the repeater receive packet from local port without collision occurs, the IR signals flow out of repeater. Otherwise, these IR signals flow into repeater.

In cascade system, it must guarantee that only one repeater drives these signals to avoid contention.

3.7 RID Receive-Transmit Interface(Daisy Chain Logic)

In the cascade system, repeater ID of each chip will be re-arranged by serial in/serial out daisy chain logic. The logic use DAISY_IN pin to monitor the RID value of the previous chained chip, and override the original ID of the current chip with the value of (RID+1) . Use the DAISY_OUT pin to periodically (about 200us) send out the exact RID of the current chip to inform the next chained chip. By this way, each repeater chip in 8 AX88860 stackable application will keep unique ID of itself. The RID is used in inter repeater bus arbitration.

DAISY_IN/OUT frame format

idle	start bit	data0	data1	data2	data3
1	0	RID[0]	RID[1]	RID[2]	PARITY

Notes: PARITY = 1 when sum of 1‘s in RID[2:0] is even

If no daisy-chain input, that is, DAISY_IN keep high, the RID of current chip can be clear to 0 during time out
period. The timer for time out is about 4sec.

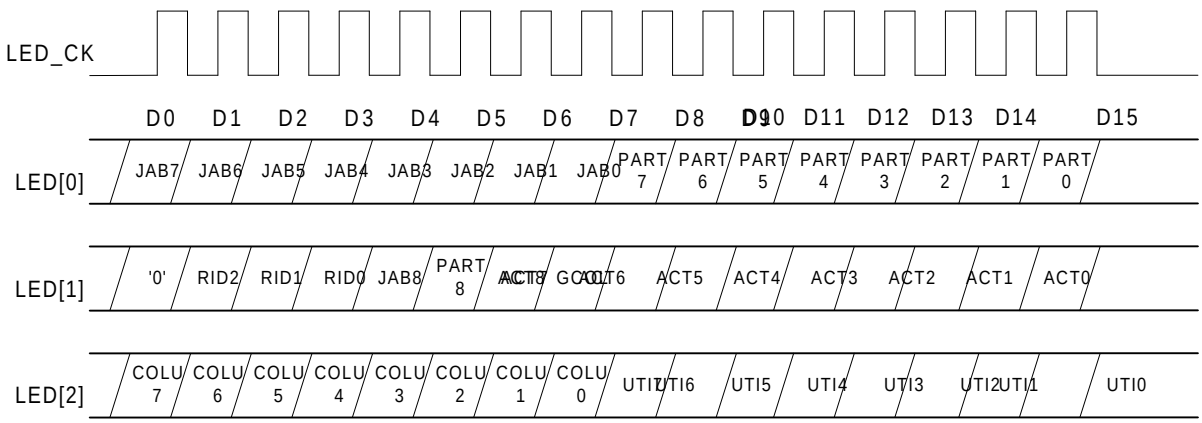
There are a input setting , /DIS_DAISY, which enable/disable daisy-chain function. With the low setting , the RID of current chip don‘t care the present data on DAISY_IN and can‘t be overrided.

3.8 LED Display Interface

AX88860 provides per-port LED status indication for partition, jabber, link/activity and support rate - based LED for global utilization (%) and global collision (%).Detail function is described on the previous pin description(LED interface). LED[7:0] are all active low. There are two display ways : complicated and simple way. It depends on the setting of MODE.

Multiple chips cascaded application (MODE = 1)

LED[2:0] Status Driver Wave-form as follows :



Notes: a. PART8~0indicates partition status for each port
b. JAB8~0 indicates jabber status for each port
c. ACT8~0 indicates activity status for each port
d. RID2~0 is the ID of repeater chip
e. COLU7~0 indicate global collision rate for each 104.8ms sampling period.
f. UTI7~0 indicate global utilization rate for each 104.8ms sampling period.

It must use external shift register to decode data on LED[2:0]. The application shows as follows:

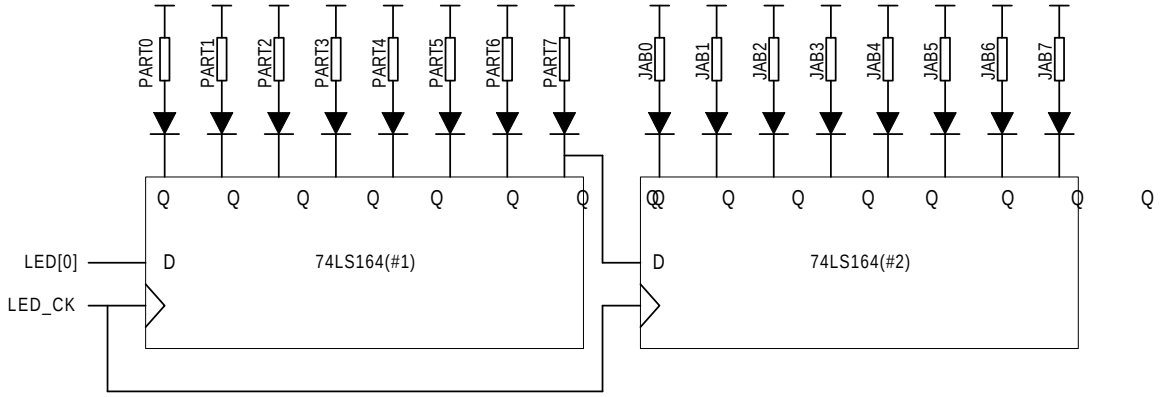


Fig - 5 Application for LED display

If the user don‘t want to show jabber status, take away the latter 74LS164(#2). The application is the same for LED[2:1].

Single chip application (MODE=0)

In this mode, the inter repeater pins are not useful, these pin can be used for display led status directly. Then the led application become simple.

	dump signal		dump signal		dump signal
/IR_ACTO[0]	PART[0]	IRD[0]	ACT[0]	LED[0]	UTI[0]
/IR_ACTO[1]	PART[1]	IRD[1]	ACT[1]	LED[1]	UTI[1]
/IR_ACTO[2]	PART[2]	IRD[2]	ACT[2]	LED[2]	UTI[2]
/IR_ACTO[3]	PART[3]	IRD[3]	ACT[3]	LED_CK	UTI[3]
/IR_ACTO[4]	PART[4]	/IRD_V	ACT[4]	RID[0]	UTI[4]
/IR_ACTO[5]	PART[5]	/IRD_ER	ACT[5]	RID[1]	UTI[6]
/IR_ACTO[6]	PART[6]	IRD_CK	ACT[6]	RID[2]	GCOL
/IR_ACTO[7]	PART[7]	IRD_ODIR	ACT[7]		
DAISY_OUT	PART[8]	RST_DLY	ACT[8]		

4.0 INTERNAL REGISTERS

4.1 Configuration Register (CONFIG)

Bit	Bit Name	Default	Bit Description
D4	MODE	1	MODE=1, multiple chip cascade application. MODE=0, single chip application.
D3	/DIS_DMII	1	/DIS_DMII= 1, one dedicated port are supported. /IR_ACTI[7:0] pins are not supported. /DIS_DMII = 0, disable the dedicated port and /IR_ACTI[7:0] pins are supported.
D2	B100	1	B100 = 1, all ports are 100Mb/ps B100 = 0, all ports are 10Mb/ps
D1	/DIS_DAISY	1	/DIS_DAISY = 1, Enable RID daisy-chain function. /DIS_DAISY = 0, Disable RID Daisy-chain Input: No matter what kind of data input from DAISY_IN pin the RPTR_ID can't be override.
D0	/BRIDGE	1	/BRIDGE = 1, the dedicated port connect to PHY type device. /BRIDGE = 0, the dedicated port connect to MAC or Bridge port

4.2 Repeater ID Register(RPTR_ID)

Bit	Bit Name	Default	Bit Description
D2-D0	RPTR_ID[2:0]	111	Repeater ID : At the rising edge of /RST , the value of RID[2:0] are latched in this register as RPTR_ID[2:0]. The value can be override according to the data from serial daisy-chain DAISY_IN pin except /DIS_DAISY is configured to "low" .

5.0 ELECTRICAL SPECIFICATION AND TIMING

5.1 Absolute Maximum Ratings

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Storage Temperature	Ts	-55	+150	°C
Supply Voltage	Vcc	-0.5	+7	V
Input Voltage	Vin	Vss-0.5	Vdd+0.5	V
Output Voltage	Vout	Vss-0.5	Vdd+0.5	V
Lead Temperature (soldering 10 seconds maximum)	Tl	-55	+250	°C

Note : Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability

5.2 General Operation Conditions

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Supply Voltage	Vdd	+4.75	+5.25	V

5.3 DC Characteristics

(Vdd=4.75V to 5.25V, Vss=0V, Ta=0°C to 70°C)

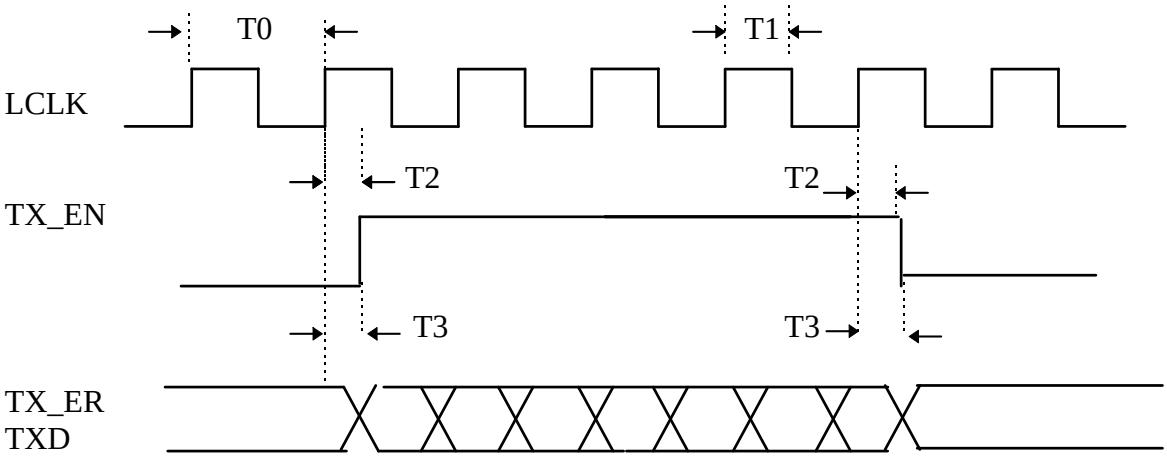
Description	SYM	Min	Max	Units
Low Input Voltage	Vil	Vss-0.5	0.8	V
High Input Voltage	Vih	2	Vdd+0.5	V
Low Output Voltage	Vol		0.4	V
High Output Voltage	Voh	2.4		V
Input Leakage Current 1 (Note 1)	Iil1		10	uA
Input Leakage Current 2 (Note 2)	Iil1		500	uA
Output Leakage Current	Iol		10	uA

Note :

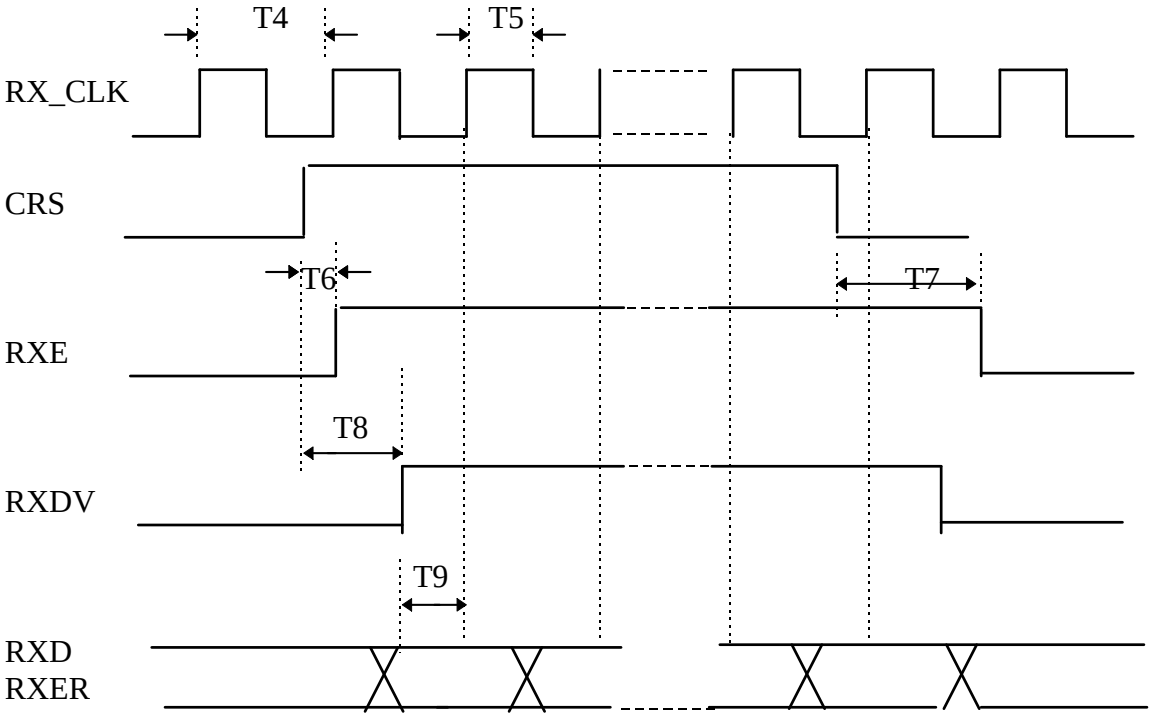
1. All the input pins without pull low or pull high.
2. Those pins had been pull low or pull high.

5.4 AC specifications

5.4.1 MII Interface Timing Tx & Rx

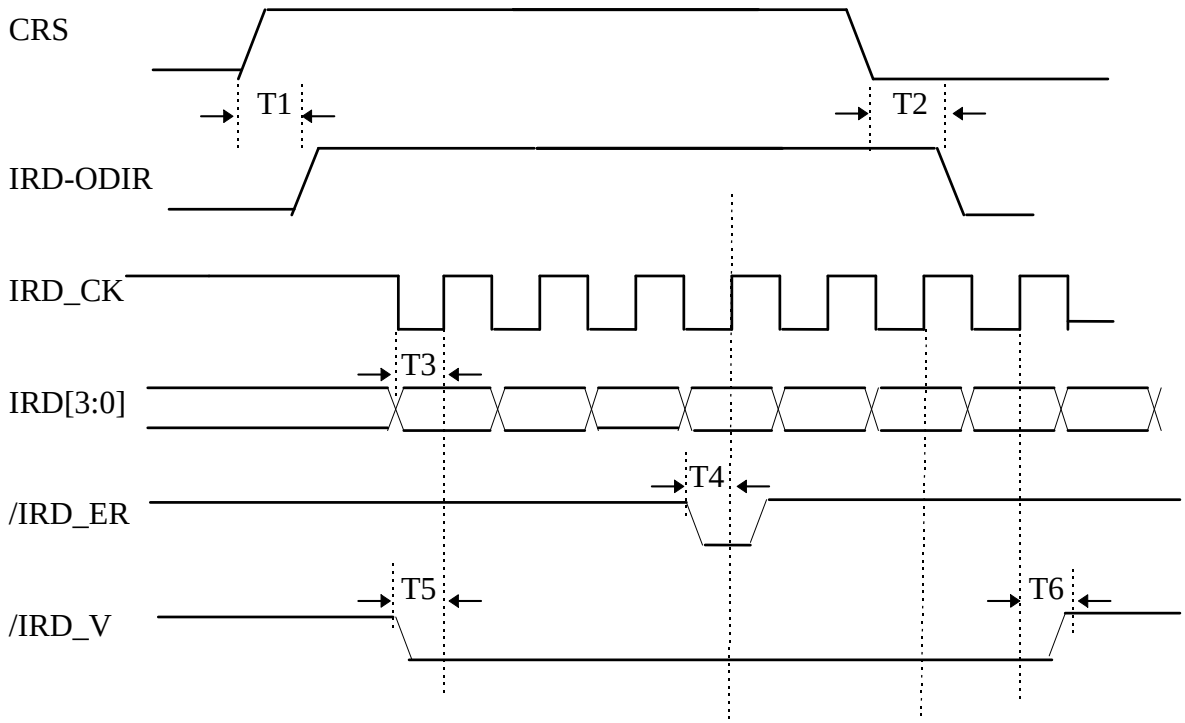


Symbol	Description	Min	Typ.	Max	Units
T0	Local Clock Cycle Time	39.996	40	40.004	ns
T1	Local Clock High Time	14	20	26	ns
T2	TX_EN Delay from LCLK High	7.440		21.760	ns
T3	TX_ER or TXD Delay from LCLK High	3.410		13.320	ns



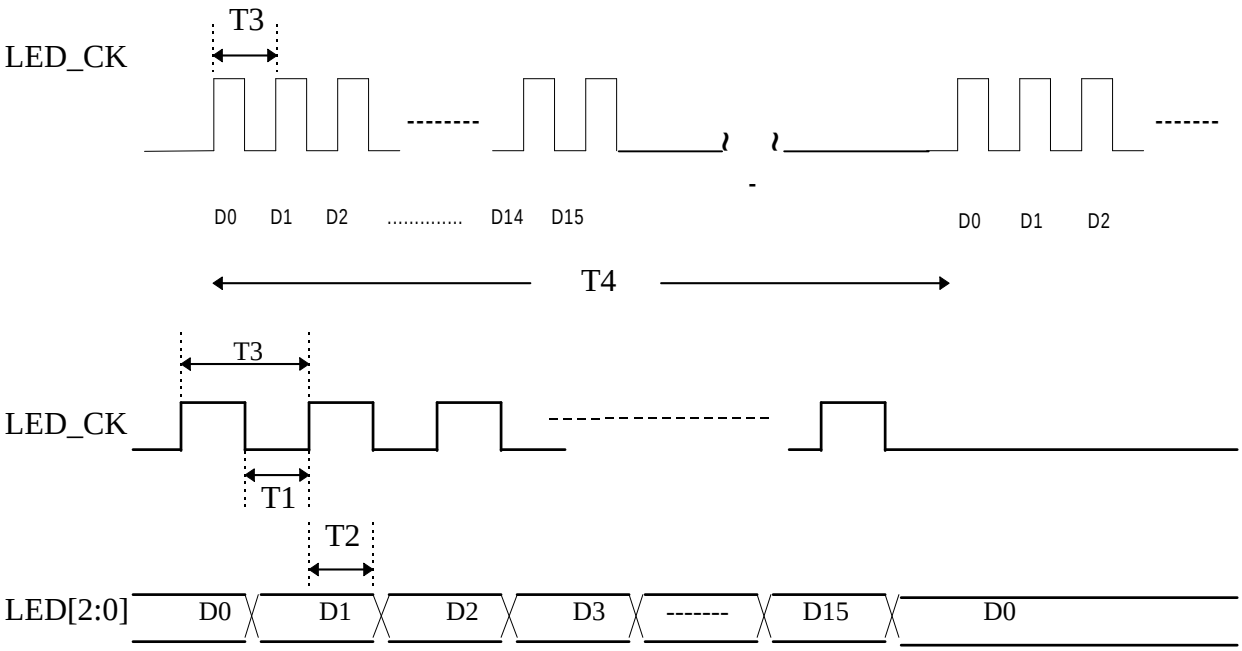
Symbol	Description	Min	Typ.	Max	Units
T4	RX_CLK Clock Cycle Time	39.996	40	40.004	ns
T5	RX_CLK Clock High Time	14	20	26	ns
T6	CRS to RXE Assertion Delay			20	ns
T7	CRS to RXE De-assertion Delay	160		200	ns
T8	CRS to RXDV Delay Requirement	40		160	ns
T9	RXD or RXDV or RX_ER setup to RX_CLK rise time	10		-	ns

5.4.2 Expansion Bus



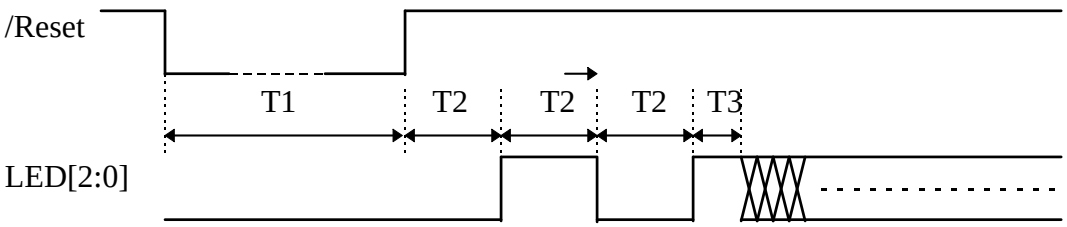
Symbol	Description	Min	Max	Units
T1	CRS Assertion to IRD-ODIR Assertion	-	20	ns
T2	CRS De-Assertion to IRD-ODIR De-Assertion	160	200	ns
T3	IRD[3:0] Setup Time to IRD-CK High	10	-	ns
T4	/IRD_ER Setup Time to IRD-CK High	10	-	ns
T5	/IRD_V Setup Time to IRD-CK High	5	-	ns
T6	/IRD_V Hold Time from IRD-CK High	5	-	ns

5.4.3 LED DISPLAY



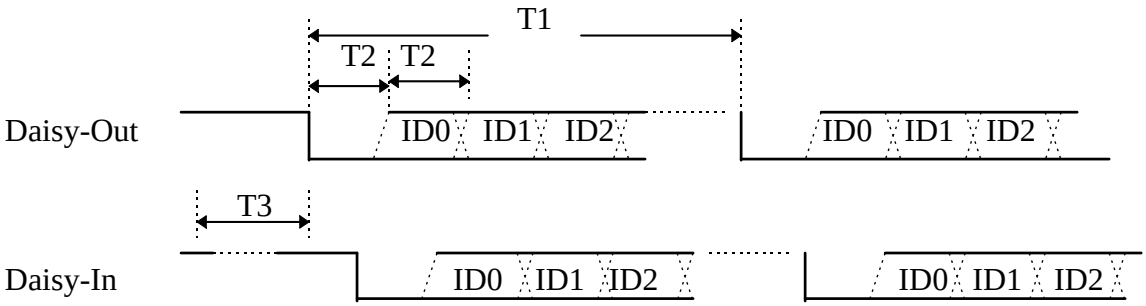
Symbol	Description	Min	Typ.	Max	Units
T1	LED setup to LED_CK High	190		200	ns
T2	LED hold from LED_CK High	200		210	ns
T3	LED_CK Period Width		400		ns
T4	continuous 16 LED_CK Cycle Time		52.4		ms

5.4.4 LED Display After Reset



Symbol	Description	Min	Typ.	Max	Units
T1	Repeater reset time	1000			ns
T2	LED Blink Time After Reset		838.4		ms
T3	LED Dark Time Before Normal Display		419.2		ms

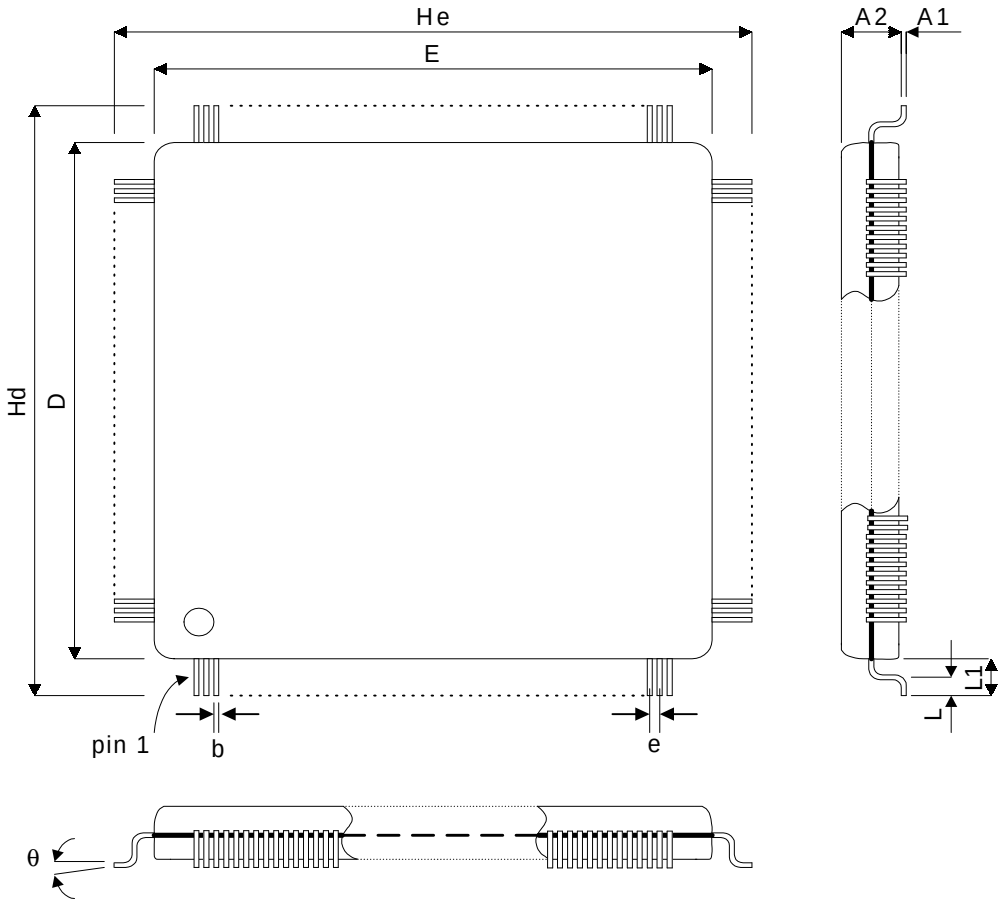
5.4.5 Repeater ID Daisy Chain



Symbol	Description	Min	Typ.	Max	Units
T1	Daisy Chain One Burst period		204.8		us
T2	Start Bit Period or Data Width		12.8		us
T3	Time-out occur when no data present on Daisy_in *		3.8		s

Note : Daisy-Chain Data-In Time-out stands for no input data (always high level) for the specific time.

6.0 PACKAGE INFORMATION



SYMBOL	MILIMETER		
	MIN.	NOM	MAX
A1	0.05	-	0.25
A2	2.55	2.65	2.75
b	0.25	0.30	0.40
D	13.80	14.00	14.20
E	19.80	20.00	20.20
e		0.65	
Hd	17.60	17.90	18.2
He	23.60	23.90	24.2
L	0.60	0.80	1.00
L1		2.00	
θ	0		8