



UT7422-H

Preliminary

Power MOSFET

40A, 30V N-CHANNEL MOSFET

DESCRIPTION

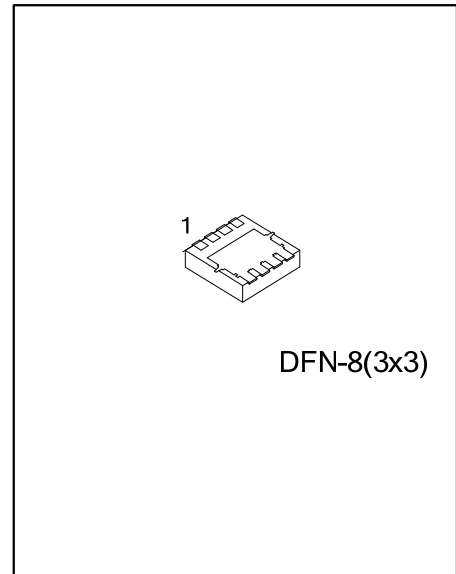
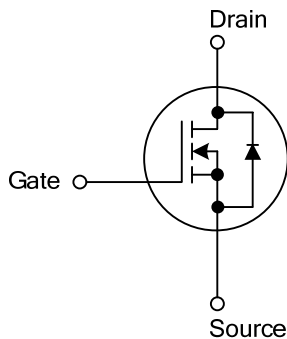
The UTC **UT7422-H** is an N-channel MOSFET, it uses UTC's advanced technology to provide the customers with a minimum on state resistance, etc.

The UTC **UT7422-H** is suitable for load switch and battery protection applications.

FEATURES

- * $R_{DS(ON)} < 4.3m\Omega @ V_{GS}=10V, I_D=20A$
- $R_{DS(ON)} < 6.0m\Omega @ V_{GS}=4.5V, I_D=16A$
- * Low $R_{DS(ON)}$

SYMBOL



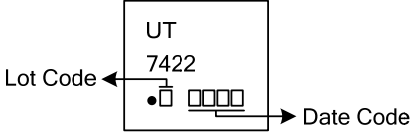
ORDERING INFORMATION

Ordering Number	Package	Pin Assignment								Packing
		1	2	3	4	5	6	7	8	
UT7422G-K08-3030-R	DFN-8(3x3)	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT7422G-K08-3030-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) K08-3030: DFN-8(3x3)</p> <p>(3) G: Halogen Free and Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current (Note 6)	I_D	40	A
Pulsed Drain Current (Note 4)	I_{DM}	200	A
Continuous Drain Current	I_{DSM}	20	A
Avalanche Current (Note 4)	I_{AS}, I_{AR}	45	A
Avalanche Energy $L=0.1\text{mH}$ (Note 4)	E_{AS}, E_{AR}	101	mJ
Power Dissipation (Note 3)	P_D	36	W
Power Dissipation (Note 2)	P_{DSM}	3.1	W
Junction Temperature	T_J	$-55\sim+150$	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	$-55\sim+150$	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

- The value of θ_{JA} is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $\theta_{JA} \leq 10\text{s}$ value and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.
- The power dissipation P_D is based on $T_{J(\text{MAX})}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.
- The θ_{JA} is the sum of the thermal impedance from junction to case θ_{JC} and case to ambient.
- The maximum current rating is package limited.

■ THERMAL CHARACTERISTICS

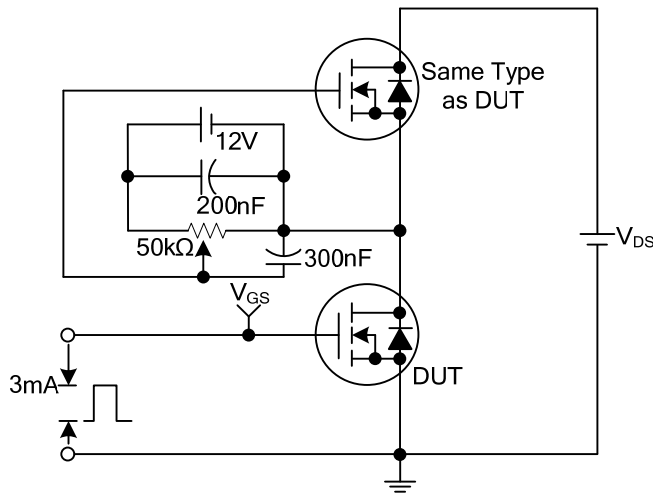
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient (Note 2, 5)	θ_{JA}	75	$^\circ\text{C}/\text{W}$
Junction-to-Case	θ_{JC}	3.4	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise noted)

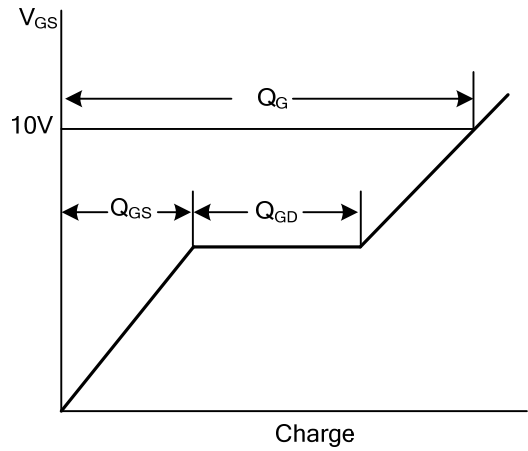
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PARAMETERS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$			1	μA
		$V_{DS}=30\text{V}, V_{GS}=0\text{V}, T_J=55^\circ\text{C}$			5	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$			100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.3	1.85	2.4	V
On State Drain Current	$I_{D(ON)}$	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	200			A
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=20\text{A}$		3.5	4.3	m Ω
		$V_{GS}=10\text{V}, I_D=20\text{A}, T_J=125^\circ\text{C}$		5.5	6.8	m Ω
		$V_{GS}=4.5\text{V}, I_D=16\text{A}$		4.5	6	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5\text{V}, I_D=20\text{A}$		85		S
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1.0\text{MHz}$	1950	2445	2940	pF
Output Capacitance	C_{OSS}		270	390	510	pF
Reverse Transfer Capacitance	C_{RSS}		130	220	310	pF
Gate Resistance	R_G	$V_{DS}=0\text{V}, V_{GS}=0\text{V}, f=1.0\text{MHz}$	1.2	2.4	3.6	Ω
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, I_D=20\text{A}$	32	41	50	nC
Total Gate Charge	Q_G	$V_{GS}=4.5\text{V}, V_{DS}=15\text{V}, I_D=20\text{A}$	15	19	24	nC
Gate to Source Charge	Q_{GS}		7.2			nC
Gate to Drain Charge	Q_{GD}		6.6			nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, R_L=0.75\Omega,$ $R_{GEN}=3\Omega$		7		ns
Rise Time	t_R		5			ns
Turn-OFF Delay Time	$t_{D(OFF)}$		41.5			ns
Fall-Time	t_F		10.5			ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Diode Forward Voltage	V_{SD}	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.7	1	V
Maximum Body-Diode Continuous Current (Note)	I_S				40	A
Body Diode Reverse Recovery Time	t_{rr}	$I_F=20\text{A}, dI/dt=500\text{A}/\mu\text{s}$		17.5	22	ns
Body Diode Reverse Recovery Charge	Q_{rr}		31	40		nC

Note: The maximum current rating is package limited.

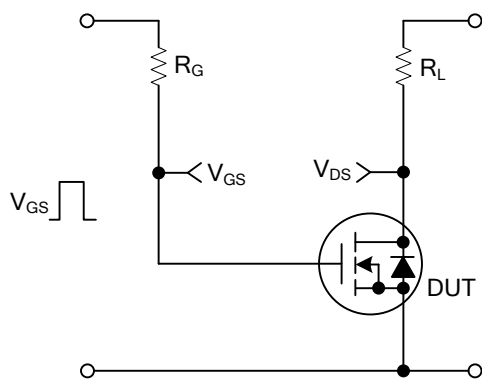
■ TEST CIRCUITS AND WAVEFORMS



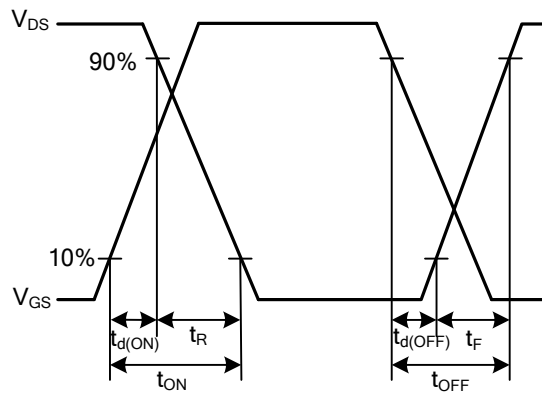
Gate Charge Test Circuit



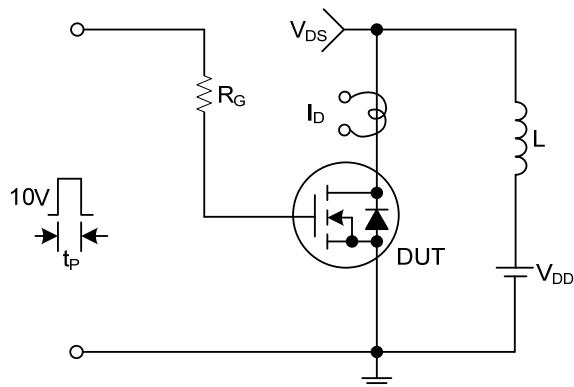
Gate Charge Waveforms



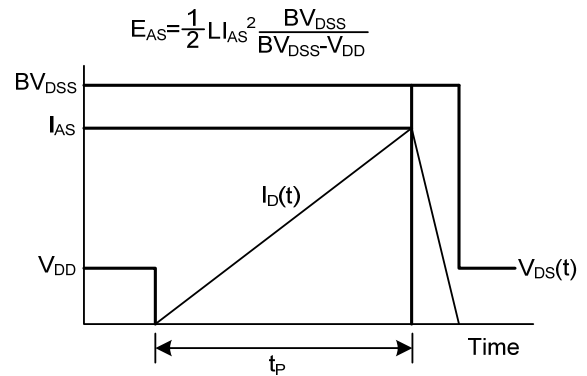
Resistive Switching Test Circuit



Resistive Switching Waveforms

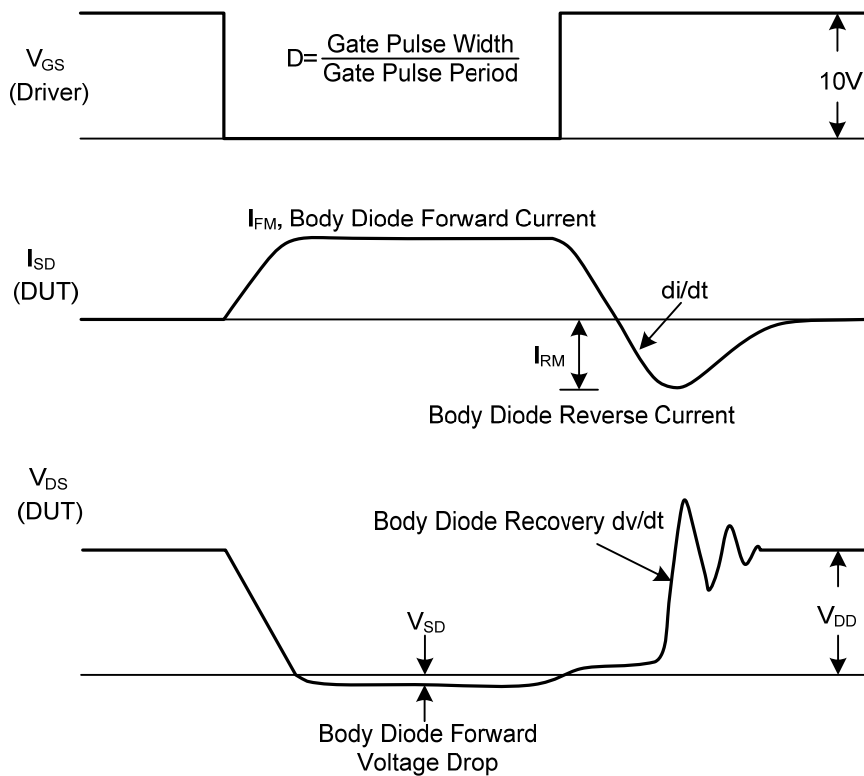
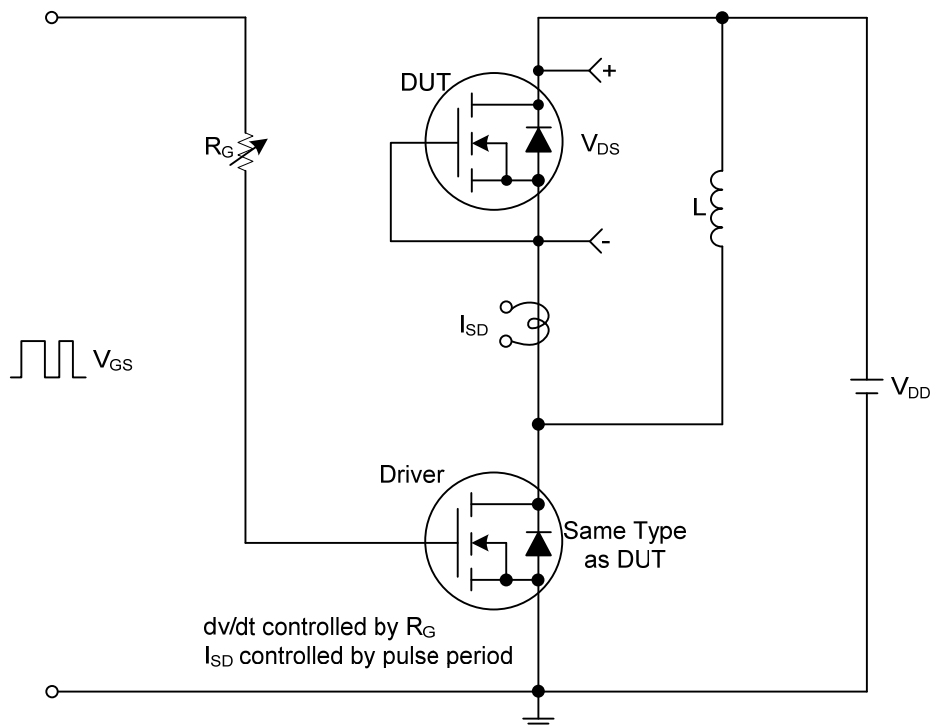


Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)



Peak Diode Recovery dv/dt Test Circuit and Waveforms

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