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Product List

SM39R4051W20, SM39R2051W20

Description

The original 8052 had 12-clock architecture. A machine cycle needed 12 clocks and most instructions were either one or two machine cycles. Thus except for the MUL and DIV instructions, the 8052 used either 12 or 24 clocks for each instruction. Furthermore, each cycle in the 8052 used two memory fetches. In many cases the second fetch was dummy, and extra clocks were wasted.

The SM39R4051 is a core of a fast single-chip 8-bit microcontroller. It is a fully functional 8-bit embedded controller that executes all ASM51 instructions and has the same instruction set as the MCS-51.

Ordering Information

SM39R4051ihhkL yymm

i: process identifier {W = 2.7V ~ 5.5V}

hh: pin count

k: package type postfix {as table below }

L:PB Free identifier

{No text is Non-PB free , "P" is PB free}

yy: year

mm: month

v: version identifier{ A, B,...}

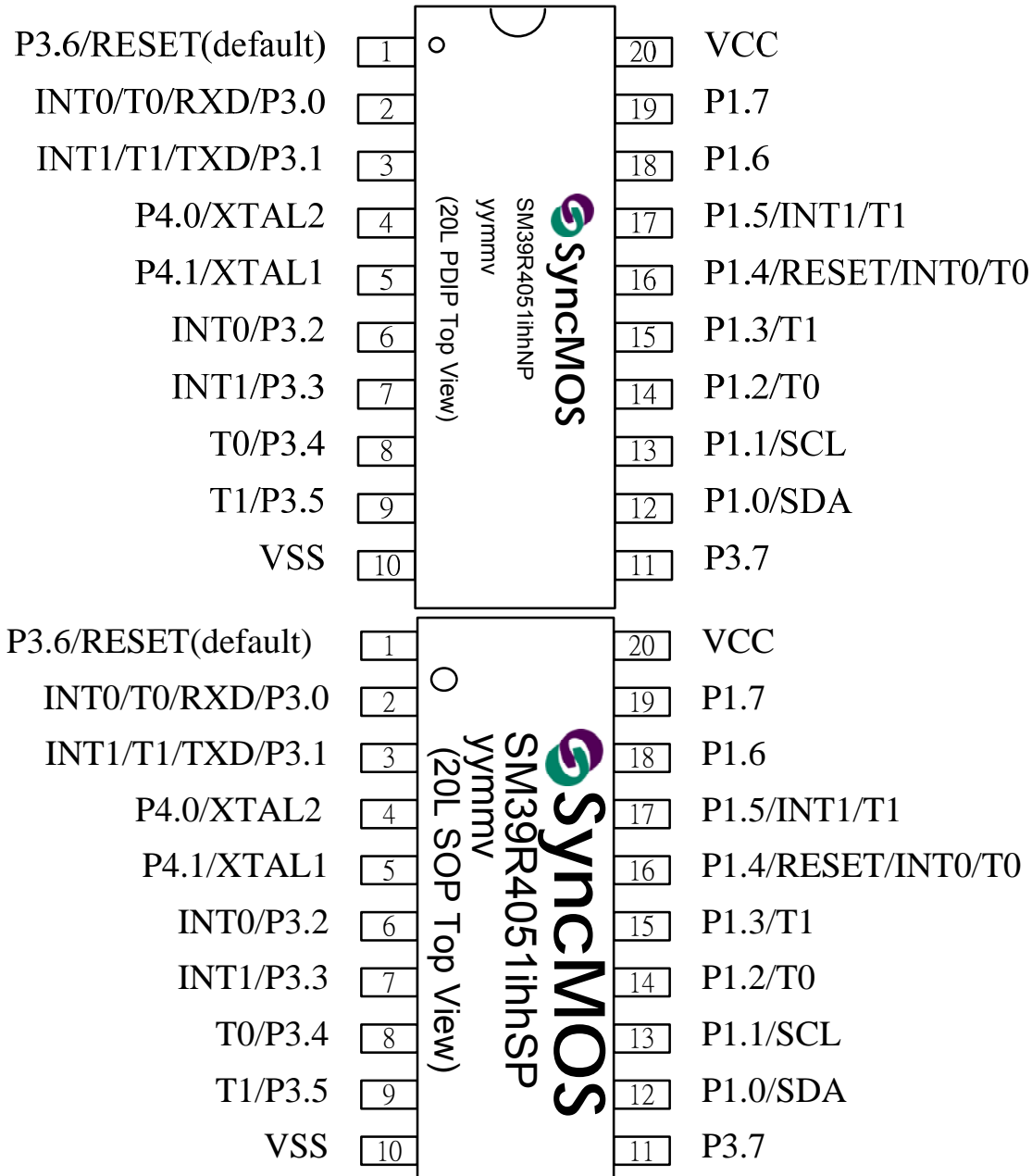
| Postfix | Package | Pin / Pad Configuration |
|---------|----------------|-------------------------|
| N | PDIP (300 mil) | Page 4 |
| S | SOP (300 mil) | Page 4 |

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Features

- Operating Voltage: 2.7V ~ 5.5V
- High speed architecture of 1 clock/machine cycle runs up to 25MHz.
- 1~8T modes are software programmable.
- Instruction-set compatible with MCS-51.
- Internal OSC with range 1MHz~24MHz
- 4K/2K Bytes on-chip flash program memory.
- 256 bytes RAM as standard 8052,
- One serial peripheral interfaces in full duplex mode.
 - Synchronous mode, fixed baud rate,
 - 8-bit UART mode, variable baud rate.
 - 9-bit UART mode, fixed baud rate,
 - 9-bit UART mode, variable baud rate.
- Additional Baud Rate Generator
- Two 16-bit Timer/Counters. (Timer 0, 1)
- 18 GPIOs(20L PDIP&SOP)
- Programmable watchdog timer.
- One IIC interface. (Master/Slave mode)
- On-chip flash memories support ISP/IAP/ICP and EEPROM functions.
- ISP service program space configurable in N*256 byte (N=0 to 4) size.
- On-Chip in-circuit emulator (ICE) functions with On-Chip Debugger (OCD).
- EMI reduction mode (ALE output inhibited).
- LVI/LVR.
- IO PAD ESD over 4KV.
- Enhance user code protection.
- External interrupt 0, 1 with four priority levels.
- Power management unit for IDLE and power down modes.

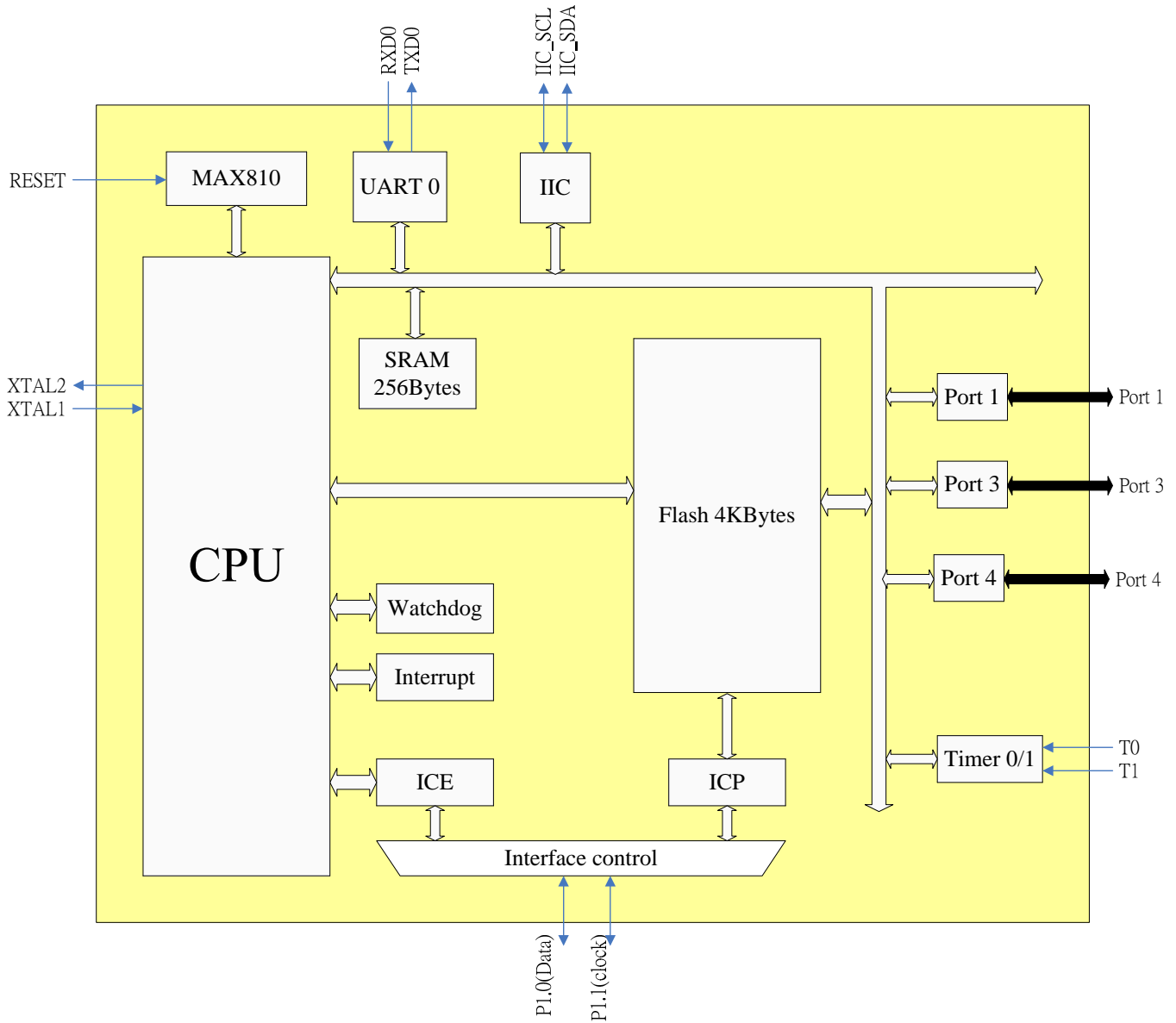
Pin Configuration



Notes :

1. The pin Reset/P3.6 factory default is Reset, user must keep this pin at low during power-up. User can configure it to GPIO (P3.6) by a flash programmer.
2. To avoid accidentally entering ISP-Mode(refer to section 13.4), care must be taken not asserting pulse signal at P3.0 during power-up while P1.5 are set to high.
3. To apply ICP function, SDA/P1.0 and SCL/P1.1 must be set to Bi-direction mode if they are configured as GPIO in system.

Block Diagram



Pin Description

| 20L PDIP/SOP | Symbol | I/O | Description |
|--------------|----------------------|-----|--|
| 1 | RESET(default)/ P3.6 | I/O | Reset pin(default) & Bit 6 of port 3 |
| 2 | P3.0/RXD/#INT0/T0 | I/O | Bit 0 of port 3 & Serial interface channel receive/transmit data & (External interrupt 0 or Timer 0 external input) |
| 3 | P3.1/TXD/#INT1/T1 | I/O | Bit 1 of port 3 & Serial interface channel transmit data or receive clock in mode 0 & (External interrupt 1 or Timer 1 external input) |
| 4 | XTAL2/P4.0 | I/O | Crystal output & Bit 0 of port 4 |
| 5 | XTAL1/P4.1 | I/O | Crystal input & Bit 1 of port 4 |
| 6 | P3.2/#INT0 | I/O | Bit 2 of port 3 & External interrupt 0 |
| 7 | P3.3/#INT1 | I/O | Bit 3 of port 3 & External interrupt 1 |
| 8 | P3.4/T0 | I/O | Bit 4 of port 3 & Timer 0 external input |
| 9 | P3.5/T1 | I/O | Bit 5 of port 3 & Timer 1 external input |
| 10 | VSS | I | Power supply |
| 11 | P3.7 | I/O | Bit 7 of port 3 |
| 12 | P1.0/SDA | I/O | Bit 0 of port 1 & On-Chip Instrumentation Command and data I/O pin synchronous to OCI_SCL in ICE and ICP functions |
| 13 | P1.1/SCL | I/O | Bit 1 of port 1 & On-Chip Instrumentation Clock I/O pin of ICE and ICP functions |
| 14 | P1.2/T0 | I/O | Bit 2 of port 1 & Timer 0 external input |
| 15 | P1.3/T1 | I/O | Bit 3 of port 1 & Timer 1 external input |
| 16 | P1.4/#INT0/T0/RESET | I/O | Bit 4 of port 1 & (External interrupt 0 or Timer 0 external input or RESET) |
| 17 | P1.5/#INT1/T1 | I/O | Bit 5 of port 1 & (External interrupt 1 or Timer 1 external input) |
| 18 | P1.6 | I/O | Bit 6 of port 1 |
| 19 | P1.7 | I/O | Bit 7 of port 1 |
| 20 | VDD | I | Power supply |

The Special Function Pin Can configured as below Table (Can be Select By SFR) :

| Signal | Default | Option1 | Option2 | Option3 |
|--------|---------|----------|----------|----------|
| #INT0 | 6(P3.2) | 2(P3.0) | 15(P1.3) | 16(P1.4) |
| #INT1 | 7(P3.3) | 3(P3.1) | 14(P1.2) | 17(P1.5) |
| T0 | 8(P3.4) | 14(P1.2) | 16(P1.4) | 2(P3.0) |
| T1 | 9(P3.5) | 15(P1.3) | 17(P1.5) | 3(P3.1) |

The RESET Pin Can configured as below Table (Can be Select By ICP or ISP) :

| Signal | Default | Option1 |
|--------|---------|---------|
| RESET | 1 | 16 |

The RESET Pin Can Be configured as I/O port P3.6 , when user use on-chip hardware RESET mechanism .

The XTAL2 can be configured as I/O port P4.0 by ICP or in ISP mode . when user use Oscillator (XTAL1 as clock input) or on-chip RC Oscillator is set to main system clock source .

The XTAL1 can be configured as I/O port P4.1 by ICP or in ISP mode , when user use on-chip RC Oscillator is set to main system clock source .

Special Function Register (SFR)

A map of the Special Function Registers is shown as below:

| Hex\Bin | X000 | X001 | X010 | X011 | X100 | X101 | X110 | X111 | Bin/Hex |
|---------|-------|---------|--------|-------|--------|--------|-------|-------|---------|
| F8 | IICS | IICCTL | IICA1 | IICA2 | IICRWD | IICEBT | | | FF |
| F0 | B | | | | | | | TAKEY | F7 |
| E8 | P4 | | | | | | | | EF |
| E0 | ACC | ISPFALH | ISPFAL | ISPFD | ISPFC | | LVC | SWRES | E7 |
| D8 | | | P3M0 | P3M1 | P4M0 | P4M1 | | | DF |
| D0 | PSW | | | | P1M0 | P1M1 | | | D7 |
| C8 | | | | | | | | | CF |
| C0 | IRCON | | | | | | | | C7 |
| B8 | IEN1 | IP1 | S0RELH | | | | | | BF |
| B0 | P3 | | | | | | WDTC | WDTK | B7 |
| A8 | IEN0 | IP0 | S0RELL | | | | | | AF |
| A0 | | | | P1WE | P3WE | | | | A7 |
| 98 | S0CON | S0BUF | | | | | | | 9F |
| 90 | P1 | AUX | | | | | | | 97 |
| 88 | TCON | TMOD | TL0 | TL1 | TH0 | TH1 | CKCON | IFCON | 8F |
| 80 | | SP | DPL | DPH | DPL1 | DPH1 | | PCON | 87 |
| Hex\Bin | X000 | X001 | X010 | X011 | X100 | X101 | X110 | X111 | Bin/Hex |

Note: Special Function Registers reset values and description for SM39R4051

| Register | Location | Reset value | Description |
|----------|----------|-------------|----------------------------|
| SP | 81h | 07h | Stack Pointer |
| DPL | 82h | 00h | Data Pointer 0 low byte |
| DPH | 83h | 00h | Data Pointer 0 high byte |
| DPL1 | 84h | 00h | Data Pointer 1 low byte |
| DPH1 | 85h | 00h | Data Pointer 1 high byte |
| PCON | 87h | 40h | Power Control |
| TCON | 88h | 00h | Timer/Counter Control |
| TMOD | 89h | 00h | Timer Mode Control |
| TL0 | 8Ah | 00h | Timer 0, low byte |
| TL1 | 8Bh | 00h | Timer 1, low byte |
| TH0 | 8Ch | 00h | Timer 0, high byte |
| TH1 | 8Dh | 00h | Timer 1, high byte |
| CKCON | 8Eh | 10h | Clock control register |
| IFCON | 8Fh | 40h | Interface control register |
| P1 | 90h | FFh | Port 1 |
| AUX | 91h | 00h | Auxiliary register |

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| Register | Location | Reset value | Description |
|----------|----------|-------------|---|
| S0CON | 98h | 00h | Serial Port 0, Control Register |
| S0BUF | 99h | 00h | Serial Port 0, Data Buffer |
| P1WE | A3h | FFh | Port 1 output enable |
| P3WE | A4h | FFh | Port 3 output enable |
| IEN0 | A8h | 00h | Interrupt Enable Register 0 |
| IP0 | A9h | 00h | Interrupt Priority Register 0 |
| S0RELL | AAh | 00h | Serial Port 0, Reload Register, low byte |
| P3 | B0h | FFh | Port 3 |
| WDTC | B6h | 04h | Watchdog timer control register |
| WDTK | B7h | 00h | Watchdog timer refresh key. |
| IEN1 | B8h | 00h | Interrupt Enable Register 1 |
| IP1 | B9h | 00h | Interrupt Priority Register 1 |
| S0RELH | BAh | 00h | Serial Port 0, Reload Register, high byte |
| IRCON | C0h | 00h | Interrupt Request Control Register |
| PSW | D0h | 00h | Program Status Word |
| P1M0 | D4h | 00h | Port 1 output mode 0 |
| P1M1 | D5h | 00h | Port 1 output mode 1 |
| P3M0 | DAh | 00h | Port 3 output mode 0 |
| P3M1 | DBh | 00h | Port 3 output mode 1 |
| P4M0 | DCh | 00h | Port 4 output mode 0 |
| P4M1 | DDh | 00h | Port 4 output mode 1 |
| ACC | E0h | 00h | Accumulator |
| ISPF AH | E1h | FFh | ISP Flash Address-High register |
| ISPF AL | E2h | FFh | ISP Flash Address-Low register |
| ISPF D | E3h | FFh | ISP Flash Data register |
| ISPF C | E4h | 00h | ISP Flash control register |
| LVC | E6h | 20h | Low voltage control register |
| SWRES | E7h | 00h | Software Reset register |
| P4 | E8h | FFh | Port 4 |
| B | F0h | 00h | B Register |
| TAKEY | F7h | 00h | Time Access Key register |
| IICS | F8h | 00h | IIC status register |
| IICCTL | F9h | 04h | IIC control register |
| IICA1 | FAh | A0h | IIC channel 1 Address 1 register |
| IICA2 | FBh | 60h | IIC channel 1 Address 2 register |
| IICRWD | FCh | 00h | IIC channel 1 Read / Write Data buffer |
| IICS2 | FDh | 00h | IIC status2 register |

Function Description

1. General Features

SM39R4051 is an 8-bit micro-controller. All of its functions and the detailed meanings of SFR will be given in the following sections.

1.1. Embedded Flash

The program can be loaded into the embedded 4KB/2KB Flash memory via its writer or In-System Programming (ISP). The high-quality Flash has a 100K-write cycle life, suitable for re-programming and data recording as EEPROM.

1.2. IO Pads

The SM39R4051 has three I/O ports: Port 1, Port 3 and Port 4. Ports 1, 3 are 8-bit ports and Port 4 is a 2-bit port. These are: quasi-bidirectional (standard 8051 port outputs), push-pull, open drain, and input-only. As description in section 5.

At 20L Package (DIP/SOP), the Int0, Int1, T0, T1 signal can be configured to other I/O as below:

| Signal | Default | Option1 | Option2 | Option3 |
|--------|---------|----------|----------|----------|
| #INT0 | 6(P3.2) | 2(P3.0) | 15(P1.3) | 16(P1.4) |
| #INT1 | 7(P3.3) | 3(P3.1) | 14(P1.2) | 17(P1.5) |
| T0 | 8(P3.4) | 14(P1.2) | 16(P1.4) | 2(P3.0) |
| T1 | 9(P3.5) | 15(P1.3) | 17(P1.5) | 3(P3.1) |

The RESET Pin Can Be configured as I/O port P3.6, when user use on-chip hardware RESET mechanism.

The XTAL2 and XTAL1 can be configured as I/O port by ICP or in ISP mode, when user use external OSC or on-chip RC Oscillator is set to main system clock source, show as below:

| | | External OSC | Internal OSC |
|-------------|-------|--------------|--------------|
| 20L package | Xtal1 | Xtal1 | P4.1 |
| | Xtal2 | P4.0 | P4.0 |

All the pins on P1, P3 and P4 are with slew rate adjustment to reduce EMI. The other way to reduce EMI is to disable the ALE output if unused. This is selected by its SFR. The IO pads can withstand 4KV ESD in human body mode guaranteeing the SM39R4051's quality in high electro-static environments.

1.3. Instruction timing Selection

The conventional 52-series MCUs are 12T, i.e., 12 oscillator clocks per machine cycle. SM39R4051 is a 1T to 8T MCU, i.e., its machine cycle is one-clock to eight-clock. In the other words, it can execute one instruction within one clock to only eight clocks.

| Mnemonic: CKCON | | | | | | | Address: 8Eh | |
|-----------------|-----|---|---|---|---|---|--------------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| - | ITS | | | - | - | - | - | 10H |

ITS: Instruction timing select.

| ITS [6:4] | Instruction timing |
|-----------|--------------------|
| 000 | 1T mode |
| 001 | 2T mode (default) |
| 010 | 3T mode |

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| | |
|-----|---------|
| 011 | 4T mode |
| 100 | 5T mode |
| 101 | 6T mode |
| 110 | 7T mode |
| 111 | 8T mode |

The default is in 2T mode, and it can be changed to another Instruction timing mode if CKCON [6:4] (at address 8Eh) is change any time. Not every instruction can be executed with one machine cycle. The exact machine cycle number for all the instructions are given in the next section.

1.4. RESET

1.4.1. Hardware RESET function

SM39R4051 provides on-chip hardware RESET mechanism, the reset duration is programmable by writer or ISP.

| |
|---------------------------------|
| on-chip hardware RESET duration |
| 25ms (default) |
| 200ms |
| 100ms |
| 50ms |
| 16ms |
| 8ms |
| 4ms |

1.4.2. Software RESET function

SM39R4051 provides one software reset mechanism to reset whole chip. To perform a software reset, the firmware must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the Software Reset register (SWRES) write attribute. After SWRES register obtain the write authority, the firmware can write FFh to the SWRES register. The hardware will decode a reset signal that "OR" with the other hardware reset. The SWRES register is self-reset at the end of the software reset procedure.

| Mnemonic | Description | Direct | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | RESET |
|-------------------------|--------------------------|--------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Software Reset function | | | | | | | | | | | |
| TAKEY | Time Access Key register | F7h | TAKEY [7:0] | | | | | | | | 00H |
| SWRES | Software Reset register | E7h | SWRES [7:0] | | | | | | | | 00H |

1.4.3. Time Access Key register (TAKEY)

| | | | | | | | | | | | |
|------------------------|---|---|---|---|---|---|---------------------|-------|--|--|--|
| Mnemonic: TAKEY | | | | | | | Address: F7H | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset | | | |
| TAKEY [7:0] | | | | | | | | 00H | | | |

Software reset register (SWRES) is read-only by default; software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the SWRES register write attribute. That is:

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah
```

1.4.4. Software Reset register (SWRES)

| | | | | | | | | | |
|------------------------|---|---|---|---|---|---|---|---------------------|--|
| Mnemonic: SWRES | | | | | | | | Address: E7H | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset | |
| SWRES [7:0] | | | | | | | | 00H | |

SWRES [7:0]: Software reset register bit. These 8-bit is self-reset at the end of the reset procedure.

SWRES [7:0] = FFh, software reset.

SWRES [7:0] = 00h ~ FEh, MCU no action.

1.4.5. Example of software reset

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah ; enable SWRES write attribute
MOV SWRES, #0FFh; software reset MCU
```

1.5. Clocks

The default clock is the external crystal. This clock is used during the initialization stage. The major work of the initialization stage is to determine the clock source used in normal operation.

The internal clock sources are from the on-chip RC-Oscillator with programmable frequency outputs as table 1-1, the clock source can set by writer or ICP.

Table 1-1: Selection of clock source

| Clock source |
|--|
| external crystal (use XTAL1 and XTAL2 pins) (default) |
| external crystal (only use XTAL1, the XTAL2 define as I/O) |
| 20MHz from on-chip RC-Oscillator |
| 16MHz from on-chip RC-Oscillator |
| 12MHz from on-chip RC-Oscillator |
| 8MHz from on-chip RC-Oscillator |
| 4MHz from on-chip RC-Oscillator |
| 2MHz from on-chip RC-Oscillator |
| 1MHz from on-chip RC-Oscillator |

2. Instruction Set

All SM39R4051 instructions are binary code compatible and perform the same functions as they do with the industry standard 8051. The following tables give a summary of the instruction set cycles of the SM39R4051 Microcontroller core.

Table 2-1: Arithmetic operations

| Mnemonic | Description | Code | Bytes | Cycles |
|---------------|---|-------|-------|--------|
| ADD A,Rn | Add register to accumulator | 28-2F | 1 | 1 |
| ADD A,direct | Add direct byte to accumulator | 25 | 2 | 2 |
| ADD A,@Ri | Add indirect RAM to accumulator | 26-27 | 1 | 2 |
| ADD A,#data | Add immediate data to accumulator | 24 | 2 | 2 |
| ADDC A,Rn | Add register to accumulator with carry flag | 38-3F | 1 | 1 |
| ADDC A,direct | Add direct byte to A with carry flag | 35 | 2 | 2 |
| ADDC A,@Ri | Add indirect RAM to A with carry flag | 36-37 | 1 | 2 |
| ADDC A,#data | Add immediate data to A with carry flag | 34 | 2 | 2 |
| SUBB A,Rn | Subtract register from A with borrow | 98-9F | 1 | 1 |
| SUBB A,direct | Subtract direct byte from A with borrow | 95 | 2 | 2 |
| SUBB A,@Ri | Subtract indirect RAM from A with borrow | 96-97 | 1 | 2 |
| SUBB A,#data | Subtract immediate data from A with borrow | 94 | 2 | 2 |
| INC A | Increment accumulator | 04 | 1 | 1 |
| INC Rn | Increment register | 08-0F | 1 | 2 |
| INC direct | Increment direct byte | 05 | 2 | 3 |
| INC @Ri | Increment indirect RAM | 06-07 | 1 | 3 |
| INC DPTR | Increment data pointer | A3 | 1 | 1 |
| DEC A | Decrement accumulator | 14 | 1 | 1 |
| DEC Rn | Decrement register | 18-1F | 1 | 2 |
| DEC direct | Decrement direct byte | 15 | 2 | 3 |
| DEC @Ri | Decrement indirect RAM | 16-17 | 1 | 3 |
| MUL AB | Multiply A and B | A4 | 1 | 5 |
| DIV | Divide A by B | 84 | 1 | 5 |
| DA A | Decimal adjust accumulator | D4 | 1 | 1 |

Table 2-2: Logic operations

| Mnemonic | Description | Code | Bytes | Cycles |
|------------------|--|-------|-------|--------|
| ANL A,Rn | AND register to accumulator | 58-5F | 1 | 1 |
| ANL A,direct | AND direct byte to accumulator | 55 | 2 | 2 |
| ANL A,@Ri | AND indirect RAM to accumulator | 56-57 | 1 | 2 |
| ANL A,#data | AND immediate data to accumulator | 54 | 2 | 2 |
| ANL direct,A | AND accumulator to direct byte | 52 | 2 | 3 |
| ANL direct,#data | AND immediate data to direct byte | 53 | 3 | 4 |
| ORL A,Rn | OR register to accumulator | 48-4F | 1 | 1 |
| ORL A,direct | OR direct byte to accumulator | 45 | 2 | 2 |
| ORL A,@Ri | OR indirect RAM to accumulator | 46-47 | 1 | 2 |
| ORL A,#data | OR immediate data to accumulator | 44 | 2 | 2 |
| ORL direct,A | OR accumulator to direct byte | 42 | 2 | 3 |
| ORL direct,#data | OR immediate data to direct byte | 43 | 3 | 4 |
| XRL A,Rn | Exclusive OR register to accumulator | 68-6F | 1 | 1 |
| XRL A,direct | Exclusive OR direct byte to accumulator | 65 | 2 | 2 |
| XRL A,@Ri | Exclusive OR indirect RAM to accumulator | 66-67 | 1 | 2 |
| XRL A,#data | Exclusive OR immediate data to accumulator | 64 | 2 | 2 |
| XRL direct,A | Exclusive OR accumulator to direct byte | 62 | 2 | 3 |
| XRL direct,#data | Exclusive OR immediate data to direct byte | 63 | 3 | 4 |
| CLR A | Clear accumulator | E4 | 1 | 1 |
| CPL A | Complement accumulator | F4 | 1 | 1 |
| RL A | Rotate accumulator left | 23 | 1 | 1 |
| RLC A | Rotate accumulator left through carry | 33 | 1 | 1 |
| RR A | Rotate accumulator right | 03 | 1 | 1 |
| RRC A | Rotate accumulator right through carry | 13 | 1 | 1 |
| SWAP A | Swap nibbles within the accumulator | C4 | 1 | 1 |

Table 2-3: Data transfer

| Mnemonic | Description | Code | Bytes | Cycles |
|---------------------|--|-------|-------|--------|
| MOV A,Rn | Move register to accumulator | E8-EF | 1 | 1 |
| MOV A,direct | Move direct byte to accumulator | E5 | 2 | 2 |
| MOV A,@Ri | Move indirect RAM to accumulator | E6-E7 | 1 | 2 |
| MOV A,#data | Move immediate data to accumulator | 74 | 2 | 2 |
| MOV Rn,A | Move accumulator to register | F8-FF | 1 | 2 |
| MOV Rn,direct | Move direct byte to register | A8-AF | 2 | 4 |
| MOV Rn,#data | Move immediate data to register | 78-7F | 2 | 2 |
| MOV direct,A | Move accumulator to direct byte | F5 | 2 | 3 |
| MOV direct,Rn | Move register to direct byte | 88-8F | 2 | 3 |
| MOV direct1,direct2 | Move direct byte to direct byte | 85 | 3 | 4 |
| MOV direct,@Ri | Move indirect RAM to direct byte | 86-87 | 2 | 4 |
| MOV direct,#data | Move immediate data to direct byte | 75 | 3 | 3 |
| MOV @Ri,A | Move accumulator to indirect RAM | F6-F7 | 1 | 3 |
| MOV @Ri,direct | Move direct byte to indirect RAM | A6-A7 | 2 | 5 |
| MOV @Ri,#data | Move immediate data to indirect RAM | 76-77 | 2 | 3 |
| MOV DPTR,#data16 | Load data pointer with a 16-bit constant | 90 | 3 | 3 |
| MOVC A,@A+DPTR | Move code byte relative to DPTR to accumulator | 93 | 1 | 3 |
| MOVC A,@A+PC | Move code byte relative to PC to accumulator | 83 | 1 | 3 |
| PUSH direct | Push direct byte onto stack | C0 | 2 | 4 |
| POP direct | Pop direct byte from stack | D0 | 2 | 3 |
| XCH A,Rn | Exchange register with accumulator | C8-CF | 1 | 2 |
| XCH A,direct | Exchange direct byte with accumulator | C5 | 2 | 3 |
| XCH A,@Ri | Exchange indirect RAM with accumulator | C6-C7 | 1 | 3 |
| XCHD A,@Ri | Exchange low-order nibble indir. RAM with A | D6-D7 | 1 | 3 |

Table 2-4: Program branches

| Mnemonic | Description | Code | Bytes | Cycles |
|--------------------|--|-------|-------|--------|
| ACALL addr11 | Absolute subroutine call | xxx11 | 2 | 6 |
| LCALL addr16 | Long subroutine call | 12 | 3 | 6 |
| RET | from subroutine | 22 | 1 | 4 |
| RETI | from interrupt | 32 | 1 | 4 |
| AJMP addr11 | Absolute jump | xxx01 | 2 | 3 |
| LJMP addr16 | Long iump | 02 | 3 | 4 |
| SJMP rel | Short jump (relative addr.) | 80 | 2 | 3 |
| JMP @A+DPTR | Jump indirect relative to the DPTR | 73 | 1 | 2 |
| JZ rel | Jump if accumulator is zero | 60 | 2 | 3 |
| JNZ rel | Jump if accumulator is not zero | 70 | 2 | 3 |
| JC rel | Jump if carry flag is set | 40 | 2 | 3 |
| JNC | Jump if carry flag is not set | 50 | 2 | 3 |
| JB bit,rel | Jump if direct bit is set | 20 | 3 | 4 |
| JNB bit,rel | Jump if direct bit is not set | 30 | 3 | 4 |
| JBC bit,direct rel | Jump if direct bit is set and clear bit | 10 | 3 | 4 |
| CJNE A,direct rel | Compare direct byte to A and jump if not equal | B5 | 3 | 4 |
| CJNE A,#data rel | Compare immediate to A and jump if not equal | B4 | 3 | 4 |
| CJNE Rn,#data rel | Compare immed. to reg. and jump if not equal | B8-BF | 3 | 4 |
| CJNE @Ri,#data rel | Compare immed. to ind. and jump if not equal | B6-B7 | 3 | 4 |
| DJNZ Rn,rel | Decrement register and jump if not zero | D8-DF | 2 | 3 |
| DJNZ direct,rel | Decrement direct byte and jump if not zero | D5 | 3 | 4 |
| NOP | No operation | 00 | 1 | 1 |

Table 2-5: Boolean manipulation

| Mnemonic | Description | Code | Bytes | Cycles |
|------------|---------------------------------------|------|-------|--------|
| CLR C | Clear carry flag | C3 | 1 | 1 |
| CLR bit | Clear direct bit | C2 | 2 | 3 |
| SETB C | Set carry flag | D3 | 1 | 1 |
| SETB bit | Set direct bit | D2 | 2 | 3 |
| CPL C | Complement carry flag | B3 | 1 | 1 |
| CPL bit | Complement direct bit | B2 | 2 | 3 |
| ANL C,bit | AND direct bit to carry flag | 82 | 2 | 2 |
| ANL C,/bit | AND complement of direct bit to carry | B0 | 2 | 2 |
| ORL C,bit | OR direct bit to carry flag | 72 | 2 | 2 |
| ORL C,/bit | OR complement of direct bit to carry | A0 | 2 | 2 |
| MOV C,bit | Move direct bit to carry flag | A2 | 2 | 2 |
| MOV bit,C | Move carry flag to direct bit | 92 | 2 | 3 |

3. Memory Structure

The SM39R4051 memory structure follows general 8052 structure. It is 4KB program memory.

3.1. Program Memory

The SM39R4051 has 4KB on-chip flash memory which can be used as general program memory or EEPROM, on which include up to 1K byte specific ISP service program memory space. The address range for the 4K byte is \$000 to \$FFF. The address range for the ISP service program is \$C00 to \$FFF. The ISP service program size can be partitioned as N blocks of 256 byte (N=0 to 4). When N=0 means no ISP service program space available, total 4K byte memory used as program memory. When N=1 means address \$F00 to \$FFF reserved for ISP service program. When N=2 means memory address \$E00 to \$FFF reserved for ISP service program...etc. Value N can be set and programmed into SM39R4051 by the writer or ICP. It can be used to record any data as EEPROM. The procedure of this EEPROM application function is described in the section 13 on internal ISP.

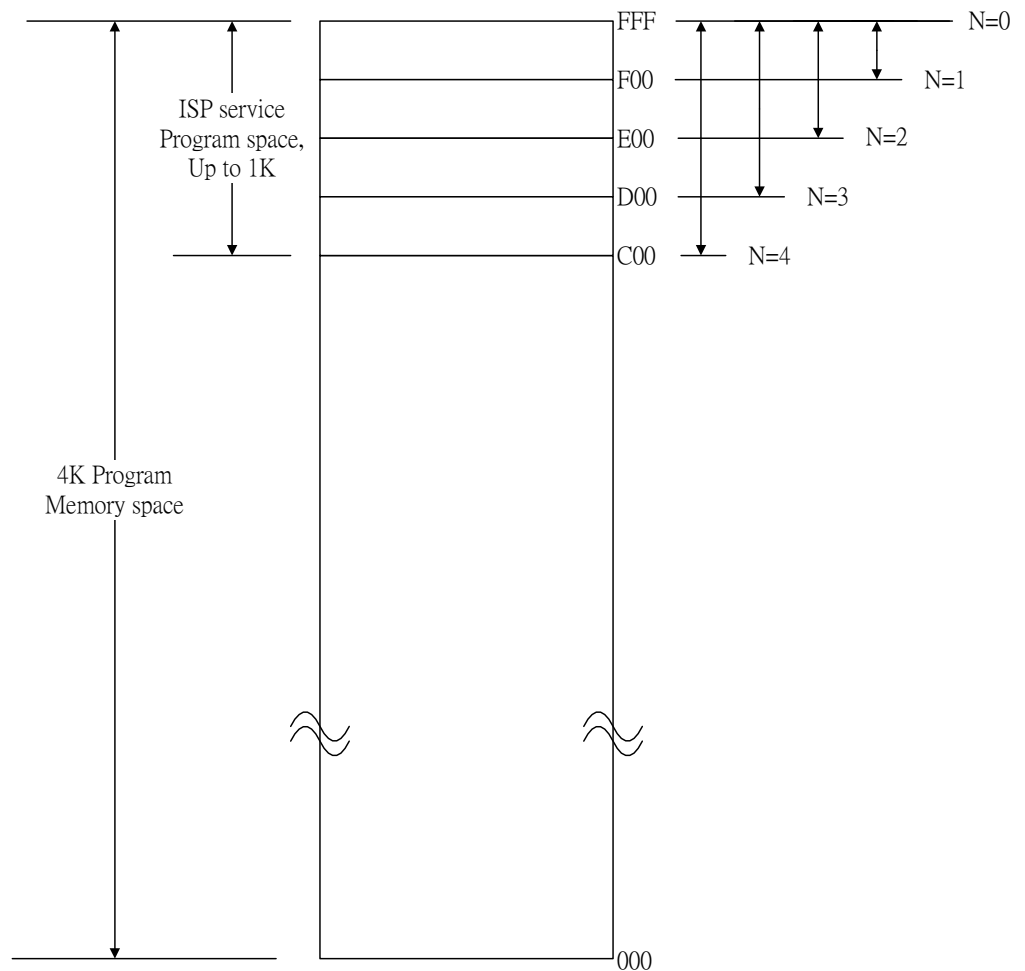


Fig. 3-1: SM39R4051 programmable Flash

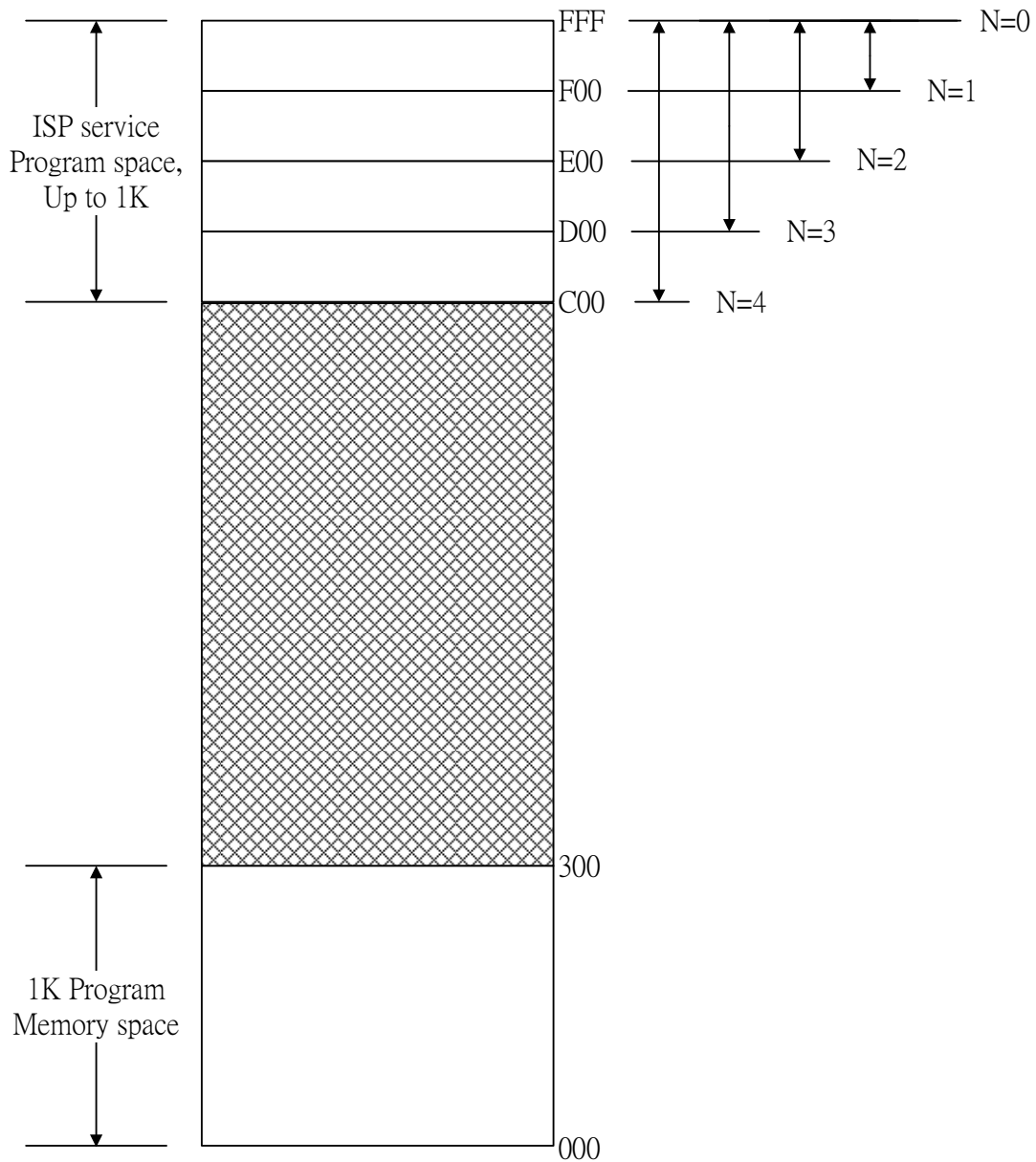


Fig. 3-2 : SM39R2051 programmable Flash

3.2. Data Memory

The SM39R4051 has 256Bytes on-chip SRAM; 256 Bytes of it are the same as general 8052 internal memory structure

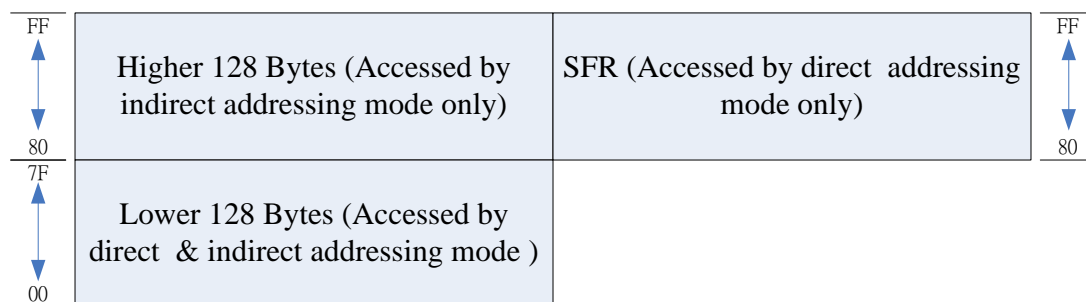


Fig. 3-3: RAM architecture

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3.2.1. Data memory - lower 128 byte (00h to 7Fh)

Data memory 00h to FFh is the same as 8052.
The address 00h to 7Fh can be accessed by direct and indirect addressing modes.
Address 00h to 1Fh is register area.
Address 20h to 2Fh is memory bit area.
Address 30h to 7Fh is for general memory area.

3.2.2. Data memory - higher 128 byte (80h to FFh)

The address 80h to FFh can be accessed by indirect addressing mode.
Address 80h to FFh is data area.

4. CPU Engine

The SM39R4051 engine is composed of four components:

- Control unit
- Arithmetic – logic unit
- Memory control unit
- RAM and SFR control unit

The SM39R4051 engine allows to fetch instruction from program memory and to execute using RAM or SFR. The following chapter describes the main engine register.

| Mnemonic | Description | Direct | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | RESET |
|-----------|----------------------------|--------|-----------|-------|-------|----------|-------|------------|-------|-------|-------|
| 8051 Core | | | | | | | | | | | |
| ACC | Accumulator | E0h | ACC.7 | ACC.6 | ACC.5 | ACC.4 | ACC.3 | ACC.2 | ACC.1 | ACC.0 | 00H |
| B | B register | F0h | B.7 | B.6 | B.5 | B.4 | B.3 | B.2 | B.1 | B.0 | 00H |
| PSW | Program status word | D0h | CY | AC | F0 | RS[1:0] | | OV | PSW.1 | P | 00H |
| SP | Stack Pointer | 81h | SP[7:0] | | | | | | | | 07H |
| DPL | Data pointer low 0 | 82h | DPL[7:0] | | | | | | | | 00H |
| DPH | Data pointer high 0 | 83h | DPH[7:0] | | | | | | | | 00H |
| DPL1 | Data pointer low 0 | 84h | DPL1[7:0] | | | | | | | | 00H |
| DPH1 | Data pointer high 0 | 85h | DPH1[7:0] | | | | | | | | 00H |
| AUX | Auxiliary register | 91h | BRGS | - | - | PTS[1:0] | | PINTS[1:0] | | DPS | 00H |
| IFCON | Interface control register | 8Fh | - | CDPR | - | - | - | - | - | ISPE | 00H |

4.1. Accumulator

ACC is the Accumulator register. Most instructions use the accumulator to store the operand.

| Mnemonic: ACC | | | | | | | | Address: E0h | |
|---------------|-------|-------|-------|-------|-------|-------|-------|--------------|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset | |
| ACC.7 | ACC.6 | ACC.5 | ACC.4 | ACC.3 | ACC.2 | ACC.1 | ACC.0 | 00h | |

ACC[7:0]: The A (or ACC) register is the standard 8052 accumulator.

4.2. B Register

The B register is used during multiply and divide instructions. It can also be used as a scratch pad register to store temporary data.

| Mnemonic: B | | | | | | | | Address: F0h | |
|-------------|-----|-----|-----|-----|-----|-----|-----|--------------|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset | |
| B.7 | B.6 | B.5 | B.4 | B.3 | B.2 | B.1 | B.0 | 00h | |

B[7:0]: The B register is the standard 8052 register that serves as a second accumulator.

4.3. Program Status Word

| | | | | | | | | |
|----------------------|----|----|----------|---|----|----|---------------------|-------|
| Mnemonic: PSW | | | | | | | Address: D0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| CY | AC | F0 | RS [1:0] | | OV | F1 | P | 00h |

CY: Carry flag.

AC: Auxiliary Carry flag for BCD operations.

F0: General purpose Flag 0 available for user.

RS[1:0]: Register bank select, used to select working register bank.

| RS[1:0] | Bank Selected | Location |
|---------|---------------|-----------|
| 00 | Bank 0 | 00h – 07h |
| 01 | Bank 1 | 08h – 0Fh |
| 10 | Bank 2 | 10h – 17h |
| 11 | Bank 3 | 18h – 1Fh |

OV: Overflow flag.

F1: General purpose Flag 1 available for user.

P: Parity flag, affected by hardware to indicate odd/even number of “one” bits in the Accumulator, i.e. even parity.

4.4. Stack Pointer

The stack pointer is a 1-byte register initialized to 07h after reset. This register is incremented before PUSH and CALL instructions, causing the stack to start from location 08h.

| | | | | | | | | |
|---------------------|---|---|---|---|---|---|---------------------|-------|
| Mnemonic: SP | | | | | | | Address: 81h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| SP [7:0] | | | | | | | | 07h |

SP[7:0]: The Stack Pointer stores the scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

4.5. Data Pointer

The data pointer (DPTR) is 2-bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2-byte register (e.g. MOV DPTR, #data16) or as two separate registers (e.g. MOV DPL, #data8). It is generally used to access the external code or data space (e.g. MOVC A, @A+DPTR, @DPTR respectively).

| | | | | | | | | |
|----------------------|---|---|---|---|---|---|---------------------|-------|
| Mnemonic: DPL | | | | | | | Address: 82h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| DPL [7:0] | | | | | | | | 00h |

DPL[7:0]: Data pointer Low 0

| | | | | | | | | |
|----------------------|---|---|---|---|---|---|---------------------|-------|
| Mnemonic: DPH | | | | | | | Address: 83h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| DPH [7:0] | | | | | | | | 00h |

DPH [7:0]: Data pointer High 0

4.6. Data Pointer 1

The Dual Data Pointer accelerates the moves of data block. The standard DPTR is a 16-bit register that is used to address external memory or peripherals. In the SM39R4051 core the standard data pointer is called DPTR, the second data pointer is called DPTR1. The data pointer select bit chooses the active pointer. The data pointer select bit is located in LSB of AUX register (DPS).

The user switches between pointers by toggling the LSB of AUX register. All DPTR-related instructions use the currently selected DPTR for any activity.

| Mnemonic: DPL1 | | | | | | | Address: 84h | |
|----------------|---|---|---|---|---|---|--------------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| DPL1 [7:0] | | | | | | | | 00h |

DPL1[7:0]: Data pointer Low 1

| Mnemonic: DPH1 | | | | | | | Address: 85h | |
|----------------|---|---|---|---|---|---|--------------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| DPH1 [7:0] | | | | | | | | 00h |

DPH1[7:0]: Data pointer High 1

| Mnemonic: AUX | | | | | | | Address: 91h | |
|---------------|---|---|----------|---|------------|---|--------------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| BRGS | - | - | PTS[1:0] | | PINTS[1:0] | | DPS | 00H |

DPS: Data Pointer selects register.
DPS = 1 is selected DPTR1.

4.7. Interface control register

| Mnemonic: IFCON | | | | | | | Address: 8Fh | |
|-----------------|------|---|---|---|---|---|--------------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| - | CDPR | - | - | - | - | - | ISPE | 00H |

CDPR: code protect (Read Only)
ISPE: ISP function enable bit
ISPE = 1, enable ISP function
ISPE = 0, disable ISP function

5. GPIO

The SM39R4051 has three I/O ports: Port 1, Port 3 and Port 4. Ports 1, 3 are 8-bit ports and Port 4 is a 2-bit port. These are: quasi-bidirectional (standard 8051 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin. All I/O port pins on the SM39R4051 may be configured by software to one of four types on a pin-by-pin basis, shown as below:

| Mnemonic | Description | Direct | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | RESET | |
|----------------------------|----------------------|--------|-------|-------|-------|-------|-----------|-------|-------|-------|-----------|-----|
| I/O port function register | | | | | | | | | | | | |
| P1M0 | Port 1 output mode 0 | D4h | | | | | P1M0[7:0] | | | | 00H | |
| P1M1 | Port 1 output mode 1 | D5h | | | | | P1M1[7:0] | | | | 00H | |
| P3M0 | Port 3 output mode 0 | DAh | | | | | P3M0[7:0] | | | | 00H | |
| P3M1 | Port 3 output mode 1 | DBh | | | | | P3M1[7:0] | | | | 00H | |
| P4M0 | Port 4 output mode 0 | DCh | | | | | | | | | P4M0[1:0] | 00H |
| P4M1 | Port 4 output mode 1 | DDh | | | | | | | | | P4M1[1:0] | 00H |
| P1WE | Port 3 output enable | A3h | | | | | P3WE[7:0] | | | | FFH | |
| P3WE | Port 1 output enable | A4h | | | | | P1WE[7:0] | | | | FFH | |

| PxM1.y | PxM0.y | Port output mode |
|--------|--------|--|
| 0 | 0 | Quasi-bidirectional (standard 8051 port outputs) (pull-up) |
| 0 | 1 | Push-pull |
| 1 | 0 | Input only (high-impedance) |
| 1 | 1 | Open drain |

The RESET Pin Can Be configured as I/O port P3.6 , when user use on-chip hardware RESET mechanism .

The XTAL2 and XTAL1 can be configured as I/O port by ICP or in ISP mode , when user use external OSC or on-chip RC Oscillator is set to main system clock source .

Mnemonic: P1WE **Address: A3h**

| | | | | | | | | |
|------|------|------|------|------|------|------|------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| P1.7 | P1.6 | P1.5 | P1.4 | P1.3 | P1.2 | P1.1 | P1.0 | FFH |

Mnemonic: P3WE **Address: A4h**

| | | | | | | | | |
|------|------|------|------|------|------|------|------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| P3.7 | P3.6 | P3.5 | P3.4 | P3.3 | P3.2 | P3.1 | P3.0 | FFH |

For general-purpose applications, every pin can be assigned to either high or low independently as given below:

| Mnemonic | Description | Direct | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | RESET |
|----------|-------------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Ports | | | | | | | | | | | |
| Port 4 | Port 4 | E8h | - | - | - | - | - | - | P4.1 | P4.0 | FFh |
| Port 3 | Port 3 | B0h | P3.7 | P3.6 | P3.5 | P3.4 | P3.3 | P3.2 | P3.1 | P3.0 | FFh |
| Port 1 | Port 1 | 90h | P1.7 | P1.6 | P1.5 | P1.4 | P1.3 | P1.2 | P1.1 | P1.0 | FFh |

Mnemonic: P1 **Address: 90h**

| | | | | | | | | |
|------|------|------|------|------|------|------|------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| P1.7 | P1.6 | P1.5 | P1.4 | P1.3 | P1.2 | P1.1 | P1.0 | FFh |

P1.7~ 0: Port1 [7] ~ Port1 [0]

Mnemonic: P3 **Address: B0h**

| | | | | | | | | |
|------|------|------|------|------|------|------|------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| P3.7 | P3.6 | P3.5 | P3.4 | P3.3 | P3.2 | P3.1 | P3.0 | FFh |

P3.7~ 0: Port3 [7] ~ Port3 [0]

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| Mnemonic: P4 | | | | | | Address: E8h | | |
|--------------|---|---|---|---|---|--------------|------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| - | - | - | - | - | - | P4.1 | P4.0 | FFh |

P4.1~ 0: Port4 [1] ~ Port4 [0]

6. Timer 0 and Timer 1

The SM39R4051 has two 16-bit timer/counter registers: Timer 0 and Timer 1. All can be configured for counter or timer operations.

In timer mode, the Timer 0 register or Timer 1 register is incremented every 12 machine cycles, which means that it counts up after every 12 periods of the clock signal.

In counter mode, the register is incremented when the falling edge is observed at the corresponding input pin T0 or T1. Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function registers (TMOD and TCON) are used to select the appropriate mode.

| Mnemonic | Description | Direct | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | RESET | |
|---------------|-----------------------|--------|-------|-------|-------|----------|-------|------------|-------|-------|-------|-----|
| Timer 0 and 1 | | | | | | | | | | | | |
| TL0 | Timer 0, low byte | 8Ah | | | | | | TL0[7:0] | | | | 00h |
| TH0 | Timer 0, high byte | 8Ch | | | | | | TH0[7:0] | | | | 00h |
| TL1 | Timer 1, low byte | 8Bh | | | | | | TL1[7:0] | | | | 00h |
| TH1 | Timer 1, high byte | 8Dh | | | | | | TH1[7:0] | | | | 00h |
| TMOD | Timer Mode Control | 89h | GATE | C/T | M1 | M0 | GATE | C/T | M1 | M0 | 00h | |
| TCON | Timer/Counter Control | 88h | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00h | |
| AUX | Auxiliary register | 91h | BRGS | - | - | PTS[1:0] | | PINTS[1:0] | | DPS | 00h | |

6.1. Timer/counter mode control register (TMOD)

Mnemonic: TMOD **Address: 89h**

| | | | | | | | | |
|---------|-----|----|----|---------|-----|----|----|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| GATE | C/T | M1 | M0 | GATE | C/T | M1 | M0 | 00h |
| Timer 1 | | | | Timer 0 | | | | |

GATE: If set, enables external gate control (pin INT0 or INT1 for Counter 0 or 1, respectively). When INT0 or INT1 is high, and TRx bit is set (see TCON register), a counter is incremented every falling edge on T0 or T1 input pin

C/T: Selects Timer or Counter operation. When set to 1, a counter operation is performed, when cleared to 0, the corresponding register will function as a timer.

M[1:0]: Selects mode for Timer/Counter 0 or Timer/Counter 1.

| M1 | M0 | Mode | Function |
|----|----|-------|--|
| 0 | 0 | Mode0 | 13-bit counter/timer, with 5 lower bits in TL0 or TL1 register and 8 bits in TH0 or TH1 register (for Timer 0 and Timer 1, respectively). The 3 high order bits of TL0 and TL1 are hold at zero. |
| 0 | 1 | Mode1 | 16-bit counter/timer. |
| 1 | 0 | Mode2 | 8-bit auto-reload counter/timer. The reload value is kept in TH0 or TH1, while TL0 or TL1 is incremented every machine cycle. When TLx overflows, a value from THx is copied to TLx. |
| 1 | 1 | Mode3 | If Timer 1 M1 and M0 bits are set to 1, Timer 1 |

| | | | |
|--|--|--|---|
| | | | stops. If Timer 0 M1 and M0 bits are set to 1, Timer 0 acts as two independent 8 bit timers / counters. |
|--|--|--|---|

6.2. Timer/counter control register (TCON)

| | | | | | | | | |
|-----------------------|-----|-----|-----|-----|-----|-----|---------------------|-------|
| Mnemonic: TCON | | | | | | | Address: 88h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00h |

TF1: Timer 1 overflow flag set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.

TR1: Timer 1 Run control bit. If cleared, Timer 1 stops.

TF0: Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.

TR0: Timer 0 Run control bit. If cleared, Timer 0 stops.

IE1: Interrupt 1 edge flag. Set by hardware, when falling edge on external pin INT1 is observed. Cleared when interrupt is processed.

IT1: Interrupt 1 type control bit. Selects falling edge or low level on input pin to cause interrupt.

IE0: Interrupt 0 edge flag. Set by hardware, when falling edge on external pin INTO is observed. Cleared when interrupt is processed.

IT0: Interrupt 0 type control bit. Selects falling edge or low level on input pin to cause interrupt.

6.3. T0、T1 signal swapping :

The T0、T1 signal can be configured to other I/O ◦

| | | | | | | | | |
|----------------------|---|---|-----------|---|------------|---|---------------------|-------|
| Mnemonic: AUX | | | | | | | Address: 91h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| BRGS | - | - | PTS [1:0] | | PINTS[1:0] | | DPS | 00H |

| Package = 20 Pin | | |
|------------------|------|------|
| PTS [1:0] | T0 | T1 |
| 0x00 | P3.4 | P3.5 |
| 0x01 | P3.0 | P3.1 |
| 0x10 | P1.4 | P1.5 |
| 0x11 | P1.2 | P1.3 |

7. Serial interface 0

The serial buffer consists of two separate registers, a transmit buffer and a receive buffer.

Writing data to the Special Function Register S0BUF sets this data in serial output buffer and starts the transmission. Reading from the S0BUF reads data from the serial receive buffer. The serial port can simultaneously transmit and receive data. It can also buffer 1 byte at receive, which prevents the receive data from being lost if the CPU reads the first byte before transmission of the second byte is completed.

| Mnemonic | Description | Direct | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | RESET |
|--------------------|---|--------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------|
| Serial interface 0 | | | | | | | | | | | |
| PCON | Power control | 87H | SMOD | - | - | - | - | - | STOP | IDLE | 40H |
| AUX | Auxiliary register | 91h | BRGS | - | - | PTS[1:0] | | PINTS[1:0] | | DPS | 00H |
| S0CON | Serial Port 0 control register | 98H | SM0 | SM1 | SM20 | RENO | TB80 | RB80 | TI0 | RI0 | 00H |
| S0BUF | Serial Port 0 data buffer | 99H | S0BUF[7:0] | | | | | | | | 00H |
| S0RELL | Serial Port 0 reload register low byte | AAH | S0REL .7 | S0REL .6 | S0REL .5 | S0REL .4 | S0REL .3 | S0REL .2 | S0REL .1 | S0REL .0 | 00H |
| S0RELH | Serial Port 0 reload register high byte | BAH | - | | | | | | S0REL .9 | S0REL .8 | 00H |

Mnemonic: AUX

Address: 91h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
|------|---|---|----------|---|------------|---|-----|-------|
| BRGS | - | - | PTS[1:0] | | PINTS[1:0] | | DPS | 00H |

BRGS: BRGS = 0 –Baud rate generator use Timer 1 TH1 SFR.

BRGS = 1 –Baud rate generator use S0REL SFR.

Mnemonic: S0CON

Address: 98h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
|-----|-----|------|------|------|------|-----|-----|-------|
| SM0 | SM1 | SM20 | RENO | TB80 | RB80 | TI0 | RI0 | 00h |

SM0,SM1: Serial Port 0 mode selection.

| SM0 | SM1 | Mode |
|-----|-----|------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

The 4 modes in UART0, Mode 0 ~ 3, are explained later.

SM20: Enables multiprocessor communication feature

RENO: If set, enables serial reception. Cleared by software to disable reception.

TB80: The 9th transmitted data bit in modes 2 and 3. Set or cleared by the CPU depending on the function it performs such as parity check, multiprocessor communication etc.

RB80: In modes 2 and 3, it is the 9th data bit received. In mode 1, if SM20 is 0, RB80 is the stop bit. In mode 0, this bit is not used. Must be cleared by software.

TI0: Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.

RI0: Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

The Serial Interface 0 can operate in the following 4 modes:

Specifications subject to change without notice contact your sales representatives for the most recent information.

| SM0 | SM1 | Mode | Description | Board Rate |
|-----|-----|------|----------------|--------------------|
| 0 | 0 | 0 | Shift register | Fosc/12 |
| 0 | 1 | 1 | 8-bit UART | Variable |
| 1 | 0 | 2 | 9-bit UART | Fosc/32 or Fosc/64 |
| 1 | 1 | 3 | 9-bit UART | Variable |

Here Fosc is the crystal or oscillator frequency.

7.1. Mode 0

Pin RXD0 serves as input and output. TXD0 outputs the shift clock. 8 bits are transmitted with LSB first. The baud rate is fixed at 1/12 of the crystal frequency. Reception is initialized in Mode 0 by setting the flags in S0CON as follows: RI0 = 0 and RENO = 1. In other modes, a start bit when RENO = 1 starts receiving serial data.

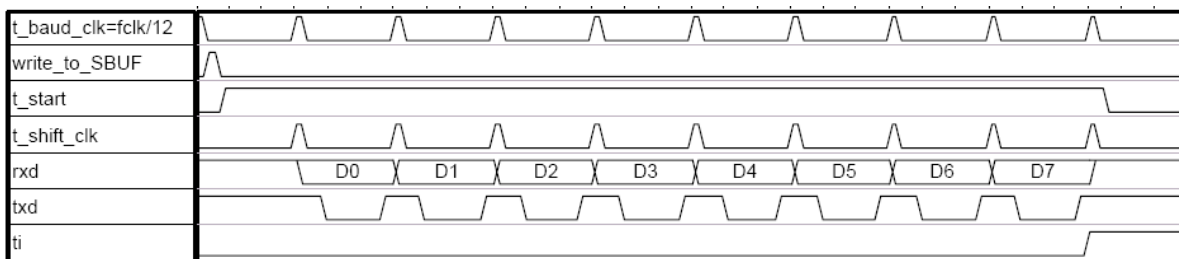


Fig. 7-1: Transmit mode 0 for Serial 0

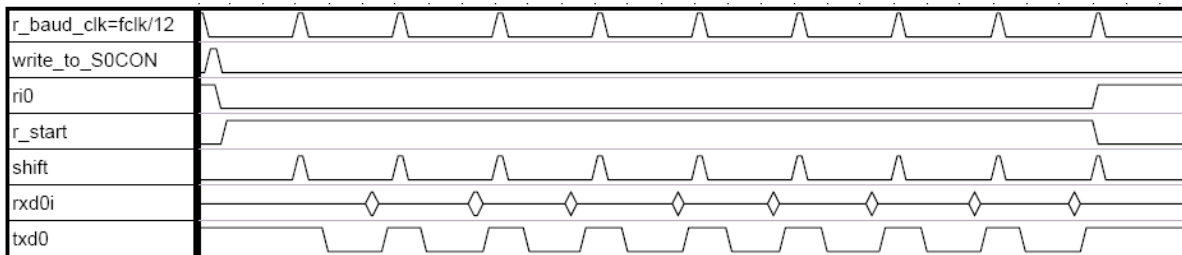


Fig. 7-2: Receive mode 0 for Serial 0

7.2. Mode 1

Pin RXD0 serves as input, and TXD0 serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading S0BUF, and stop bit sets the flag RB80 in the Special Function Register S0CON. In mode 1 either internal baud rate generator or timer 1 can be use to specify baud rate.



Fig. 7-3: Transmit mode 1 for Serial 0

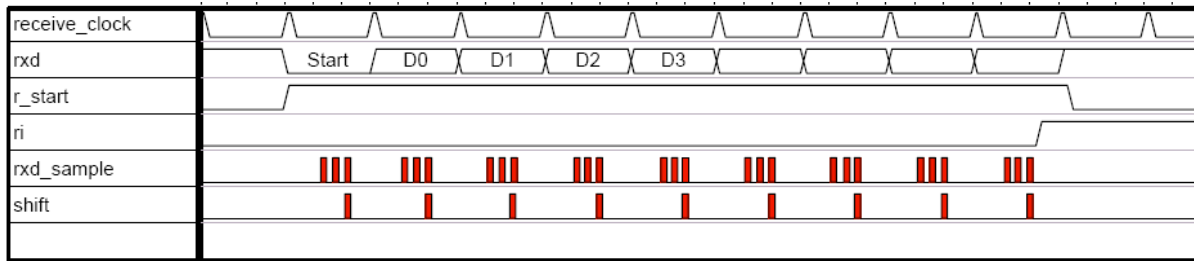


Fig. 7-4: Receive mode 1 for Serial 0

7.3. Mode 2

This mode is similar to Mode 1, with two differences. The baud rate is fixed at 1/32 (SMOD=1) or 1/64 (SMOD=0) of oscillator frequency and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB8 in S0CON is output as the 9th bit, and at receive, the 9th bit affects RB8 in Special Function Register S0CON.

7.4. Mode 3

The only difference between Mode 2 and Mode 3 is that in Mode 3 either internal baud rate generator or timer 1 can be used to specify baud rate.



Fig. 7-5: Transmit modes 2 and 3 for Serial 0

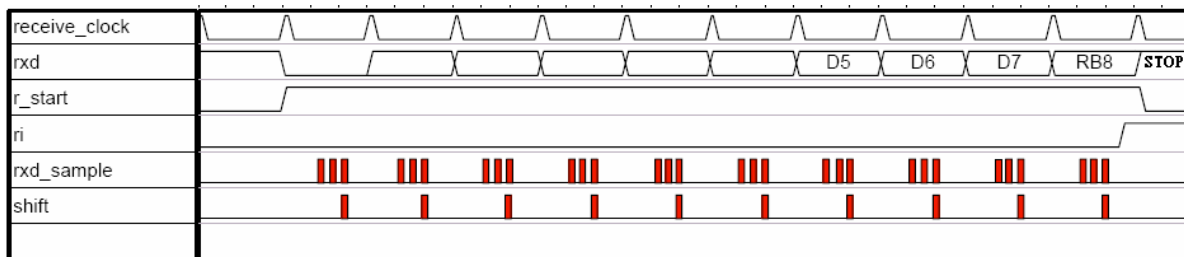


Fig. 7-6: Receive modes 2 and 3 for Serial 0

7.5. Multiprocessor communication of Serial Interface 0

The feature of receiving 9 bits in Modes 2 and 3 of Serial Interface 0 can be used for multiprocessor communication. In this case, the slave processors have bit SM20 in S0CON. When the master processor outputs slave's address, it sets the 9th bit to 1, causing a serial port receive interrupt in all the slaves. The slave processors compare the received byte with their network address. If there is a match, the addressed slave will clear SM20 and receive the rest of the message, while other slaves will leave SM20 bit unaffected and ignore this message. After addressing the slave, the host will output the rest of the message with the 9th bit set to 0, so no serial port receive interrupt will be generated in unselected slaves.

7.6. Baud rate generator

7.6.1. Serial interface 0 modes 1 and 3

(a) When BRGS = 0 (in SFR AUX):

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{\text{OSC}}}{32 \times 12 \times (256 - \text{TH1})}$$

(b) When BRGS = 1 (in SFR AUX):

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{\text{OSC}}}{64 \times (2^{10} - \text{S0REL})}$$

7.6.2. Clock source for baud rate

The on-chip RC-Oscillator frequency varies within $\pm 3\%$ after factory calibration. In case of application with higher clock precision requirement, external Crystal is usually recommended clock source.

8. Watchdog timer

The Watch Dog Timer (WDT) is an 8-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0, Timer1 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter. User should check WDTF bit of WDTC register whenever un-predicted reset happened. After an external reset the watchdog timer is disabled and all registers are set to zeros.

The watchdog timer has a free running on-chip RC oscillator (250KHz ±20%). The WDT will keep on running even after the system clock has been turned off (for example, in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the MCU to reset. The WDT can be enabled or disabled any time during the normal mode. Please refer the WDTE bit of WDTC register. The default WDT time-out period is approximately 16.38ms (WDTM [3:0] = 0100b).

The WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit3 ~ bit0 (WDTM [3:0]) of Watch Dog Timer Control Register (WDTC) should be set accordingly.

$$WDTCLK = \frac{250KHz}{2^{WDTM}}$$

$$\text{Watchdog reset time} = \frac{256}{WDTCLK}$$

Table 8.1 WDT time-out period

| WDTM [3:0] | Divider (250 KHz RC oscillator in) | Time period @ 250KHz |
|------------|---------------------------------------|----------------------|
| 0000 | 1 | 1.02ms |
| 0001 | 2 | 2.05ms |
| 0010 | 4 | 4.10ms |
| 0011 | 8 | 8.19ms |
| 0100 | 16 | 16.38ms (default) |
| 0101 | 32 | 32.77ms |
| 0110 | 64 | 65.54ms |
| 0111 | 128 | 131.07ms |
| 1000 | 256 | 262.14ms |
| 1001 | 512 | 524.29ms |
| 1010 | 1024 | 1.05s |
| 1011 | 2048 | 2.10s |
| 1100 | 4096 | 4.19s |
| 1101 | 8192 | 8.39s |
| 1110 | 16384 | 16.78s |
| 1111 | 32768 | 33.55s |

When MCU is reset, the MCU will be read WDTE control bit status. When WDTE bit is set to 1, the watchdog function will be disabled no matter what the WDTM bit status is. When WDTE bit is clear to 0, the watchdog function will be enabled if WDTM bit is set to 1 by program. User can to set WDTE on the writer or ISP.

The program can enable the WDT function by programming 1 to the WDTE bit premise that WDTE control bit is clear to 0. After WDTE set to 1, the 8 bit-counter starts to count with the selected time base source clock which set by WDTM [3:0]. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when MCU been reset, either hardware reset or WDT reset.

Once the watchdog is started it cannot be stopped. User can refreshed the watchdog timer to zero by writing 0x55 to

Watch Dog Timer refresh Key (WDTK) register. This will clear the content of the 8-bit counter and let the counter re-start to count from the beginning. The watchdog timer must be refreshed regularly to prevent reset request signal from becoming active.

When Watchdog timer is overflow, the WDTF flag will set to one and automatically reset MCU. The WDTF flag can be clear by software or external reset or power on reset.

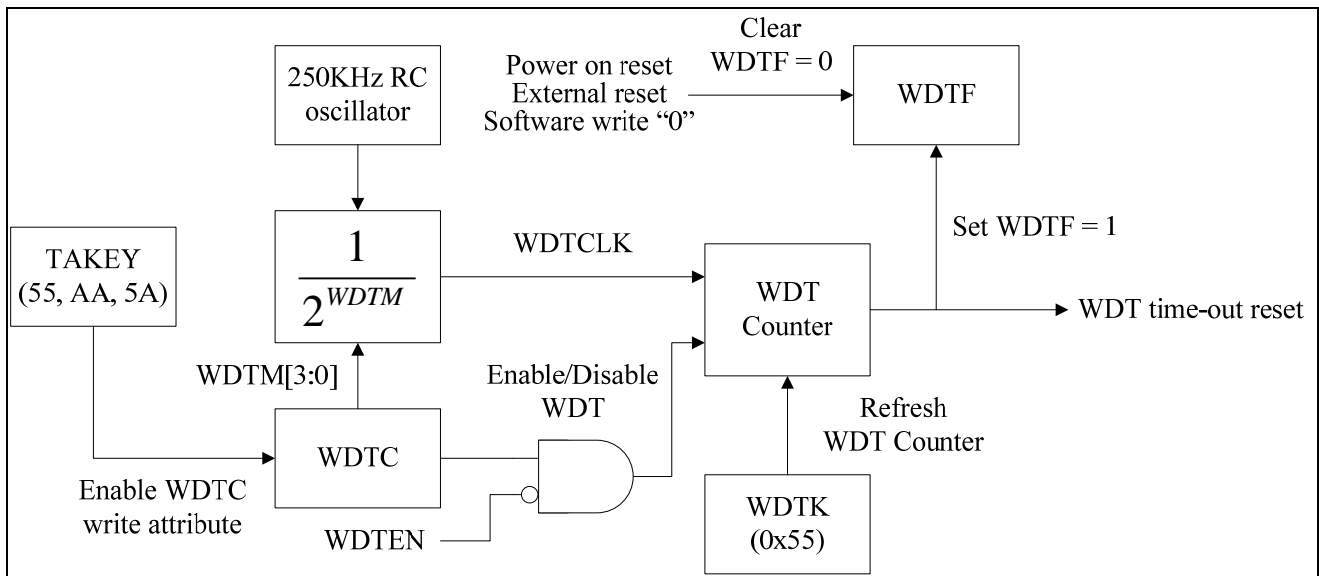


Fig. 8-1: Watchdog timer block diagram

| Mnemonic | Description | Direct | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | RESET |
|----------------|---------------------------------|--------|-------------|-------|-------|-------|------------|-------|-------|-------|-------|
| Watchdog Timer | | | | | | | | | | | |
| TAKEY | Time Access Key register | F7h | TAKEY [7:0] | | | | | | | | 00H |
| WDTC | Watchdog timer control register | B6h | WDTF | - | WDTE | - | WDTM [3:0] | | | 04H | |
| WDTK | Watchdog timer refresh key | B7h | WDTK[7:0] | | | | | | | | 00H |

| | | | | | | | | | |
|------------------------|---|---|---|---|---|---|---------------------|-------|--|
| Mnemonic: TAKEY | | | | | | | Address: F7h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset | |
| TAKEY [7:0] | | | | | | | | 00H | |

Watchdog timer control register (WDTC) is read-only by default; software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the WDTC write attribute. That is:

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah
```

| | | | | | | | | | |
|-----------------------|---|------|---|------------|---|---|---------------------|-------|--|
| Mnemonic: WDTC | | | | | | | Address: B6h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset | |
| WDTF | - | WDTE | - | WDTM [3:0] | | | 04H | | |

WDTF: Watchdog timer reset flag.

When MCU is reset by watchdog, WDTF flag will be set to one by hardware. This flag clear by software or external reset or power on reset.

WDTE: Control bit used to enable Watchdog timer.

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The WDTE bit can be used only if WDTEN is "0". If the WDTEN bit is "0", then WDT can be disabled / enabled by the WDTE bit.

0: Disable WDT.

1: Enable WDT.

The WDTE bit is not used if WDTEN is "1". That is, if the WDTEN bit is "1", WDT is always disabled no matter what the WDTE bit status is. The WDTE bit can be read and written.

WDTM [3:0]: WDT clock source divider bit. Please see table 8.1 to reference the WDT time-out period.

| Mnemonic: WDTK | | | | | | | Address: B7h | |
|----------------|---|---|---|---|---|---|--------------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| WDTK[7:0] | | | | | | | | 00h |

WDTK: Watchdog timer refresh key.

A programmer must write 0x55 into WDTK register, and then the watchdog timer will be cleared to zero.

For example, if enable WDT and select time-out reset period is 327.68ms.

First, programming the information block OP3 bit7 WDTEN to "0".

Secondly,

MOV TAKEY, #55h

MOV TAKEY, #AAh

MOV TAKEY, #5Ah

MOV WDTC, #28h

; enable WDTC write attribute.

; Set WDTM [3:0] = 1000b. Set WDTE =1 to enable WDT

; function.

.

.

.

MOV WDTK, #55h

; Clear WDT timer to 0.

9. Interrupt

The SM39R4051 provides 7 interrupt sources with four priority levels. Each source has its own request flag(s) located in a special function register. Each interrupt requested by the corresponding flag could individually be enabled or disabled by the enable bits in SFR's IEN0, and IEN1.

When the interrupt occurs, the engine will vector to the predetermined address as shown in Table 9.1. Once interrupt service has begun, it can be interrupted only by a higher priority interrupt. The interrupt service is terminated by a return from instruction RETI. When an RETI is performed, the processor will return to the instruction that would have been next when interrupt occurred.

When the interrupt condition occurs, the processor will also indicate this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled once per machine cycle, and then samples are polled by hardware. If the sample indicates a pending interrupt when the interrupt is enabled, then interrupt request flag is set. On the next instruction cycle the interrupt will be acknowledged by hardware forcing an LCALL to appropriate vector address.

Interrupt response will require a varying amount of time depending on the state of microcontroller when the interrupt occurs. If microcontroller is performing an interrupt service with equal or greater priority, the new interrupt will not be invoked. In other cases, the response time depends on current instruction. The fastest possible response to an interrupt is 7 machine cycles. This includes one machine cycle for detecting the interrupt and six cycles for perform the LCALL.

Table 9-1: Interrupt vectors

| Interrupt Request Flags | Interrupt Vector Address | Interrupt Number *(use Keil C Tool) |
|--------------------------------------|--------------------------|-------------------------------------|
| IE0 – External interrupt 0 | 0003h | 0 |
| TF0 – Timer 0 interrupt | 000Bh | 1 |
| IE1 – External interrupt 1 | 0013h | 2 |
| TF1 – Timer 1 interrupt | 001Bh | 3 |
| RI0/TI0 – Serial channel 0 interrupt | 0023h | 4 |
| LVIIIF – Low Voltage Interrupt | 0063h | 12 |
| IICIF – IIC interrupt | 006Bh | 13 |

*See Keil C about C51 User's Guide about Interrupt Function description

| Mnemonic | Description | Direct | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | RESET |
|-----------|-----------------------------|--------|-------|-------|-------|----------|-------|------------|-------|-------|-------|
| Interrupt | | | | | | | | | | | |
| AUX | Auxiliary register | 91h | BRGS | - | - | PTS[1:0] | | PINTS[1:0] | | DPS | 00H |
| IEN0 | Interrupt Enable 0 register | A8H | EA | - | - | ES0 | ET1 | EX1 | ET0 | EX0 | 00H |
| IEN1 | Interrupt Enable 1 register | B8H | - | - | IEIIC | IELVI | - | - | - | - | 00H |
| IRCON | Interrupt request register | C0H | - | - | IICIF | LVIIIF | - | - | - | - | 00H |
| IP0 | Interrupt priority level 0 | A9h | - | - | IP0.5 | IP0.4 | IP0.3 | IP0.2 | IP0.1 | IP0.0 | 00h |
| IP1 | Interrupt priority level 1 | B9h | - | - | IP1.5 | IP1.4 | IP1.3 | IP1.2 | IP1.1 | IP1.0 | 00h |

| Mnemonic: AUX | | | | | | | Address: 91h | |
|---------------|---|---|----------|---|------------|---|--------------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| BRGS | - | - | PTS[1:0] | | PINTS[1:0] | | DPS | 00H |

The INTO、INT1 signal can be configured to other I/O。

| Package = 20 Pin | | |
|------------------|------|------|
| PINTS [1:0] | INT0 | INT1 |
| 0x00 | P3.2 | P3.3 |
| 0x01 | P3.0 | P3.1 |
| 0x10 | P1.4 | P1.5 |
| 0x11 | P3.2 | P3.3 |

Interrupt Enable 0 register(IEN0)

| Mnemonic: IEN0 | | | | | | | Address: A8h | |
|----------------|---|---|-----|-----|-----|-----|--------------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| EA | - | - | ES0 | ET1 | EX1 | ET0 | EX0 | 00h |

EA: EA=0 – Disable all interrupt.
EA=1 – Enable all interrupt.

ES0: ES0=0 – Disable Serial channel 0 interrupt.
ES0=1 – Enable Serial channel 0 interrupt.

ET1: ET1=0 – Disable Timer 1 overflow interrupt.
ET1=1 – Enable Timer 1 overflow interrupt.

EX1: EX1=0 – Disable external interrupt 1.
EX1=1 – Enable external interrupt 1.

ET0: ET0=0 – Disable Timer 0 overflow interrupt.
ET0=1 – Enable Timer 0 overflow interrupt.

EX0: EX0=0 – Disable external interrupt 0.
EX0=1 – Enable external interrupt 0.

Interrupt Enable 1 register(IEN1)

| Mnemonic: IEN1 | | | | | | | Address: B8h | |
|----------------|---|-------|-------|---|---|---|--------------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| - | - | IEIIC | IELVI | - | - | - | - | 00h |

IEIIC: IIC interrupt enable.
IEIICS = 0 – Disable IIC interrupt.
IEIICS = 1 – Enable IIC interrupt.

IELVI: LVI interrupt enable.
IELVI = 0 – Disable LVI interrupt.
IELVI = 1 – Enable LVI interrupt.

Interrupt request register(IRCON)

| Mnemonic: IRCON | | | | | | | Address: C0h | |
|-----------------|---|-------|-------|---|---|---|--------------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| - | - | IICIF | LVIIF | - | - | - | - | 00H |

IICIF: IIC interrupt flag.
LVIIF: LVI interrupt flag.

9.1. Priority level structure

All interrupt sources are combined in groups:

Table 9-2: Priority level groups

| Groups- | |
|----------------------------|---------------|
| External interrupt 0 | |
| Timer 0 interrupt | - |
| External interrupt 1 | - |
| Timer 1 interrupt | - |
| Serial channel 0 interrupt | LVI interrupt |
| - | IIC interrupt |

Each group of interrupt sources can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register ip0 and one in ip1. If requests of the same priority level will be received simultaneously, an internal polling sequence determines which request is serviced first.

| Mnemonic: IP0 | | | | | | | | Address: A9h | |
|---------------|---|-------|-------|-------|-------|-------|-------|--------------|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset | |
| - | - | IP0.5 | IP0.4 | IP0.3 | IP0.2 | IP0.1 | IP0.0 | 00h | |

| Mnemonic: IP1 | | | | | | | | Address: B9h | |
|---------------|---|-------|-------|-------|-------|-------|-------|--------------|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset | |
| - | - | IP1.5 | IP1.4 | IP1.3 | IP1.2 | IP1.1 | IP1.0 | 00h | |

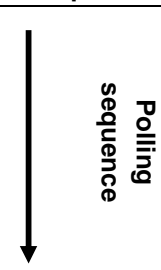
Table 9-3: Priority levels

| IP1.x | IP0.x | Priority Level |
|-------|-------|------------------|
| 0 | 0 | Level0 (lowest) |
| 0 | 1 | Level1 |
| 1 | 0 | Level2 |
| 1 | 1 | Level3 (highest) |

Table 9-4: Groups of priority

| Bit | Group | |
|--------------|----------------------------|---------------|
| IP1.0, IP0.0 | External interrupt 0 | - |
| IP1.1, IP0.1 | Timer 0 interrupt | - |
| IP1.2, IP0.2 | External interrupt 1 | - |
| IP1.3, IP0.3 | Timer 1 interrupt | - |
| IP1.4, IP0.4 | Serial channel 0 interrupt | LVI interrupt |
| IP1.5, IP0.5 | - | IIC interrupt |

Table 9-5: Polling sequence

| Interrupt source | Sequence |
|----------------------------|--|
| External interrupt 0 |  Polling sequence |
| Timer 0 interrupt | |
| External interrupt 1 | |
| Timer 1 interrupt | |
| Serial channel 0 interrupt | |
| LVI interrupt | |
| IIC interrupt | |

10. Power Management Unit

Power management unit serves two power management modes, IDLE and STOP, for the users to do power saving function.

| Mnemonic: PCON | | | | | | | Address: 87h | |
|----------------|---|---|---|---|---|------|--------------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| SMOD | - | - | - | - | - | STOP | IDLE | 40h |

STOP: Stop mode control bit. Setting this bit turning on the Stop Mode.

Stop bit is always read as 0

IDLE: Idle mode control bit. Setting this bit turning on the Idle Mode.

Idle bit is always read as 0

10.1. Idle mode

Setting the IDLE bit of PCON register invokes the IDLE mode. The IDLE mode leaves internal clocks and peripherals running. Power consumption drops because the CPU is not active. The CPU can exit the IDLE state with any interrupts or a reset.

10.2. Stop mode

Setting the STOP bit of PCON register invokes the STOP mode. All internal clocking in this mode is turn off. The CPU will exit this state only if interrupts asserted from external INT0/1 and LVI or hardware reset by WDT and LVR.

11. IIC function

The IIC module uses the SCL (clock) and the SDA (data) line to communicate with external IIC interface. Its speed can be selected to 400Kbps (maximum) by software setting the IICBR [2:0] control bit. The IIC module provided 2 interrupts (RXIF, TXIF). It will generate START, repeated START and STOP signals automatically in master mode and can detect START, repeated START and STOP signals in slave mode. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400pF.

The interrupt vector is 6Bh.

| Mnemonic | Description | Direct | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | RESET |
|--------------|----------------------------|--------|-------------|-------|-------|-------|-------|------------|-------|------------------|-------|
| IIC function | | | | | | | | | | | |
| IICCTL | IIC control register | F9h | IICEN | MSS | MAS | AB_EN | BF_EN | IICBR[2:0] | | | 04H |
| IICS | IIC status register | F8h | - | MPIF | LAIF | RXIF | TXIF | RXAK | TXAK | RW,B B | 00H |
| IICA1 | IIC Address 1 register | FAh | IICA1[7:1] | | | | | | | MATCH1 or RW1 | A0H |
| IICA2 | IIC Address 2 register | FBh | IICA2[7:1] | | | | | | | MATCH2 or RW2 | 60H |
| IICRWD | IIC Read/Write register | FCh | IICRWD[7:0] | | | | | | | | 00H |
| IICEBT | IIC Enable Bus Transaction | FDh | FU_EN | | - | | | | | | 00H |

Mnemonic: IICCTL

Address: F9h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
|-------|-----|-----|-------|-------|------------|---|---|-------|
| IICEN | MSS | MAS | AB_EN | BF_EN | IICBR[2:0] | | | 04h |

IICEN: Enable IIC module

IICEN = 1 is Enable

IICEN = 0 is Disable.

MSS: Master or slave mode select.

MSS = 1 is master mode.

MSS = 0 is slave mode.

*The software must set this bit before setting others register.

MAS: Master address select (master mode only)

MAS = 0 is to use IICA1.

MAS = 1 is to use IICA2.

AB_EN: Arbitration lost enable bit. (Master mode only)

If set AB_EN bit, the hardware will check arbitration lost. Once arbitration lost occurred, hardware will return to IDLE state. If this bit is cleared, hardware will not care arbitration lost condition. Set this bit when multi-master and slave connection. Clear this bit when single master to single slave.

BF_EN: Bus busy enable bit. (Master mode only)

If set BF_EN bit, hardware will not generate a start condition to bus until BF=0. Clear this bit will always generate a start condition to bus when MStart is set. Set this bit when multi-master and slave connection. Clear this bit when single master to single slave.

IICBR[2:0]: Baud rate selection (master mode only), where Fosc is the external crystal or oscillator frequency. The default is Fosc/512 for users' convenience.

| IICBR[2:0] | Baud rate |
|------------|-----------|
| 000 | Fosc/32 |
| 001 | Fosc/64 |
| 010 | Fosc/128 |

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| | |
|-----|-----------|
| 011 | Fosc/256 |
| 100 | Fosc/512 |
| 101 | Fosc/1024 |
| 110 | Fosc/2048 |
| 111 | Fosc/4096 |

| | | | | | | | | |
|-----------------------|------|------|------|------|------|------|---------------------|-------|
| Mnemonic: IICS | | | | | | | Address: F8H | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| - | MPIF | LAIF | RXIF | TXIF | RXAK | TxAk | RW | 00H |

- MPIF:** The Stop condition Interrupt Flag
The stop condition occurred and this bit will be set. Software need to clear this bit
- LAIF:** Arbitration lost bit. (Master mode only)
The Arbitration Interrupt Flag, the bus arbitration lost occurred and this bit will be set. Software need to clear this bit
- RxIF:** The data Receive Interrupt Flag (RXIF) is set after the IICRWD (IIC Read Write Data Buffer) is loaded with a newly receive data.
- TxIF:** The data Transmit Interrupt Flag (TXIF) is set when the data of the IICRWD (IIC Read Write Data Buffer) is downloaded to the shift register.
- RxAK:** The Acknowledge Status indicate bit. When clear, it means an acknowledge signal has been received after the complete 8 bits data transmit on the bus.
- TxAk:** The Acknowledge status transmit bit. When received complete 8 bits data, this bit will set (NoAck) or clear (Ack) and transmit to master to indicate the receive status.
- RW: Master Mode:**
Bus busy bit
If detect scl=0 or sda=0 or bus start, this bit will be set. If detect stop,this bit will be cleared. This bit can be cleared by software to return ready state.
- Slave Mode:**
The slave mode read (received) or wrote (transmit) on the IIC bus. When this bit is clear, the slave module received data on the IIC bus (SDA).(Slave mode only)

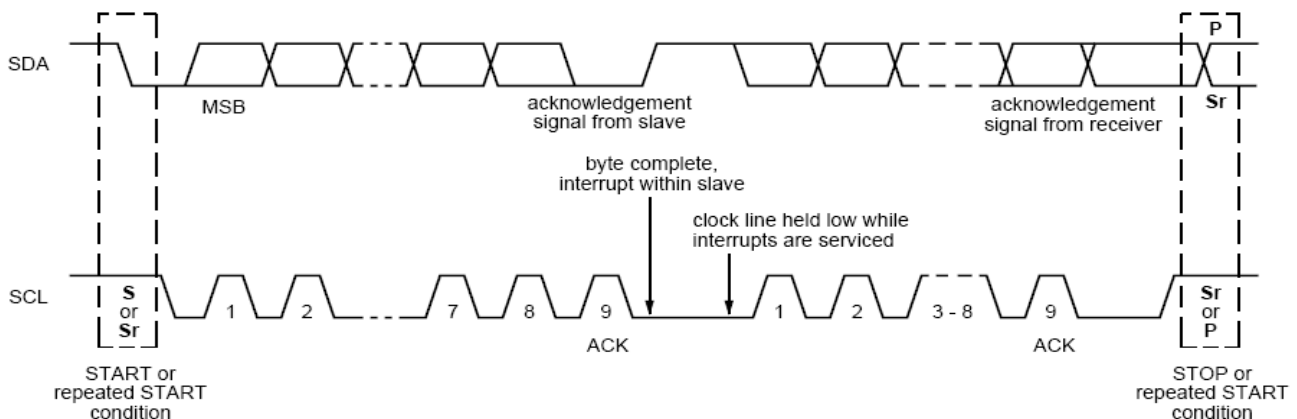


Fig. 11-1: Acknowledgement bit in the 9th bit of a byte transmission

| | | | | | | | | |
|------------------------|---|---|---|---|---|---|---------------------|-------|
| Mnemonic: IICA1 | | | | | | | Address: FAH | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| IICA1[7:1] | | | | | | | Match1 or RW1 | A0H |
| R/W | | | | | | | R or R/W | |

Slave mode:
IICA1[7:1]: IIC Address registers
This is the first 7-bit address for this slave module. It will be checked when an address (from

master) is received

Match1: When IICA1 matches with the received address from the master side, this bit will set to 1 by hardware. When IIC bus gets or send first data, this bit will clear automatically.

Master mode:

IICA1[7:1]: IIC Address registers

This 7-bit address indicates the slave with which it wants to communicate.

RW1: This bit will be sent out as RW of the slave side if the module has set the MStart or RStart bit. It appears at the 8th bit after the IIC address as shown in Fig. 14-2. It is used to tell the salve the direction of the following communication. If it is 1, the module is in master receive mode. If 0, the module is in master transmit mode.

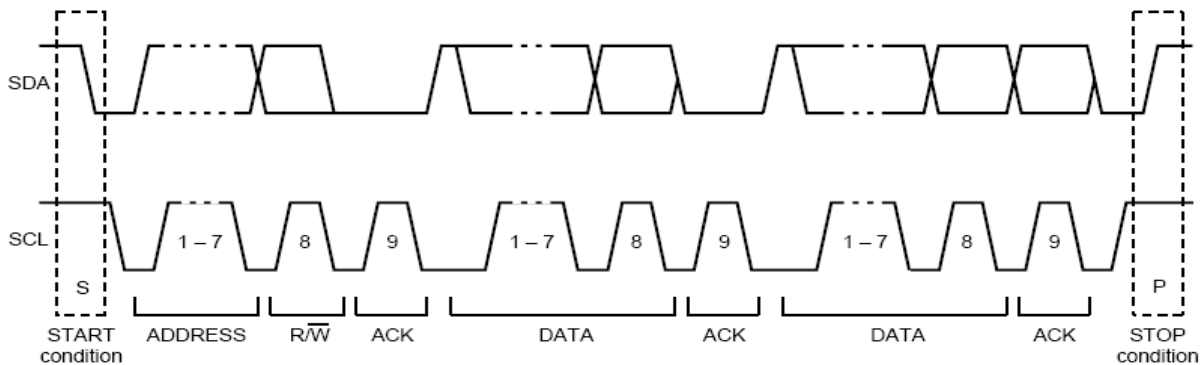


Fig. 11-2: RW bit in the 8th bit after IIC address

| Mnemonic: IICA2 | | | | | | | Address: FBh | |
|-----------------|---|---|---|---|---|---|---------------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| IICA2[7:1] | | | | | | | Match2 or RW2 | 60h |
| R/W | | | | | | | R or R/W | |

Slave mode:

IICA2[7:1]: IIC Address registers

This is the second 7-bit address for this slave module.

It will be checked when an address (from master) is received

Match2: When IICA2 matches with the received address from the master side, this bit will set to 1 by hardware. When IIC bus gets or send first data, this bit will clear automatically.

Master mode:

IICA2[7:1]: IIC Address registers

This 7-bit address indicates the slave with which it wants to communicate.

RW2: This bit will be sent out as RW of the slave side if the module has set the MStart or RStart bit. It is used to tell the salve the direction of the following communication. If it is 1, the module is in master receive mode. If 0, the module is in master transmit mode.

| Mnemonic: IICRWD | | | | | | | Address: FCh | |
|------------------|---|---|---|---|---|---|--------------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| IICRWD[7:0] | | | | | | | | 00h |

IICRWD[7:0]: IIC read write data buffer.

In receiving (read) mode, the received byte is stored here.

In transmitting mode, the byte to be shifted out through SDA stays here.

| Mnemonic: IICEBT | | | | | | | Address: FDH | |
|------------------|---|---|---|---|---|---|--------------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| FU_EN | - | - | - | - | - | - | - | 00H |

Master Mode :

- 00: reserved
- 01: IIC bus module will enable read/write data transfer on SDA and SCL.
- 10: IIC bus module generate a start condition on the SDA/SCL, then send out address which is stored in the IICA1/IICA2(selected by MAS control bit)
- 11: IIC bus module generate a stop condition on the SDA/SCL.

Slave mode:

- 01: FU_EN[7:6] should be set as 01 only. The other value is inhibited.
- Notice:
1. FU_EN[7:6] should be set as 01 before read/write data transfer for bus release; otherwise, SCL will be locked(pull low).
 2. FU_EN[7:6] should be set as 01 after read/write data transfer for receiving a stop condition from bus master.
 3. In transmit data mode(slave mode), the output data should be filled into IICRWD before setting FU_EN[7:6] as 01.
 4. FU_EN[7:6] will be auto-clear by hardware, so setting FU_EN[7:6] repeatedly is necessary.

12. LVI – Low Voltage Interrupt

The interrupt vector 63h.

| | | | | | | | | |
|---------------|--------|-------|-------|---|---|-------|--------------|-------|
| Mnemonic: LVC | | | | | | | Address: E6h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| LVI_EN | LVI_VS | LVRXE | LVSIF | - | - | EPSIF | - | 20H |

LVI_EN: Low voltage interrupt function enable bit.

0: disable low voltage detect function.

1: enable low voltage detect function.

LVI_VS: Low Voltage Interrupt level Selection

0 :The level of voltage is set at Low-level

1 :The level of voltage is set at Hi-Level

LVRXE: External low voltage reset function enable bit.

0: disable external low voltage reset function.

1: enable external low voltage reset function.

LVSIF Low Voltage Status Flag

1:the VDD voltage under LVI voltage

0:the VDD voltage above LVI voltage

EPSIF MCU External Voltage Status Flag

1: means less than 3.8V(external power)

0: means more than 3.9V(external power)

Hi-level :

| Symbol | Parameter | Min | Typ | Max | Units |
|------------------|-------------------------------------|-----|-----|-----|-------|
| V _{LVI} | Low Voltage Interrupt Voltage Level | 3.4 | 3.7 | 4.0 | V |
| V _{LVR} | Low Voltage Reset Voltage Level | 3.2 | 3.5 | 3.8 | V |

Notes: The V_{LVI} always above V_{LVR} about 0.2V.

Low-level :

| Symbol | Parameter | Min | Typ | Max | Units |
|------------------|-------------------------------------|-----|-----|-----|-------|
| V _{LVI} | Low Voltage Interrupt Voltage Level | 2.1 | 2.3 | 2.5 | V |
| V _{LVR} | Low Voltage Reset Voltage Level | 1.9 | 2.1 | 2.3 | V |

Notes: The V_{LVI} always above V_{LVR} about 0.2V.

13. In-System Programming (Internal ISP)

The SM39R4051 can generate flash control signal by internal hardware circuit. Users utilize flash control register, flash address register and flash data register to perform the ISP function without removing the SM39R4051 from the system. The SM39R4051 provides internal flash control signals which can do flash program/chip erase/page erase/protect functions. User need to design and use any kind of interface which SM39R4051 can input data. User then utilize ISP service program to perform the flash program/chip erase/page erase/protect functions.

13.1. ISP service program

The ISP service program is a user developed firmware program which resides in the ISP service program space. After user developed the ISP service program, user then determine the size of the ISP service program. User need to program the ISP service program in the SM39R4051 for the ISP purpose.

The ISP service programs were developed by user so that it should includes any features which relates to the flash memory programming function as well as communication protocol between SM39R4051 and host device which output data to the SM39R4051. For example, if user utilize UART interface to receive/transmit data between SM39R4051 and host device, the ISP service program should include baud rate, checksum or parity check or any error-checking mechanism to avoid data transmission error.

The ISP service program can be initiated under SM39R4051 active or idle mode. It can not be initiated under power down mode.

13.2. Lock Bit (N)

The Lock Bit N has two functions: one is for service program size configuration and the other is to lock the ISP service program space from flash erase function.

The ISP service program space address range \$C00 to \$FFF. It can be divided as blocks of N*256 byte. (N=0 to 4). When N=0 means no ISP function, all of 4K byte flash memory can be used as program memory. When N=1 means ISP service program occupies 256 byte while the rest of 3.75K byte flash memory can be used as program memory. The maximum ISP service program allowed is 1K byte when N=4. Under such configuration, the usable program memory space is 3K byte.

After N determined, SM39R4051 will reserve the ISP service program space downward from the top of the program address \$FFF. The start address of the ISP service program located at \$0C00. Please see section 3.1 program memory diagram for this ISP service program space structure.

The lock bit N function is different from the flash protect function. The flash erase function can erase all of the flash memory except for the locked ISP service program space. If the flash not has been protected, the content of ISP service program still can be read. If the flash has been protected, the overall content of flash program memory space including ISP service program space can not be read.

Table 13.1 ISP code area.

| N | ISP service program address |
|---|-------------------------------|
| 0 | No ISP service program |
| 1 | 256 bytes (\$F00h ~ \$FFFh) |
| 2 | 512 bytes (\$E00h ~ \$FFFh) |
| 3 | 768 bytes (\$D00h ~ \$FFFh) |
| 4 | 1.0 K bytes (\$C00h ~ \$FFFh) |

ISP service program configurable in N*256 byte (N= 0 ~ 4)

13.3. Program the ISP Service Program

After Lock Bit N is set and ISP service program been programmed, the ISP service program memory will be protected (locked) automatically. The lock bit N has its own program/erase timing. It is different from the flash memory program/erase timing so the locked ISP service program can not be erased by flash erase function. If user needs to erase the locked ISP service program, he can do it by writer only. User can not change ISP service program when SM39R4051 was in system.

13.4. Initiate ISP Service Program

To initiate the ISP service program is to load the program counter (PC) with start address of ISP service program and execute it. There are four ways to do so:

- (1) Blank reset. Hardware reset with first flash address blank (\$0000=#FFH) will load the PC with start address of ISP service program. The hardware reset includes MAX810 (power on reset) and external pad reset. The hardware will issue a strobe window about 256us after hardware reset.
- (2) Execute jump instruction can load the start address of the ISP service program to PC.
- (3) Enter's ISP service program by hardware setting. User can force SM39R4051 enter ISP service program by setting P1.5, "active low" during hardware reset period. The hardware reset includes MAX810 (power on reset) and external pad reset. The hardware will issue a strobe window about 256us after hardware reset. In application system design, user should take care of the setting of P1.5, at reset period to prevent SM39R4051 from entering ISP service program.
- (4) Enter's ISP service program by hardware setting, the P3.0 will be detected the two clock signals during hardware reset period. The hardware reset includes MAX810 (power on reset) and external pad reset. The hardware will issue a 256us strobe window to detect 2 clock signals after hardware reset.

During the strobe window, the hardware will detect the status of P1.5 and P3.0. If they meet one of above conditions, chip will switch to ISP mode automatically. After ISP service program executed, user need to reset the SM39R4051, either by hardware reset or by WDT, or jump to the address \$0000 to re-start the firmware program.

There are 6 kinds of entry mechanisms for user different applications. This entry method will select on the writer or ISP.

- (1) First Address Blank. i.e. \$0000 = 0xFF. And triggered by Internal reset signal.
- (2) First Address Blank. i.e. \$0000 = 0xFF. And triggered by PAD reset signal.
- (3) P1.5=0. And triggered by Internal reset signal.
- (4) P1.5=0. And triggered by PAD reset signal.
- (5) P3.0 input 2 clocks. And triggered by Internal reset signal.
- (6) P3.0 input 2 clocks. And triggered by PAD reset signal.

13.5. ISP register – TAKEY, IFCON, ISPFAH, ISPFAL, ISPFD and ISPFC

| Mnemonic | Description | Direct | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | RESET |
|--------------|-----------------------------------|--------|--------------|-------|-------|-------|--------------|-------|-------|-------|-------|
| ISP function | | | | | | | | | | | |
| TAKEY | Time Access Key register | F7h | TAKEY [7:0] | | | | | | | | 00H |
| IFCON | Interface Control register | 8Fh | - | CDPR | - | - | - | - | - | ISPE | 00H |
| ISPFAH | ISP Flash Address - High register | E1h | - | | | | ISPFAH [3:0] | | | | FFH |
| ISPFAL | ISP Flash Address - Low register | E2h | ISPFAL [7:0] | | | | | | | | FFH |
| ISPFD | ISP Flash Data register | E3h | ISPFD [7:0] | | | | | | | | FFH |

| | | | | | | | | | | | | | | | | | | | | |
|-------|-------|-------|---|------|------|------|------|-----|----------------------------|-------|-------|-------|---|------|------|------|------|-----|----------------------------|-----|
| ISPF0 | ISPF1 | ISPF2 | - | EMF4 | EMF3 | EMF2 | EMF1 | E4h | ISP Flash Control register | ISPF0 | ISPF1 | ISPF2 | - | EMF4 | EMF3 | EMF2 | EMF1 | E4h | ISP Flash Control register | 00H |
|-------|-------|-------|---|------|------|------|------|-----|----------------------------|-------|-------|-------|---|------|------|------|------|-----|----------------------------|-----|

Mnemonic: TAKEY

Address: F7H

| | | | | | | | | |
|-------------|---|---|---|---|---|---|---|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| TAKEY [7:0] | | | | | | | | 00H |

ISP enable bit (ISPE) is read-only by default, software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the ISPE bit write attribute. That is:

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah
```

Mnemonic: IFCON

Address: 8FH

| | | | | | | | | |
|---|------|---|---|---|---|---|------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| - | CDPR | - | - | - | - | - | ISPE | 00H |

The bit 0 (ISPE) of IFCON is ISP enable bit. User can enable overall SM39R4051 ISP function by setting ISPE bit to 1, to disable overall ISP function by set ISPE to 0. The function of ISPE behaves like a security key. User can disable overall ISP function to prevent software program be erased accidentally. ISP registers ISPF0, ISPF1, ISPF2 and ISPF3 are read-only by default. Software must be set ISPE bit to 1 to enable these 4 registers write attribute.

Mnemonic: ISPF0H

Address: E1H

| | | | | | | | | |
|---|---|---|---|---------|---------|---------|---------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| - | - | - | - | ISPF0H3 | ISPF0H2 | ISPF0H1 | ISPF0H0 | FFH |

ISPF0H [3:0]: Flash address-high for ISP function

Mnemonic: ISPF0L

Address: E2H

| | | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| ISPF0L7 | ISPF0L6 | ISPF0L5 | ISPF0L4 | ISPF0L3 | ISPF0L2 | ISPF0L1 | ISPF0L0 | FFH |

ISPF0L [7:0]: Flash address-Low for ISP function

The ISPF0H & ISPF0L provide the 12-bit flash memory address for ISP function. The flash memory address should not include the ISP service program space address. If the flash memory address indicated by ISPF0H & ISPF0L registers overlay with the ISP service program space address, the flash program/page erase of ISP function executed thereafter will have no effect.

Mnemonic: ISPF0D

Address: E3H

| | | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| ISPF0D7 | ISPF0D6 | ISPF0D5 | ISPF0D4 | ISPF0D3 | ISPF0D2 | ISPF0D1 | ISPF0D0 | FFH |

ISPF0D [7:0]: Flash data for ISP function.

The ISPF0D provide the 8-bit data register for ISP function.

Mnemonic: ISPF0C

Address: E4H

| | | | | | | | | |
|------|------|------|------|---|-----------|-----------|-----------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| EMF1 | EMF2 | EMF3 | EMF4 | - | ISPF0C[2] | ISPF0C[1] | ISPF0C[0] | 00H |

EMF1: Entry mechanism (1) flag, clear by reset. (Read only)
EMF2: Entry mechanism (2) flag, clear by reset. (Read only)
EMF3: Entry mechanism (3) flag, clear by reset. (Read only)

EMF4: Entry mechanism (4) flag, clear by reset. (Read only)
ISPF [2:0]: ISP function select bit.

| ISPF[2:0] | ISP function |
|-----------|--------------|
| 000 | Byte program |
| 001 | Chip protect |
| 010 | Page erase |
| 011 | Chip erase |
| 100 | Write option |
| 101 | Read option |
| 110 | Erase option |
| 111 | Finish Flag |

One page of flash memory is 256 byte

The Option function can access the XTAL1 and XTAL2 configured to I/O pins select(description in section 1.2) 、 Internal reset time select(description in section 1.4.1) 、 clock source select(description in section 1.5) 、 Reset configured to I/O pins function select(description in section 5) 、 WDTEN control bit(description in section 8) 、 or ISP entry mechanisms select(description in section 13) 。
When chip protected or no ISP service, option can only read.

The choice ISP function will start to execute once the software write data to ISPFC register.

To perform byte program/page erases ISP function, user need to specify flash address at first. When performing page erase function, SM39R4051 will erase entire page which flash address indicated by ISPF AH & ISPF AL registers located within the page.

e.g. flash address: \$YMN

page erase function will erase from \$Y00 to \$YFF

To perform the chip erase ISP function, SM39R4051 will erase all the flash program memory except the ISP service program space. To perform chip protect ISP function, the SM39R4051 flash memory content will be read #00H.

e.g. ISP service program to do the byte program - to program #22H to the address \$0105H

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah           ; enable ISPE write attribute
MOV IFCON, #01H          ; enable SM39R4051 ISP function
MOV ISPF AH, #01H        ; set flash address-high, 01H
MOV ISPF AL, #05H        ; set flash address-low, 05H
MOV ISPF D, #22H         ; set flash data to be programmed, data = 22H
MOV ISPF C, #00H         ; start to program #22H to the flash address $0105H
```

Operating Conditions

| Symbol | Description | Min. | Typ. | Max. | Unit. | Remarks |
|-----------------|-----------------------|------|------|------|-------|--------------------------------|
| TA | Operating temperature | -40 | 25 | 85 | °C | Ambient temperature under bias |
| V _{CC} | Supply voltage | 2.7 | | 5.5 | V | 23MHz(Max) |
| V _{CC} | Supply voltage | 3.0 | | 5.5 | V | 25MHz(Max) |

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0V

| Symbol | Parameter | Valid | Min | Max | Units | Conditions |
|--------|---|------------|--------------------|-----------------------|-------|--|
| VIL1 | Input Low-voltage | Port 1,3,4 | -0.5 | 0.8 | V | V _{CC} =5V |
| VIL2 | Input Low-voltage | RES, XTAL1 | 0 | 0.8 | V | |
| VIH1 | Input High-voltage | Port 1,3,4 | 2.0 | V _{CC} + 0.5 | V | |
| VIH2 | Input High-voltage | RES, XTAL1 | 70%V _{CC} | V _{CC} + 0.5 | V | |
| VOL | Output Low-voltage | Port 1,3,4 | | 0.4 | V | IOL=5.0mA V _{CC} =5V |
| VOH1 | Output High-voltage using Strong Pull-up ⁽¹⁾ | Port 1,3,4 | 2.4 | | V | IOH= -16mA |
| VOH2 | Output High-voltage using Weak Pull-up ⁽²⁾ | Port 1,3,4 | 2.4 | | V | IOH= -280uA |
| IIL | Logic 0 Input Current | Port 1,3,4 | | -75 | uA | Vin= 0.45V |
| ITL | Logical Transition Current | Port 1,3,4 | | -650 | uA | Vin= 2.0V |
| ILI | Input Leakage Current | Port 1,3,4 | | ±10 | uA | 0.45V<Vin<V _{CC} |
| RRST | Reset Pull-down Resistor | RES | 50 | 300 | kΩ | |
| CIO | Pin Capacitance | | | 10 | pF | Freq= 1MHz, Ta= 25°C |
| ICC | Power Supply Current | VDD | | 11 | mA | Active mode, 12MHz, V _{CC} =5V, 25 °C |
| | | | | 10 | mA | Idle mode, 12MHz, V _{CC} =5V, 25 °C |
| | | | | 3 | uA | Power down mode V _{CC} =5V, 25 °C |

- Notes:
1. Port in Push-Pull Output Mode
 2. Port in Quasi-Bidirectional Mode

$T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 3.0\text{V}$

| Symbol | Parameter | Valid | Min | Max | Units | Conditions |
|--------|---|------------|--------------|----------------|------------------|---|
| VIL1 | Input Low-voltage | Port 1,3,4 | -0.5 | 0.8 | V | $V_{CC}=3.0\text{V}$ |
| VIL2 | Input Low-voltage | RES, XTAL1 | 0 | 0.8 | V | |
| VIH1 | Input High-voltage | Port 1,3,4 | 2.0 | $V_{CC} + 0.5$ | V | |
| VIH2 | Input High-voltage | RES, XTAL1 | $70\%V_{CC}$ | $V_{CC} + 0.5$ | V | |
| VOL | Output Low-voltage | Port 1,3,4 | | 0.4 | V | $I_{OL}=3.0\text{mA}$ $V_{CC}=3.0\text{V}$ |
| VOH1 | Output High-voltage using Strong Pull-up ⁽¹⁾ | Port 1,3,4 | 2.4 | | V | $I_{OH} = -3.2\text{mA}$ |
| VOH2 | Output High-voltage using Weak Pull-up ⁽²⁾ | Port 1,3,4 | 2.4 | | V | $I_{OH} = -55\mu\text{A}$ |
| IIL | Logic 0 Input Current | Port 1,3,4 | | -75 | μA | $V_{in} = 0.45\text{V}$ |
| ITL | Logical Transition Current | Port 1,3,4 | | -650 | μA | $V_{in} = 1.5\text{V}$ |
| ILI | Input Leakage Current | Port 1,3,4 | | ± 10 | μA | $0.45\text{V} < V_{in} < V_{CC}$ |
| RRST | Reset Pull-down Resistor | RES | 50 | 300 | $\text{k}\Omega$ | |
| CIO | Pin Capacitance | | | 10 | pF | Freq= 1MHz, $T_a = 25^{\circ}\text{C}$ |
| ICC | Power Supply Current | VDD | | 10 | mA | Active mode, 12MHz, $V_{CC}=3.0\text{V}$, 25°C |
| | | | | 9 | mA | Idle mode, 12MHz, $V_{CC}=3.0\text{V}$, 25°C |
| | | | | 2 | μA | Power down mode, $V_{CC}=3.0\text{V}$, 25°C |

Notes: 1. Port in Push-Pull Output Mode
2. Port in Quasi-Bidirectional Mode

Suggest circuit connect :

