CY62167G/CY62167GE MoBL®

16-Mbit (1 M words × 16 bit / 2 M words × 8 bit) Static RAM with Error-Correcting Code (ECC)

Features

- Ultra-low standby current
  - ❏ Typical standby current: 4.6 μA
  - ❏ Maximum standby current: 16 μA
- High speed: 45 ns / 55 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- 48-pin TSOP I package configurable as 1 M × 16 or 2 M × 8 SRAM
- Available in Pb-free 48-ball VFBGA and 48-pin TSOP I packages

Functional Description

CY62167G and CY62167GE are high-performance CMOS, low-power (MoBL®) SRAM devices with embedded ECC[1]. Both devices are offered in single and dual chip enable options and in multiple pin configurations. The CY62167GE device includes an ERR pin that signals a single-bit error-detection and correction event during a read cycle.

To access devices with a single chip enable input, assert the chip enable ($\overline{CE}$) input LOW. To access dual chip enable devices, assert both chip enable inputs – $\overline{CE}_1$ as LOW and CE_2 as HIGH.

To perform data writes, assert the Write Enable ($\overline{WE}$) input LOW, and provide the data and address on the device data pins (I/O$_0$ through I/O$_{15}$) and address pins (A$_0$ through A$_{19}$) respectively. The Byte High Enable ($\overline{BHE}$) and Byte Low Enable ($\overline{BLE}$) inputs control byte writes and write data on the corresponding I/O lines to the memory location specified. $\overline{BHE}$ controls I/O$_8$ through I/O$_{15}$ and $\overline{BLE}$ controls I/O$_0$ through I/O$_7$.

To perform data reads, assert the Output Enable ($\overline{OE}$) input and provide the required address on the address lines. You can access read data on the I/O lines (I/O$_0$ through I/O$_{15}$). To perform byte accesses, assert the required byte enable signal ($\overline{BHE}$ or $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O$_0$ through I/O$_{15}$) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH for a single chip enable device and $\overline{CE}_1$ HIGH / CE_2 LOW for a dual chip enable device), or the control signals are de-asserted ($\overline{OE}$, $\overline{BLE}$, $\overline{BHE}$).

These devices have a unique Byte Power-down feature where, if both the Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) are disabled, the devices seamlessly switch to the standby mode irrespective of the state of the chip enables, thereby saving power.

On the CY62167GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High). See the Truth Table – CY62167G/CY62167GE on page 17 for a complete description of read and write modes.

The CY62167G and CY62167GE devices are available in a Pb-free 48-pin TSOP I package and 48-ball VFBGA packages. The logic block diagrams are on page 2.

The device in the 48-pin TSOP I package can also be configured to function as a 2 M words ×8 bit device. Refer to the Pin Configurations section for details.

Note
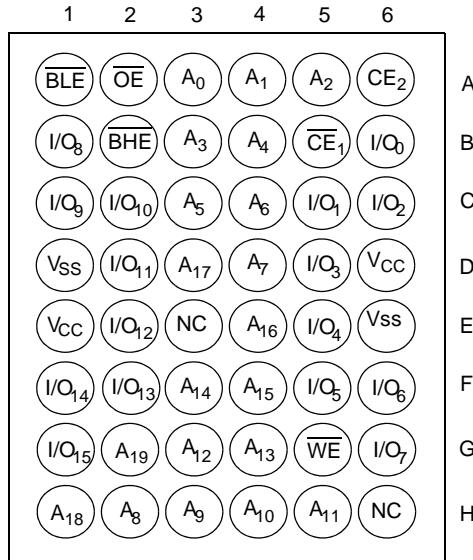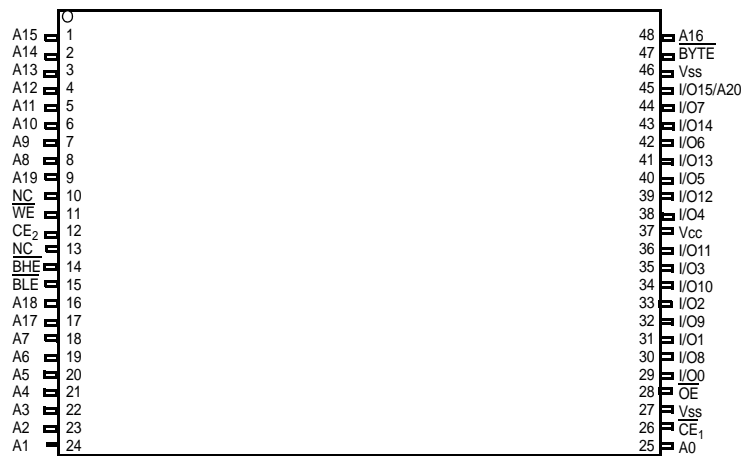1. This device does not support automatic write-back on error detection.

Logic Block Diagram – CY62167G

Logic Block Diagram – CY62167GE

Contents

Pin Configuration – CY62167G

Figure 1. 48-ball VFBGA pinout (Dual Chip Enable without ERR) – CY62167G [2]

Figure 2. 48-pin TSOP I pinout (Dual Chip Enable without ERR) – CY62167G [2, 3]

Notes
2. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
3. Tie the $\overline{\text{BYTE}}$ pin in the 48-pin TSOP I package to V_{CC} to use the device as a 1 M × 16 SRAM. The 48-pin TSOP I package can also be used as a 2 M ×8 SRAM by tying the BYTE signal to V_{SS}. In the 2 M ×8 configuration, pin 45 is the extra address line A20, while BHE, BLE, and I/O$_8$ to I/O$_{14}$ pins are not used and can be left floating.

Pin Configuration – CY62167GE

Figure 3. 48-ball VFBGA pinout (Single Chip Enable with ERR) – CY62167GE [4]

Figure 4. 48-ball VFBGA pinout (Dual Chip Enable with ERR) – CY62167GE [4]
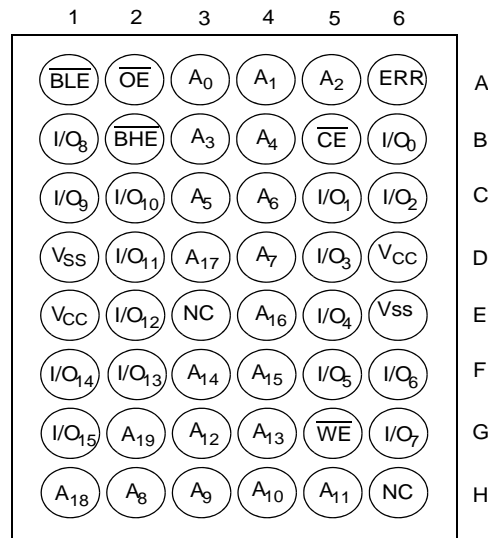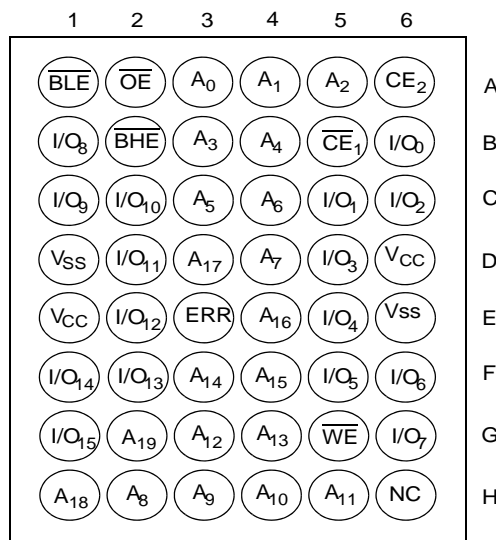

Note
4. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

Pin Configuration – CY62167GE (continued)

Figure 5. 48-pin TSOP I pinout (Dual Chip Enable with ERR) – CY62167GE [5, 6]

```
A15     1                                    48   A16
A14     2                                    47   BYTE
A13     3                                    46   Vss
A12     4                                    45   I/O15/A20
A11     5                                    44   I/O7
A10     6                                    43   I/O14
A9      7                                    42   I/O6
A8      8                                    41   I/O13
A19     9                                    40   I/O5
NC      10                                   39   I/O12
WE      11                                   38   I/O4
CE2     12                                   37   Vcc
ERR     13                                   36   I/O11
BHE     14                                   35   I/O3
BLE     15                                   34   I/O10
A18     16                                   33   I/O2
A17     17                                   32   I/O9
A7      18                                   31   I/O1
A6      19                                   30   I/O8
A5      20                                   29   I/O0
A4      21                                   28   OE
A3      22                                   27   Vss
A2      23                                   26   CE1
A1      24                                   25   A0
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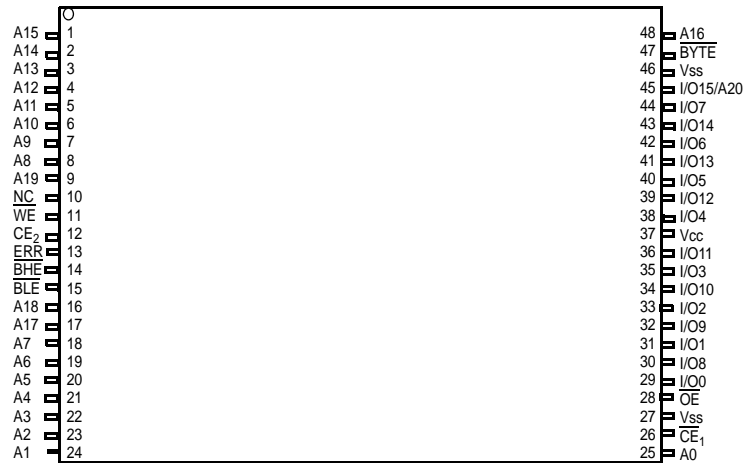
Notes
5. NC pins are not connected internally to the die and are typically used for address expansion to a higher density device. Refer to the respective datasheets for pin configuration.
6. Tie the $\overline{BYTE}$ pin in the 48-pin TSOP I package to V_{CC} to use the device as a 1 M ×16 SRAM. The 48-pin TSOP I package can also be used as a 2 M ×8 SRAM by tying the $\overline{BYTE}$ signal to V_{SS}. In the 2 M ×8 configuration, pin 45 is the extra address line A20, while the $\overline{BHE}$, $\overline{BLE}$, and I/O8 to I/O14 pins are not used and can be left floating.

Product Portfolio

Product	Features and Options (see the Pin Configurations section)	Range	V_CC Range (V)	Speed (ns)	Current Consumption			
					Operating I_CC, (mA) f = f_max		Standby, I_SB2 (μA)	
					Typ[7]	Max	Typ[7]	Max
CY62167G(E)18	Single or dual Chip Enables Optional ERR pin	Industrial	1.65 V–2.2 V	55	29	32	5.5	26
CY62167G(E)30			2.2 V–3.6 V	45	29	36	4.6	16
CY62167G(E)			4.5 V–5.5 V					

Note
7. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to + 150 °C

Ambient temperature with
power applied .... –55 °C to + 125 °C

Supply voltage to ground
potential ....–0.5 V to 6 V

DC voltage applied to outputs
in High Z state[8] .... –0.5 V to V_{CC} + 0.5 V

DC input voltage[8] .... –0.5 V to V_{CC} + 0.5 V

Output current into outputs (LOW) .... 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) .... >2001 V

Latch-up current .... >140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}[9]
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description		Test Conditions		45/55 ns			Unit
					Min	Typ[10]	Max	
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OH} = –0.1 mA		1.4	–	–	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –0.1 mA		2.0	–	–	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.2	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.4	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.2	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	
V_{IH}	Input HIGH voltage[8]	1.65 V to 2.2 V	–		1.4	–	V_{CC} + 0.2	V
		2.2 V to 2.7 V	–		2.0	–	V_{CC} + 0.3	
		2.7 V to 3.6 V	–		2.0	–	V_{CC} + 0.3	
		4.5 V to 5.5 V	–		2.2	–	V_{CC} + 0.5	
V_{IL}	Input LOW voltage[8]	1.65 V to 2.2 V	–		–0.2	–	0.4	V
		2.2 V to 2.7 V	–		–0.3	–	0.6	
		2.7 V to 3.6 V	–		–0.3	–	0.8	
		4.5 V to 5.5 V	–		–0.5	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–1.0	–	+1.0	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1.0	–	+1.0	µA
I_{CC}	V_{CC} operating supply current		V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels	f = 22.22 MHz (45 ns)	–	29.0	36.0	mA
				f = 18.18 MHz (55 ns)	–	29.0	32.0	mA
				f = 1 MHz	–	7.0	9.0	mA

Notes
8. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 2 ns.
9. Full device AC operation assumes a 100-µs ramp time from 0 to V_{CC} (min) and 200-µs wait time after V_{CC} stabilizes to its operational value.
10. Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested.

DC Electrical Characteristics (continued)

Over the operating range of –40 °C to 85 °C

Parameter	Description	Test Conditions		45/55 ns			Unit
				Min	Typ[10]	Max	
I_{SB1}[11]	Automatic power down current – CMOS inputs; V_{CC} = 2.2 to 3.6 V and 4.5 to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), $V_{CC} = V_{CC(max)}$		–	4.6	16.0	µA
	Automatic power down current – CMOS inputs V_{CC} = 1.65 to 2.2 V			–	5.5	26.0	
I_{SB2}[11]	Automatic power down current – CMOS inputs V_{CC} = 2.2 to 3.6 V and 4.5 to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2$V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, $V_{CC} = V_{CC(max)}$	25 °C	–	4.6	6.0[12]	µA
			40 °C	–	5.1	8.0[12]	
			70 °C	–	8.4	12.0[12]	
			85 °C	–	12.0	16.0	
	Automatic power down current – CMOS inputs V_{CC} = 1.65 to 2.2 V	$\overline{CE}_1 \geq V_{CC} - 0.2$V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, $V_{CC} = V_{CC(max)}$		–	5.5	26.0	

Notes
11. Chip enables ($\overline{CE}_1$ and CE_2) and $\overline{BYTE}$ must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
12. The I_{SB2} maximum limits at 25 °C, 40 °C, and 70 °C are guaranteed by design and not 100% tested.

Capacitance

Parameter [13]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25$ °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [13]	Description	Test Conditions	48-ball VFBGA	48-pin TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	31.50	57.99	°C/W
Θ_{JC}	Thermal resistance (junction to case)		15.75	13.42	°C/W

AC Test Loads and Waveforms

Figure 6. AC Test Loads and Waveforms
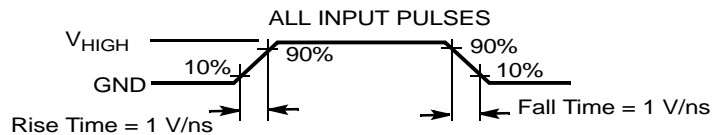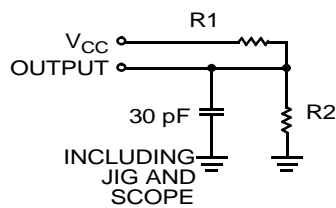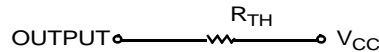
Parameters	1.8 V	2.5 V	3.0 V	5.0 V	Unit
R1	13500	16667	1103	1800	Ω
R2	10800	15385	1554	990	Ω
R_{TH}	6000	8000	645	639	Ω
V_{TH}	0.80	1.20	1.75	1.77	V

Note
13. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ[14]	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	–	V
I_{CCDR}[15, 16]	Data retention current	$1.2\ V \le V_{CC} \le 2.2\ V$, $\overline{CE}_1 \ge V_{CC} - 0.2\ V$ or $CE_2 \le 0.2\ V$ or ($\overline{BHE}$ and $\overline{BLE}$) $\ge V_{CC} - 0.2\ V$, $V_{IN} \ge V_{CC} - 0.2\ V$ or $V_{IN} \le 0.2\ V$	–	5.5	26.0	µA
		$2.2\ V < V_{CC} \le 3.6\ V$ or $4.5\ V \le V_{CC} \le 5.5\ V$, $\overline{CE}_1 \ge V_{CC} - 0.2\ V$ or $CE_2 \le 0.2\ V$ or ($\overline{BHE}$ and $\overline{BLE}$) $\ge V_{CC} - 0.2\ V$, $V_{IN} \ge V_{CC} - 0.2\ V$ or $V_{IN} \le 0.2\ V$	–	4.6	16.0	µA
t_{CDR}[17]	Chip deselect to data retention time		0	–	–	–
t_R[18]	Operation recovery time		45/55	–	–	ns

Data Retention Waveform

Figure 7. Data Retention Waveform [19]

Switching Characteristics

| Parameter [20, 21]	Description	45 ns Min	45 ns Max	55 ns Min	55 ns Max	Unit
READ CYCLE						
t_{RC}	Read cycle time	45.0	–	55.0	–	ns
t_{AA}	Address to data valid / Address to ERR valid	–	45.0	–	55.0	ns
t_{OHA}	Data hold from address change / ERR hold from address change	10.0	–	10.0	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid / $\overline{CE}$ LOW to ERR valid	–	45.0	–	55.0	ns
t_{DOE}	$\overline{OE}$ LOW to data valid / $\overline{OE}$ LOW to ERR valid	–	22.0	–	25.0	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[21]	5.0	–	5.0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[21, 22]	–	18.0	–	18.0	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low-Z[21]	10.0	–	10.0	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High-Z[21, 22]	–	18.0	–	18.0	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power-down	–	45.0	–	55.0	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to data valid	–	45.0	–	55.0	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low-Z[21]	5.0	–	5.0	–	ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High-Z[21, 22]	–	18.0	–	18.0	ns
WRITE CYCLE[23, 24]						
t_{WC}	Write cycle time	45.0	–	55.0	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35.0	–	40.0	–	ns
t_{AW}	Address setup to write end	35.0	–	40.0	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35.0	–	40.0	–	ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to write end	35.0	–	40.0	–	ns
t_{SD}	Data setup to write end	25.0	–	25.0	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[21, 22]	–	18.0	–	20.0	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[21]	10.0	–	10.0	–	ns

Notes
20. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and V_{CC}/2 (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$V). Test conditions for the read cycle use the output loading shown in Figure 6 on page 10, unless specified otherwise.
21. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
22. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
23. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both $= V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
24. The minimum write cycle pulse width for WRITE Cycle 1 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{HZWE} and t_{SD}

Switching Waveforms

Figure 8. Read Cycle No. 1 of CY62167G (Address Transition Controlled)[25, 26]
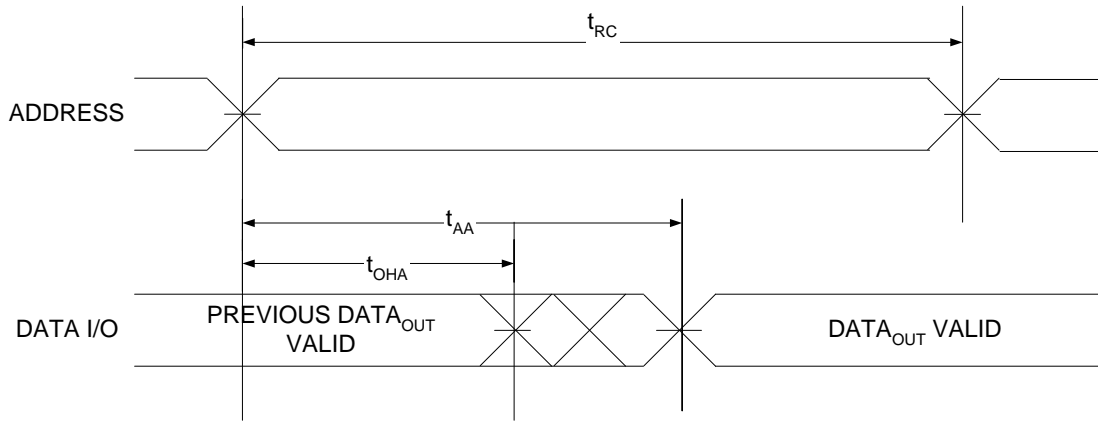
Figure 9. Read Cycle No. 1 of CY62167GE (Address Transition Controlled)[25, 26]
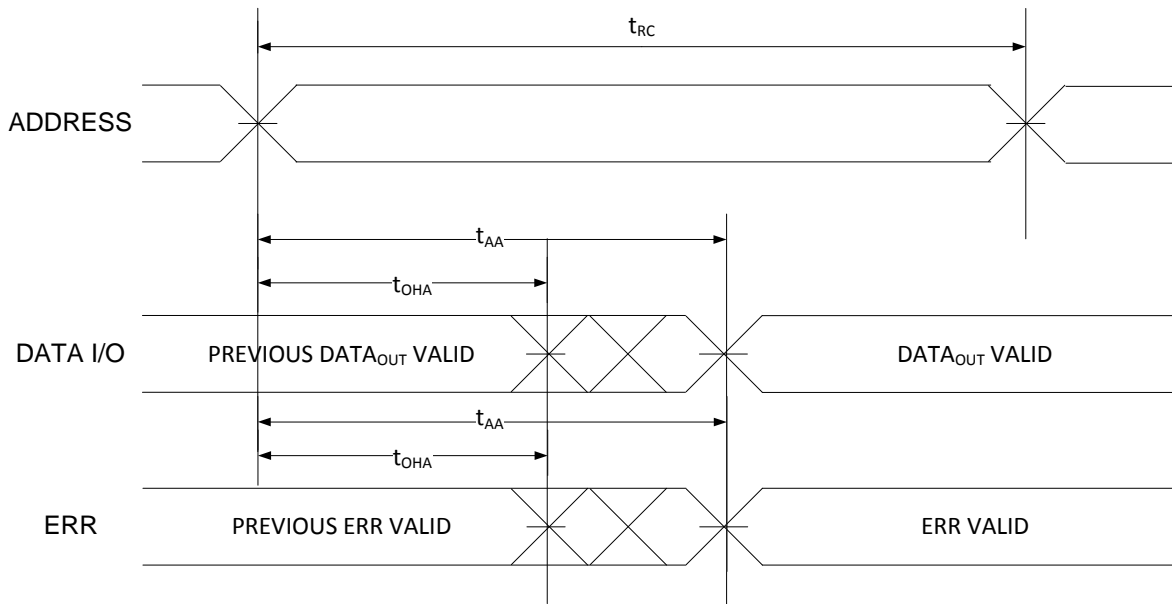
Notes
25. The device is continuously selected. $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$, or both = V_{IL}.
26. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 10. Read Cycle No. 2 ($\overline{OE}$ Controlled)[27, 28, 29, 31]
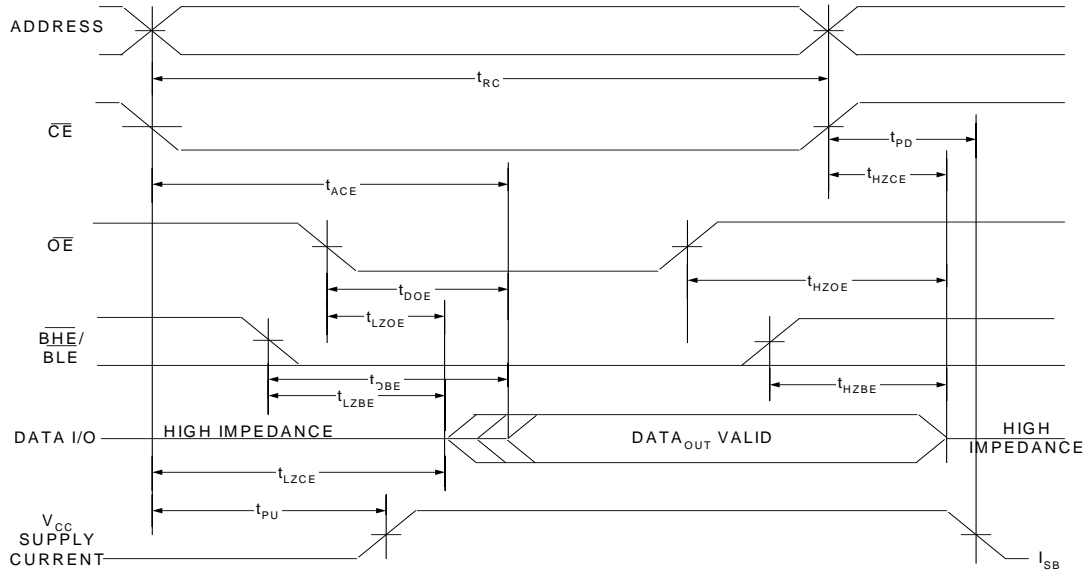
### Figure 11. Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[28, 30, 31, 33]
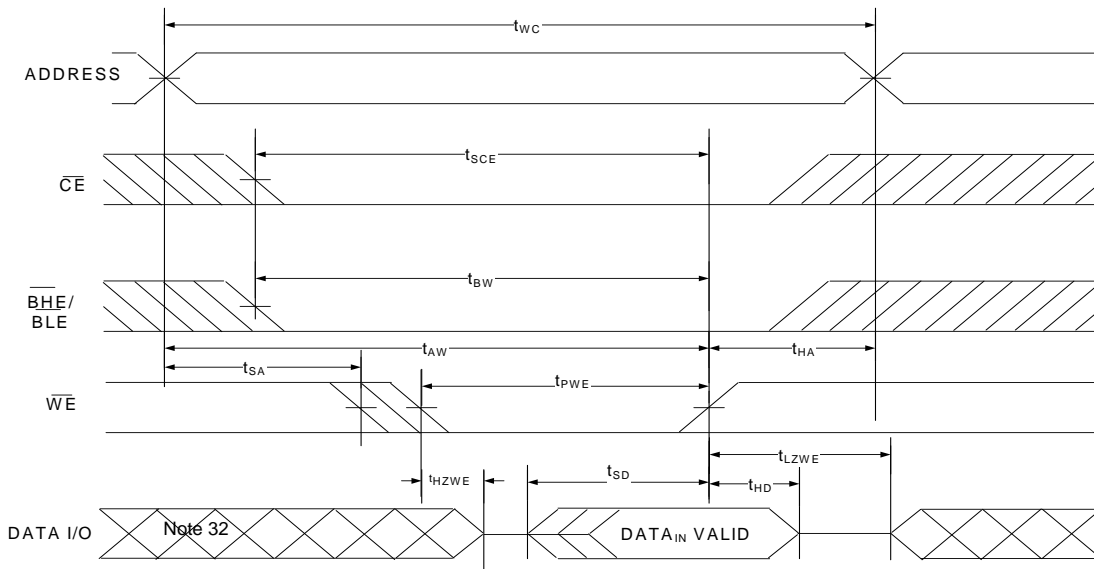
Notes

27. $\overline{WE}$ is HIGH for read cycle.
28. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
29. Address valid prior to or coincident with $\overline{CE}$ LOW transition.
30. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE_1} = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$, or both = V_{IL}, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
31. Data I/O is in the high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$, or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
32. During this period, the I/Os are in the output state. Do not apply input signals.
33. The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD}.

Switching Waveforms (continued)

Figure 12. Write Cycle No. 2 ($\overline{CE}$ Controlled) [34, 35, 36]
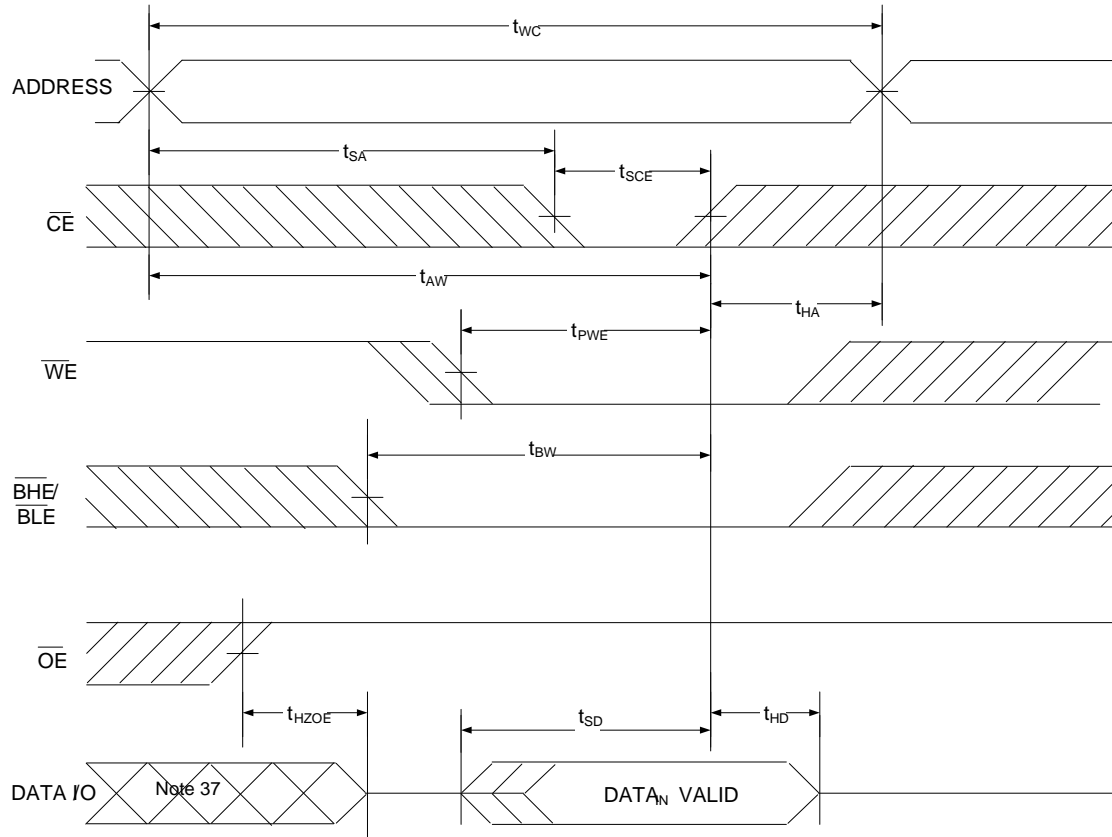
Notes
34. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
35. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both $= V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
36. Data I/O is in the high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$, or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
37. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 13. Write Cycle No. 4 (BHE/BLE controlled, OE LOW) [38, 39, 40]

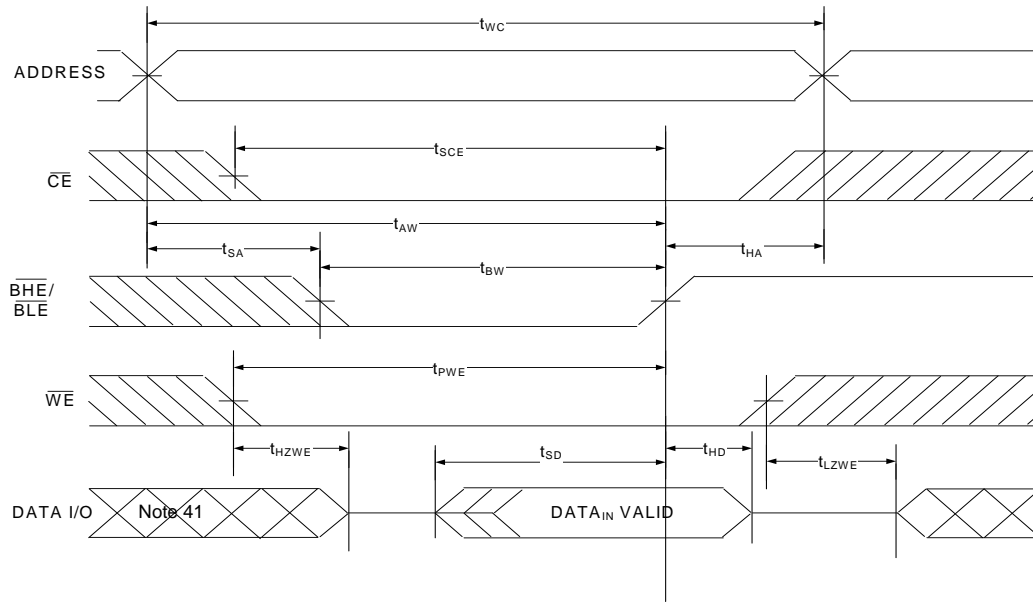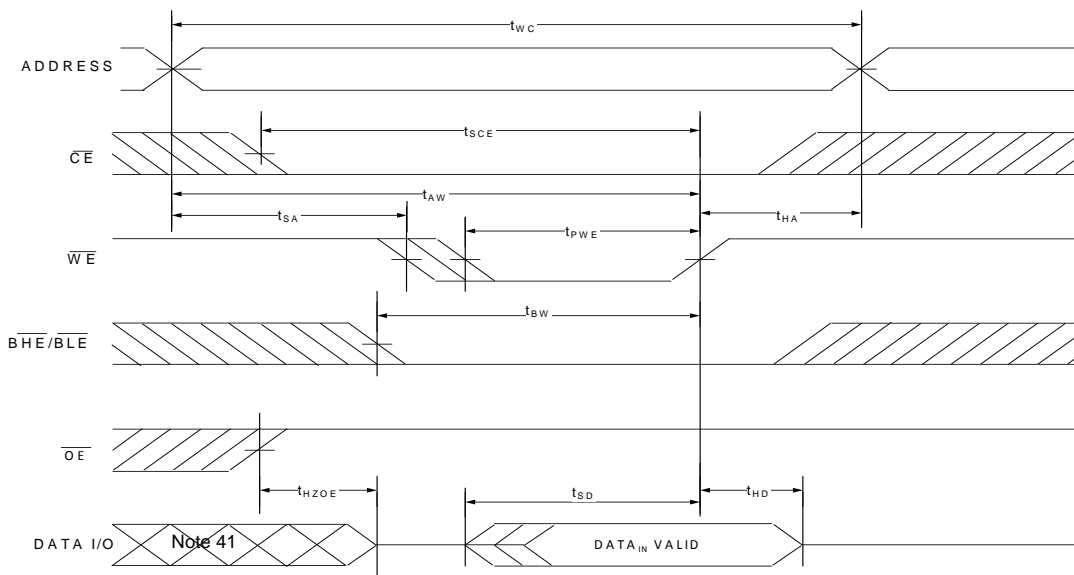**Figure 14. Write Cycle No. 5 (WE controlled)** [38, 39, 40]

Notes
38. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
39. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
40. Data I/O is in the high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$, or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
41. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table – CY62167G/CY62167GE

BYTE [42]	$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power	Configuration
X[43]	H	X[43]	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})	2 M × 8 / 1 M × 16
X	X[43]	L	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})	2 M × 8 / 1 M × 16
X	X[43]	X[43]	X	X	H	H	High-Z	Deselect/Power-down	Standby (I_{SB})	1 M × 16
H	L	H	H	L	L	L	Data Out (I/O$_0$–I/O$_{15}$)	Read	Active (I_{CC})	1 M × 16
H	L	H	H	L	H	L	Data Out (I/O$_0$–I/O$_7$); High-Z (I/O$_8$–I/O$_{15}$)	Read	Active (I_{CC})	1 M × 16
H	L	H	H	L	L	H	High Z (I/O$_0$–I/O$_7$); Data Out (I/O$_8$–I/O$_{15}$)	Read	Active (I_{CC})	1 M × 16
H	L	H	H	H	L	H	High-Z	Output disabled	Active (I_{CC})	1 M × 16
H	L	H	H	H	H	L	High-Z	Output disabled	Active (I_{CC})	1 M × 16
H	L	H	H	H	L	L	High-Z	Output disabled	Active (I_{CC})	1 M × 16
H	L	H	L	X	L	L	Data In (I/O$_0$–I/O$_{15}$)	Write	Active (I_{CC})	1 M × 16
H	L	H	L	X	H	L	Data In (I/O$_0$–I/O$_7$); High-Z (I/O$_8$–I/O$_{15}$)	Write	Active (I_{CC})	1 M × 16
H	L	H	L	X	L	H	High-Z (I/O$_0$–I/O$_7$); Data In (I/O$_8$–I/O$_{15}$)	Write	Active (I_{CC})	1 M × 16
L	L	H	H	L	X	X	Data Out (I/O$_0$–I/O$_7$)	Read	Active (I_{CC})	2 M × 8
L	L	H	H	H	X	X	High-Z	Output disabled	Active (I_{CC})	2 M × 8
L	L	H	L	X	X	X	Data In (I/O$_0$–I/O$_7$)	Write	Active (I_{CC})	2 M × 8

ERR Output – CY62167GE

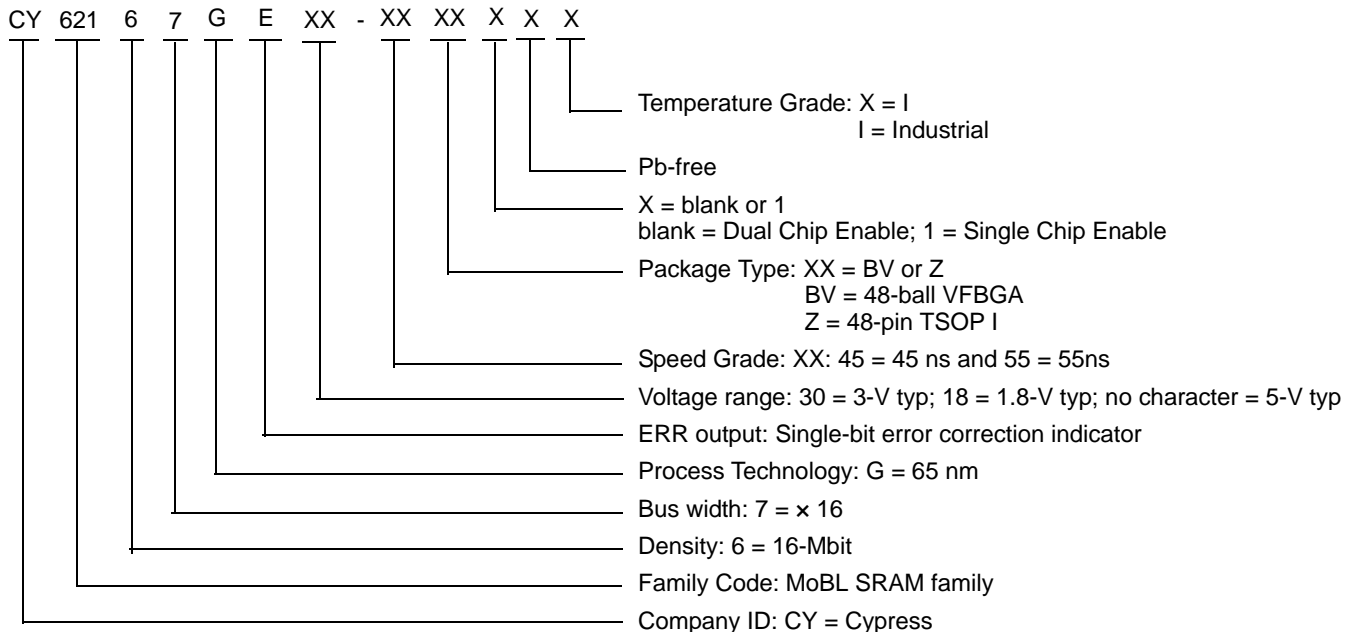| Output	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
High-Z	Device deselected / outputs disabled / Write operation

Notes
42. This pin is available only in the 48-pin TSOP I package. Tie the $\overline{BYTE}$ to V_{CC} to configure the device in the 1 M ×16 option. The 48-pin TSOP I package can also be used as a 2 M × 8 SRAM by tying the $\overline{BYTE}$ signal to V_{SS}.
43. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62167G30-45BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48, Dual Chip Enable without ERR	Industrial
	CY62167G30-45ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) (Pb-free), Package Code: Z48A, Dual Chip Enable without ERR	
	CY62167G-45ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) (Pb-free), Dual Chip Enable without ERR	
	CY62167GE30-45BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Dual Chip Enable with ERR output at pin E3	
	CY62167GE30-45ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) (Pb-free), Dual Chip Enable with ERR output at pin 13	
	CY62167GE-45ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1 mm) (Pb-free), Dual Chip Enable with ERR output at pin 13	
55	CY62167G18-55BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Dual Chip Enable without ERR	Industrial
	CY62167GE18-55BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Dual Chip Enable with ERR output at pin E3	

Ordering Code Definitions

CY 621 6 7 G E XX - XX XX X X X

Temperature Grade: X = I
I = Industrial

Pb-free

X = blank or 1
blank = Dual Chip Enable; 1 = Single Chip Enable

Package Type: XX = BV or Z
BV = 48-ball VFBGA
Z = 48-pin TSOP I

Speed Grade: XX: 45 = 45 ns and 55 = 55ns

Voltage range: 30 = 3-V typ; 18 = 1.8-V typ; no character = 5-V typ

ERR output: Single-bit error correction indicator

Process Technology: G = 65 nm

Bus width: 7 = × 16

Density: 6 = 16-Mbit

Family Code: MoBL SRAM family

Company ID: CY = Cypress

Package Diagrams

Figure 15. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150

NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Package Diagrams (continued)

Figure 16. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Z48A Package Outline, 51-85183

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary metal oxide semiconductor
I/O	Input/output
$\overline{OE}$	Output Enable
SRAM	Static random access memory
TSOP	Thin small outline package
VFBGA	Very fine-pitch ball grid array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Errata

This Errata is applicable for the Rev. *C silicon only.

This section describes the errata for the 16-Mbit asynchronous MoBL SRAM - CY62167G/CY62167GE - in the 65-nm process technology. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

If you have questions, contact your local Cypress Sales Representative or raise a technical support case at www.cypress.com/go/support.

Part Numbers Affected

Part Number	Device Characteristics
CY62167G (all packages and options) CY62167GE (all packages and options)	16-Mbit MoBL SRAM

CY62167G(E) Qualification Status

Product Status: Engineering Samples (**Note:** Reliability qualification is not complete. These samples are recommended to be used for engineering builds and evaluation only, and not for production builds).

CY62167G(E) SRAM Errata Summary

This table defines the errata applicability to available 16-Mbit devices.

Items	Part Numbers	Silicon Revision	Fix Status
[1] I_{SB1}, I_{SB2} and I_{CCDR} (Standby current specifications) do not meet datasheet spec	CY62167G/ CY62167GE	*C	Fixed devices available from December 14, 2014

1. I_{SB1}, I_{SB2} (Standby current) and I_{CCDR} (Data Retention Current) issue

■ **Problem Definition**

I_{SB1} (f = fmax), I_{SB2} (f = 0) and I_{CCDR} do not meet the datasheet limits as captured in the tables below.

Parameter	Description	Test Conditions		Datasheet Typ [14]	Errata Typ [14]	Unit
I_{SB2}[11]	Automatic power down current – CMOS inputs V_{CC} = 2.2 to 3.6 V and 4.5 to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, $V_{CC} = V_{CC(max)}$	25 °C	4.6	5.3	µA
			40 °C	5.1	5.8	
			70 °C	8.4	9.0	
	Automatic power down current – CMOS inputs V_{CC} = 1.65 to 2.2 V	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, $V_{CC} = V_{CC(max)}$		5.5	6.9	

Parameter	Description	Test Conditions	Datasheet Typ [14]	Errata Typ [14]	Unit
I_{SB1}[11]	Automatic power down current – CMOS inputs; V_{CC} = 2.2 to 3.6 V and 4.5 to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, f = f_{max} (address and data only),	4.6	5.3	µA
	Automatic power down current – CMOS inputs V_{CC} = 1.65 to 2.2 V	f = 0 ($\overline{OE}$, and $\overline{WE}$), $V_{CC} = V_{CC(max)}$	5.5	6.9	
I_{CCDR}[15,16]	Data retention current	1.2 V $\leq V_{CC} \leq 2.2$ V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	5.5	6.9	µA
		2.2 V $< V_{CC} \leq 3.6$ V or 4.5 V $\leq V_{CC} \leq 5.5$ V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	4.6	5.3	

■ **Parameters Affected**

Standby current specifications I_{SB1}, I_{SB2} and I_{CCDR}

■ **Trigger Condition**

When Chip Enable (s) is/are de-asserted to place the device in standby mode, the current drawn (I_{SB1}/ I_{SB2}) are greater than the datasheet-specified limit.

When Chip is in data retention mode, the current drawn (I_{CCDR}) is greater than the datasheet-specified limit.

■ **Scope of Impact**

Since these are Engineering samples and are expected to be used for evaluation, a marginal increase in standby/ data retention current is not expected to have an impact. Increase in standby/ data retention currents could result in a long term effect of reduced battery life; however, since these are Engineering samples expected to be used for engineering builds and evaluation only, impact is expected to be minimal.

■ **Workaround**

Ensure adequate source of power that accounts for the increased standby current

■ **Fix Status**

Fixed devices available from December 14, 2014.

Document History Page

Document Title: CY62167G/CY62167GE MoBL®, 16-Mbit (1 M words × 16 bit / 2 M words × 8 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81537				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	3690096	TAVA	07/26/2012	New data sheet.
*A	3776318	AJU	10/30/2012	Updated Document title to "16-Mbit (1 M words × 16 bit / 2 M words × 8 bit) Static RAM with Error-Correcting Code (ECC)". Updated Features (Included ECC feature, updated typical standby current spec). Added note #1 Corrected typos in Functional Description. Updated Logic Block Diagram – CY62167G, Logic Block Diagram – CY62167GE for better clarity. Updated Notes 2, 3, 4, 5 for better clarity. Listed all product options in Product Portfolio. Added typical values for I_{SB2} parameter. Updated Note 7 for better clarity. Updated Maximum Ratings to extend limits for 5 V device. Changed latch up current limit from 200 to 140 mA (per JEDEC limits). Updated DC Electrical Characteristics Corrected I_{OH} and I_{OL} conditions for V_{OH} and V_{OL} specifications. Added I_{CC} typical and maximum values at f = 1 MHz Changed typical spec for I_{SB1} and I_{SB2} from 2.5 µA to 3.2 µA. Split the I_{SB1} and I_{SB2} specs across multiple voltage ranges. Updated Description and Test Conditions for I_{SB1} and I_{SB2} parameters. Added Note 11 and referred it in the I_{SB1} and I_{SB2} parameters. Changed C_{IN} and C_{OUT} values from 8 pF to 10 pF. Updated Thermal Resistance values of Θ_{JA} and Θ_{JC} parameters for 48 pin TSOP I package. Added values for V_{HIGH} parameters in AC Test Loads and Waveforms. Updated Data Retention Characteristics Split Test Conditions of I_{CCDR} parameter into two rows to cover multiple V_{CC} ranges. Changed typical spec for I_{CCDR} from 2.5 µA to 3.2 µA. Updated Note 15 to remove byte enables. Updated Data Retention Waveform (Referred Note 19 in Figure 7). Updated Switching Characteristics Updated Notes 20, 23 for better clarity. Updated Switching Waveforms Updated Note 25 for better clarity. Updated Figure 10 as a single figure applicable to both CY62167G and CY62167GE. Referred Notes 28, 29 in Figure 10. Referred Note 28 in Figure 11. Corrected typos in Note 29, 31, 36, 40. Referred Note 34 in Figure 12.

Document History Page (continued)

Document Title: CY62167G/CY62167GE MoBL®, 16-Mbit (1 M words × 16 bit / 2 M words × 8 bit) Static RAM with Error-Correcting Code (ECC) **Document Number: 001-81537**				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*A (Cont.)	3776318	AJU	10/30/2012	Removed "Write Cycle No. 3 (WE controlled, OE LOW)" waveform. Removed the Note "During this period the I/Os are in output state. Do not apply input signals." and its references. Removed the Note "If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state." and its references (captured in Notes 31, 36, 40) Referred Notes 38, 39, 40 in Figure 13. Updated Truth Table – CY62167G/CY62167GE (Removed references of Note 43 in BHE and BLE column). Updated Package Diagrams (spec 51-85150 (Changed revision from *G to *H)).
*B	4003550	MEMJ	05/28/2013	Updated Document Title to read as "CY62167G/CY62167GE MoBL®, 16-Mbit (1 M words × 16 bit / 2 M words × 8 bit) Static RAM with Error-Correcting Code (ECC)" Added 55 ns (1.8 V) device details Updated Logic Block Diagram – CY62167G. Updated Logic Block Diagram – CY62167GE. Updated Pin Configuration – CY62167GE (Added Figure 4). Updated Product Portfolio: Updated details of I_{SB2} parameter. Updated DC Electrical Characteristics: Changed typical value of I_{CC} parameter from 5 mA to 7 mA and max value from 30 to 36. Changed typical value of I_{SB1} parameter from 3.2 µA to 4 µA for "V_{CC} = 1.65 to 2.2 V". Changed typical value of I_{SB2} parameter from 3.2 µA to 4 µA for "V_{CC} = 1.65 to 2.2 V". Updated AC Test Loads and Waveforms: Updated the table below Figure 6. Updated Data Retention Characteristics: Changed typical value of I_{CCDR} parameter from 3.2 µA to 4 µA for first condition only. Updated I_{cc} Typical to 29 mA from 25 mA. Updated Data Retention Waveform: Updated Figure 7. Updated Switching Waveforms: Updated Figure 12. Renamed "Truth Table – CY62167G" as Truth Table – CY62167G/CY62167GE and updated the same table (Added BYTE information). Updated Ordering Information (Updated part numbers).

Document History Page (continued)

Document Title: CY62167G/CY62167GE MoBL®, 16-Mbit (1 M words × 16 bit / 2 M words × 8 bit) Static RAM with Error-Correcting Code (ECC)				
Document Number: 001-81537				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*C	4094068	NILE / MEMJ	10/29/2013	Updated Product Portfolio: Updated values of "Operating I_{CC}" at f = f_{MAX} (Corresponding to 55-ns speed bin only). Replaced "an error detection" with "a single-bit error detection". Updated Pin Configuration – CY62167G: Updated title of Figure 1 and Figure 2. Updated Pin Configuration – CY62167GE: Updated title of Figure 5. Updated DC Electrical Characteristics: Referred Note 8 in description of V_{IH} parameter. Updated Test Conditions of I_{CC} parameter (Removed f = f_{MAX} and added f = 22.22 MHz (45 ns) and f = 18.18 MHz (55 ns) and added corresponding values). Added typical and maximum values for I_{SB2} parameter for intermediate temperatures. Updated Data Retention Characteristics: Added Note 16 and referred the same note in I_{CCDR} parameter. Updated Ordering Information: Updated part numbers. Segregated 45 ns and 55 ns parts list in the table. Updated "Package Type" column (Added ERR pin location information and Single or Dual Chip Enable information). Added Errata. Updated in new template.
*D	4274810	MEMJ	02/08/2014	Updated Operating Range: Added Note 9 and referred the same note in V_{CC} column.
*E	4292074	MEMJ / VINI	03/07/2014	Updated DC Electrical Characteristics: Changed I_{SB2}(Max) at 25C from 7uA to 4.8uA Changed I_{SB2}(typ) at 40C from 6uA to 4.5uA Changed I_{SB2}(Max) at 40C from 9uA to 8uA Added Note 10 and referred to typical values Added Note 24 and referred to write cycle timing parameters in Switching Characteristics Referred Note 31 to Figure 10. Changed title of Figure 11 from '$\overline{WE}$ controlled' to '$\overline{WE}$ controlled, $\overline{OE}$ LOW' Added Note 32 and 33 in Figure 11. Added Note 37 in Figure 12. Added Figure 14, $\overline{WE}$ controlled write Corrected ERR table by replacing "no error in stored data" with "no single bit error in stored data". Corrected ERR pin location to E3 in 'Dual Chip Enable with ERR option' in the 48-VFBGA package in Ordering Information. Added Note 41 in Figure 13 and Figure 14.
*F	4330547	AJU	04/02/2014	Changed lower limit for V_{CC} from 1.0 V to 1.2 V in I_{CCDR} conditions.

Document History Page (continued)

Document Title: CY62167G/CY62167GE MoBL®, 16-Mbit (1 M words × 16 bit / 2 M words × 8 bit) Static RAM with Error-Correcting Code (ECC) **Document Number: 001-81537**				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*G	4397546	VINI	06/03/2014	Updated Features: Changed typical standby current from 3.2 to 4.6 μA Updated Product Portfolio: Changed I_{SB1} and I_{SB2} typical from 4.0 to 5.5 μA and maximum from 23.0 μA to 26.0 μA in the 1.8-V part Changed 25 °C I_{SB1} and I_{SB2} typical from 3.2 to 4.6 μA and maximum from 4.8 μA to 6.0 μA in the 3.3-V and 5-V parts. Changed 40 °C I_{SB2} typical from 4.5 to 5.1 μA in the 3.3-V and 5-V parts Changed 70 °C I_{SB2} typical from 9.0 to 8.4 μA in the 3.3-V and 5-V parts. Reworded foot notes 10, 12, and 14. Referenced Note 12 from max values of I_{SB2} at 25 °C, 40°C and 70 °C Updated Data Retention Characteristics: Changed ICCDR typical current to 5.5 μA and maximum to 26.0 μA in the 1.8-V part Changed ICCDR typical current to 4.6 μA in the 3.3-V and 5-V parts.
*H	4489659	AJU	09/01/2014	Removed Errata (The Errata applicable for the Rev. ** silicon only). Added Errata (The Errata applicable for the Rev. *C silicon only).
*I	4469360	NILE	09/18/2014	No technical updates.

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