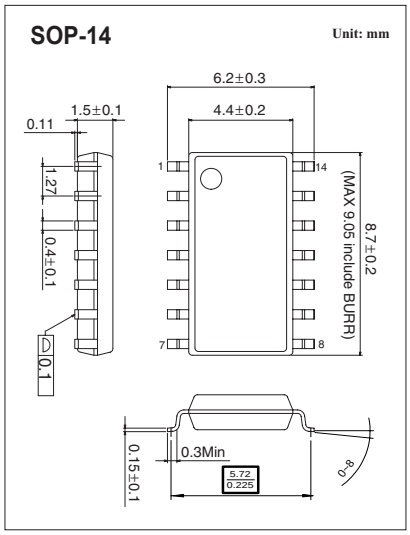
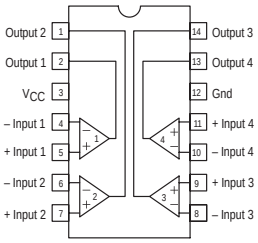
Quad Single Supply Comparators

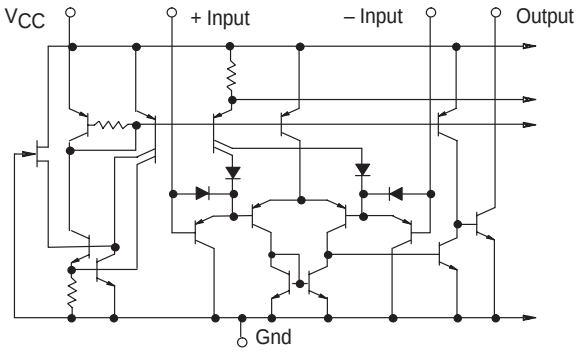
■ Features

- Single or Split Supply Operation
- Low Input Bias Current: 25 nA (Typ)
- Low Input Offset Current: ±5.0 nA (Typ)
- Input Common Mode Voltage Range to Gnd
- Low Output Saturation Voltage: 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible





■ Circuit Schematic



■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	V
Input Differential Voltage Range	V_{IDR}	36	V
Input Common Mode Voltage Range	V_{ICR}	-0.3 to V_{CC}	V
Output Short Circuit-to-Ground *	I_{SC}	Continuous	
Power Dissipation @ T_A = 25℃	P_D		
Derate above 25℃		8.0	mW/℃
Plastic Package		1.0	W
Operating Ambient Temperature Range	T_A	0 to 70	℃
Junction Temperature	T_J	150	℃
Storage Temperature Range	Tstg	-65 to +150	℃

* The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.

■ Electrical Characteristics (V_{CC} = +5.0 V, T_A =25℃, unless otherwise noted.)

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Input Offset Voltage *4	V_{IO}			±2.0	±5.0	mV
Input Bias Current *4,5	I_{IB}			25	250	nA
Input Offset Current *4	I_{IO}			±5.0	±50	nA
Input Common Mode Voltage Range	V_{ICMR}		0		V_{CC}-1.5	V
Supply Current	I_{CC}	R_L = ∞(For All Comparators)		0.8	2.0	mA
		R_L = ∞, V_{CC} = 30 V		1.0	2.5	
Voltage Gain	A_{VOL}	R_L≥15 kΩ, V_{CC} = 15 V	50	200		V/mV
Large Signal Response Time		V_I = TTL Logic Swing,V_{ref} = 1.4 V, V_{RL} = 5.0 V,R_L = 5.1 KΩ		300		ns
Response Time *6		V_{RL} = 5.0 V, R_L = 5.1 kΩ		1.3		μs
Output Sink Current	I_{Sink}	V_I (-)≥+1.0 V, V_I(+) = 0,V_O ≤ 1.5 V	6.0	16		mA
Saturation Voltage	V_{sat}	V_I(-) ≥+1.0 V, V_I(+) = 0,I_{sink} ≤4.0 mA		130	400	mV
Output Leakage Current	I_{OL}	V_I(+) ≥+1.0 V, V_I(-) = 0,V_O = +5.0 V		0.1		nA

■ Performance Characteristics (V_{CC}=+5.0V,0℃≤T_A≤70℃)

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Input Offset Voltage *4	V_{IO}				±9.0	mV
Input Bias Current*4,5	I_{IB}				400	nA
Input Offset Current *4	I_{IO}				±150	nA
Input Common Mode Voltage Range	V_{ICMR}		0		V_{CC}-2.0	V
Saturation Voltage	V_{sat}	V_I(-) ≥ +1.0 V, V_I(+) = 0,I_{sink} ≤ 4.0 mA			700	mV
Output Leakage Current	I_{OL}	V_I(+)≥ +1.0 V, V_I(-) = 0,VO = 30 V			1.0	μA
Differential Input Voltage	V_{ID}	All VI≥ 0 V			V_{CC}	V

*4. At the output switch point, V≈ 1.4 V, Rs ≤ 100 Ω 5.0 V ≤ V_{CC} ≤ 30 V, with the inputs over the full common mode range (0 V to V_{CC} -1.5 V).

*5. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.

*6. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.