AN4207
Application note

Getting started with STM32F37x/38x SDADC (Sigma-Delta ADC)

Introduction

The STM32F37x series of microcontrollers combines a 32-bit ARM Cortex-M4 core with a DSP and FPU instructions running at 72 MHz with advanced analog peripherals.

This series introduces the combination of a Cortex-M4 core with a precise 16-bit Sigma-Delta ADC.

This document outlines the main features of the SDADC and shows how the SDADC can be used in various application cases. By way of example, four application cases are presented in this document:

1. Temperature measurement using PT100
2. Pressure measurement using MPX2102A
3. Wave recorder
4. ElectroCardioGram (ECG) acquisition

To help you get started quickly, the four application cases are implemented in C language and are available as part of the STM32F37x DSP and standard peripherals library package *stm32f37x_dsp_stdperiph_lib* and the STM32373C-EVAL demonstration firmware package *stm32373c-eval_fw*

Please note that this document is not intended to replace the Sigma-Delta Analog to Digital Converter (SDADC) section in the STM32F37xx/STM32F38xx reference manual RM0313.

All values given in this document are guidance only. Please refer to the related datasheet to get guaranteed and up-to-date values.

Table 1. Applicable products

Type	Part numbers
Microcontrollers	STM32F37X, STM32F38x

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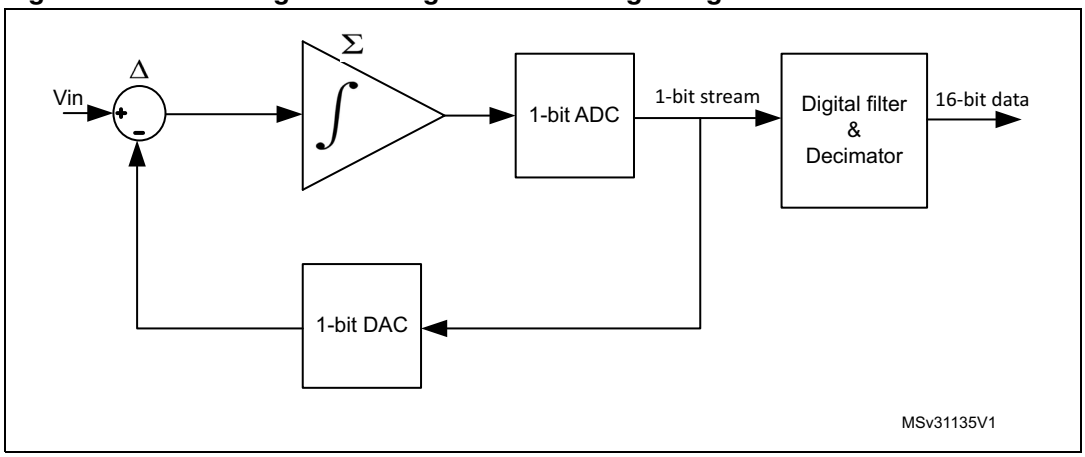
1 Basics of sigma-delta converters

Sigma-delta converters, also known as oversampling converters, consist of two basic circuits: a modulator and a digital filter (*Figure 1*). In the modulator, the input signal is added to the negative feedback signal from the digital to analog converter (DAC). The signal's difference, after passing through the integrating circuit, reaches the input of the comparator (1-bit ADC), where it is compared to the reference voltage (the comparator works as a 1-bit quantizer). The input signal from the comparator (1-bit ADC) controls the 1-bit converter and reaches the input of the digital filter, which decreases flowability and transforms the 1-bit stream into 16-bit words. The used filter topology that ensures the low-pass stage is Sinc³.

Figure 1. Block diagram of a sigma-delta analog to digital converter



2 Overview of 16-bit SDADC

2.1 Main features

STM32F37x/38x devices have three embedded Sigma-Delta Analog to Digital Converters (SDADC). They can be synchronized together and each has the following main features:

- Effective number of bits (ENOB) equal to 14 bits
- 5 differential input pairs, or 9 single-ended inputs, or a combination
- High-performance data throughput:
  - 16.6 ksps input sampling rate when multiplexing between different channels
  - 50 ksps input sampling rate for single-channel operation
- Programmable gain: x0.5, x1, x2, x4, x8, x16 and x32
- Selectable reference voltage: V_{DDSD}, 1.22 V, 1.8 V and V_{REF}

2.1.1 Clock selection

The SDADC clock is supplied by SDADCCLK which divides the system clock (SYSCLK) by a selectable prescaler: 2, 4, 6, 8, 10, 12, 14, 16, 20, 24, 28, 32, 36, 40, 44 and 48.

The typical operating frequency of SDADC is 6 MHz in fast mode and 1.5 MHz in slow mode.

Example:

If SYSCLK is set to 72 MHz, the SDADC divider should be set to SYSCLK/Typical Frequency:

Fast speed mode: prescaler = 72 MHz / 6 MHz = 12

Low speed mode: prescaler = 72 MHz / 1.5 MHz = 48

2.1.2 Input modes

The SDADC has three possible input modes, that can be combined.

- Differential mode:
- Single ended offset mode
- Single ended zero reference mode

Differential mode

It is recommended to use differential mode when the sensors being used produce very small signals that are very susceptible to noise. This is especially the case when using thermocouple and bridge type sensors (pressure sensors).

In differential mode, the SDADC converts the difference between SDADCx_AINyP and SDADCx_AINyM. The result can be either positive or negative depending on which input is at higher voltage.

Note: The SDADC can not measure negative voltages and the input voltage on each channel must stay within the electrical limits of the device.

The input range is [-Vref/(2*gain), + Vref/(2*gain)] and the conversion value is in the range [-32767, +32767]

Example:

For a 1.22V reference voltage and a gain set to 1, the input range is +/- 0.61V

The formula is:

Vin = SDADCx_AINyP - SDADCx_AINyM = ReadData * Vref/(2 x gain x 32767)

with ReadData is two's complement read data from the SDADC data register (SDADCx_JDATAR or SDADCx_RDATAR)

Figure 2. Input signal range in differential mode

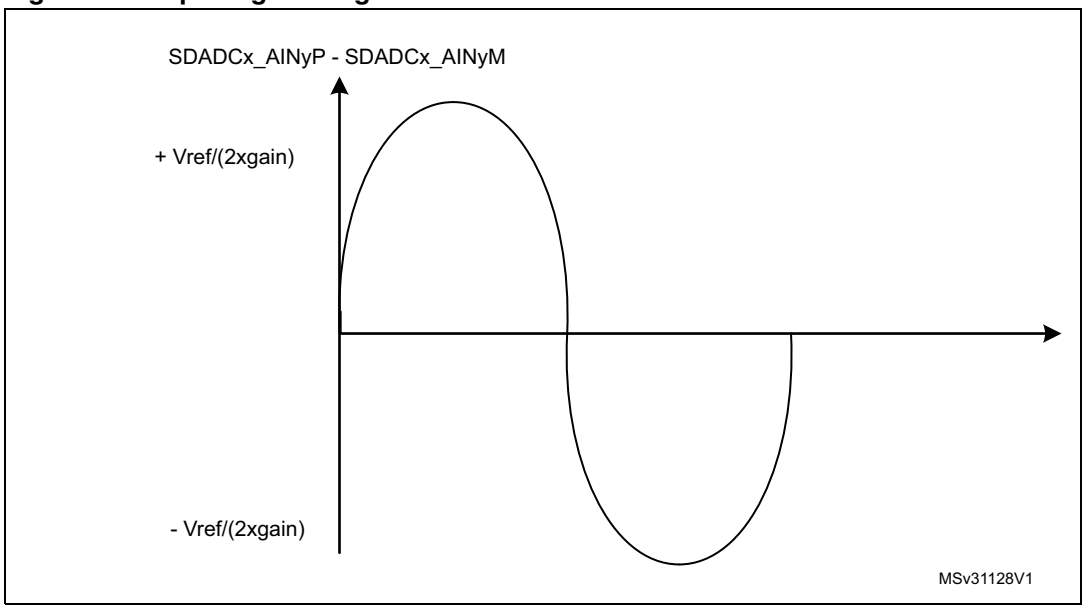
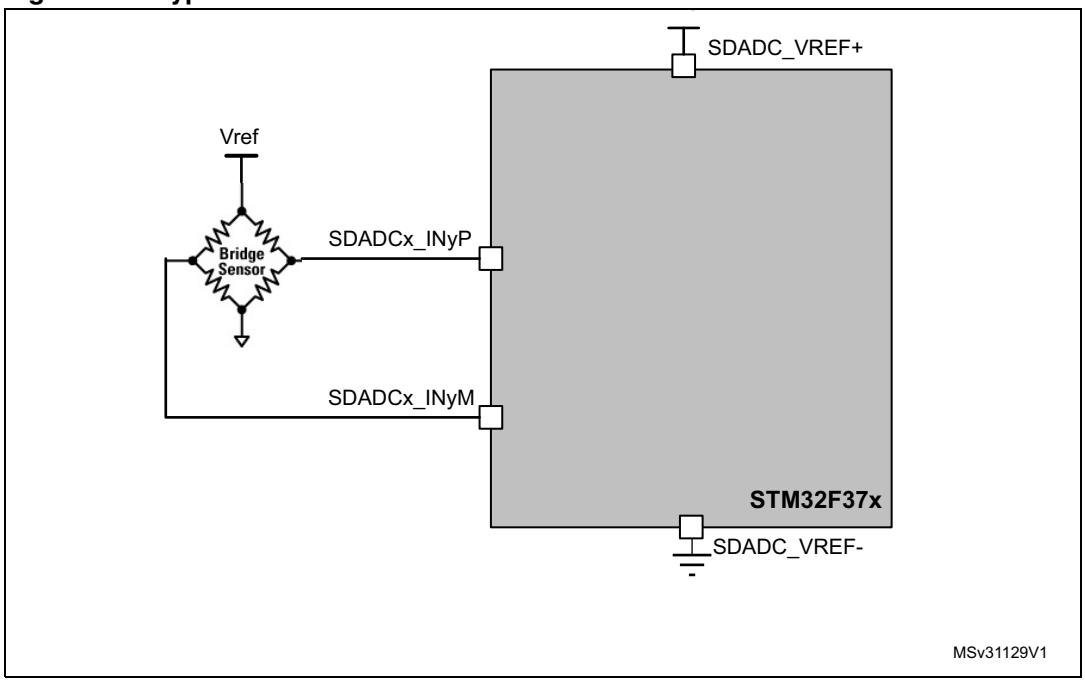


Figure 3 shows how to connect a bridge type sensor to the 16-bit SDADC.

As shown below both positive (SDADCx_AINyP) and negative (SDADCx_AINyM) inputs are connected to sensor outputs.

Figure 3. Typical connection of differential sensor to differential channels



Single ended offset mode

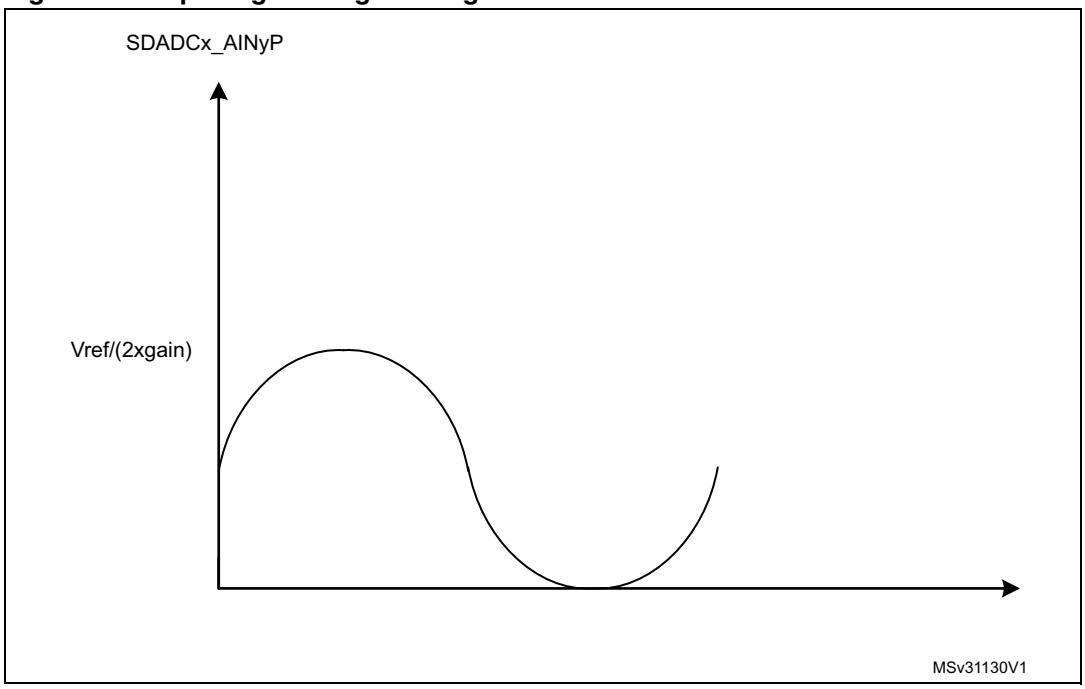
In single ended offset mode, conversions are performed by connecting the negative input to 0 V internally, leaving the corresponding pin for the negative input (SDADCx_AINyM) free to be used for other purposes. The signal to be measured is applied to the positive input SDADCx_AINyP. This mode of operation is similar to differential mode, except that the output data is only from 0 to +32767, and not from –32767 to +32767, therefore half the dynamic range is lost, consequently the SNR is degraded.

The formula is:

$$Vin = SDADCx\_AINyP = ReadData * Vref/(2 \times gain \times 32767)$$

with ReadData is two's complement read data from SDADC data register (SDADCx_JDATAR or SDADCx_RDATAR)

Figure 4. Input signal range in single ended offset mode



Single ended zero reference mode

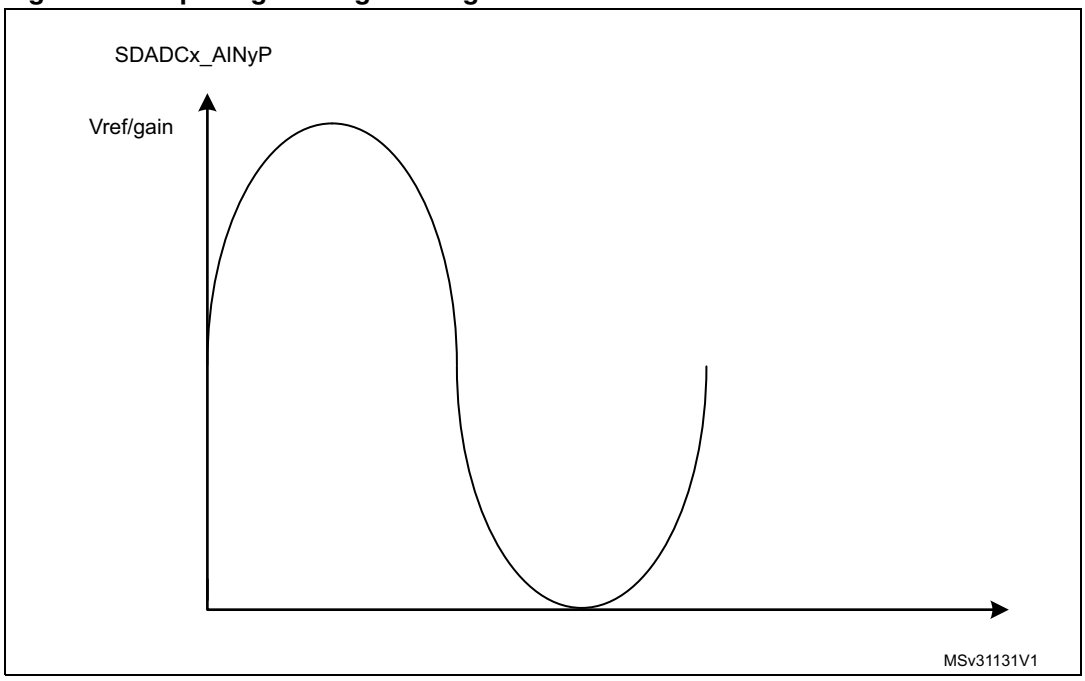
The signal is applied to the positive input SDADCx_AINyP, and the negative input is set to the signal reference (normally 0 V). This mode injects an input common mode of half scale to the ADC thus maintaining the dynamic range the same as in differential mode (-32767 to +32767). In this mode, the injected common mode is dependent on gain variations.

The formula is:

$$Vin = SDADCx\_AINyP = (ReadData + 32767) * Vref/(gain \times 65535)$$

with ReadData is two's complement read data from SDADC data register (SDADCx_JDATAR or SDADCx_RDATAR)

Figure 5. Input signal range in single ended zero reference mode



Note: When channel p (with p is even) is used in differential mode, the channel p+1 is automatically used as minus input (SDADCx_AINyM) and therefore channel p+1 can not be used in single ended mode (zero reference mode or offset mode).

When channel 4 is configured in differential mode channel 5 is automatically used as minus input and therefore channel 5 can not be used either in single ended offset mode or in single ended zero reference mode.

2.1.3 SDADC voltage references

The SDADC reference voltage is selectable among four sources:

1. VREFINT1: A 1.2V embedded reference voltage
2. VREFINT2: A 1.8V embedded reference voltage
3. VDDSD: The SDADC analog supply voltage. It ranges from 2.2 V to 3.6 V
4. VREFSD+: The external SDADC reference voltage. It ranges from 1.1 V to VDDSD

The table below shows the voltage weights per bit (step size) using three possible references.

Table 2. Voltage step sizes

VREFSD+	µV/bit
VREINT1: 1.2	18.46
VREINT2: 1.8	27.69
3.3V	50.35

2.1.4 Calibration

In order to get the best performance from the SDADC two parameters should be calibrated. These parameters are offset and gain.

Offset calibration

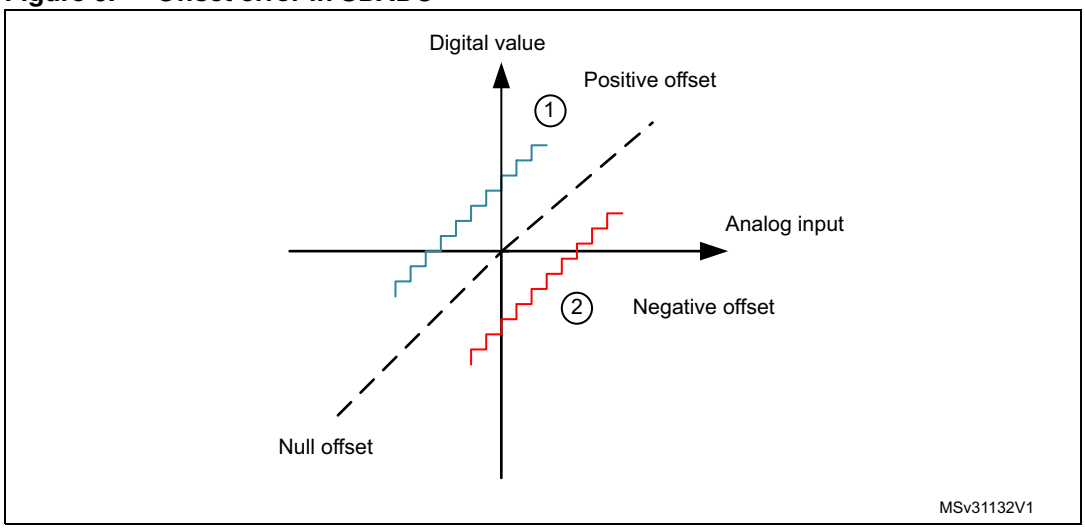
The offset error is a constant value that is added to the ideal conversion value.*Figure 6* illustrates the offset error.

The SDADC embedded in STM32F37x/38x devices provides automatic offset calibration without adding external components. Its principle can be summarized in the following steps:

1. Short internally both channel inputs (positive and negative)
2. Perform conversion and store result in internal register (configuration register)
3. Subtract automatically the calibration value from conversion value during standard conversion.

Note: It is recommended to run calibration at least once after SDADC configuration

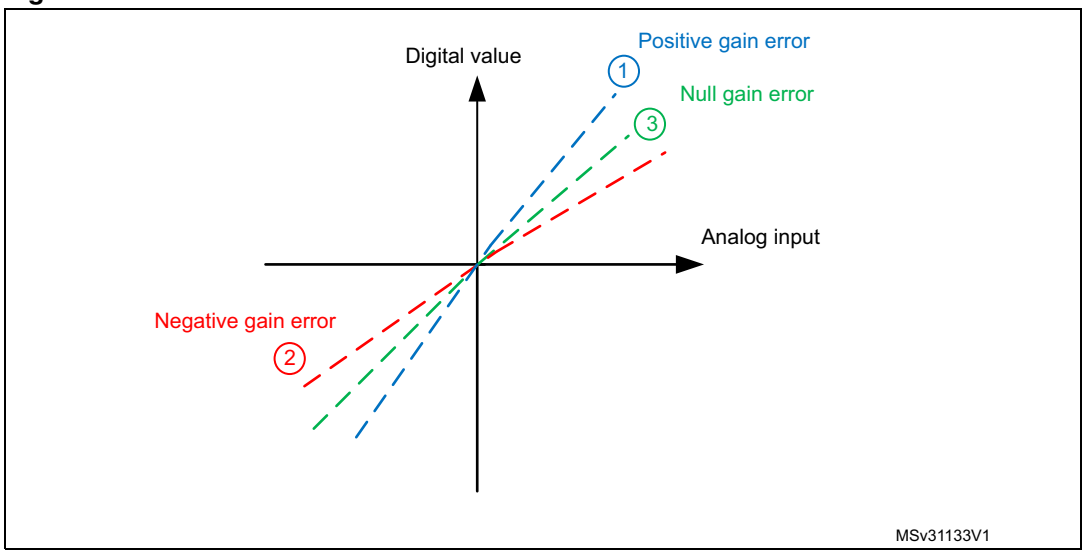
Figure 6. Offset error in SDADC



Gain calibration

Another error source is the gain error. As illustrated in *Figure 7* the gain error is the deviation of the SDADC's transfer function from the ideal straight line. It is due to the built-in programmable amplifier. According to the device datasheet the typical analog gain error is -2.7% which means there can be 884 counts (at maximum voltage) due to gain error. So reducing the gain error is mandatory when performing accurate measurements.

Figure 7. Gain error in SDADC



Two types of gain are implemented in the SDADC:

Analog gain: x1/2, x1, x2, x4, x8

Digital gain: x16 and x32.

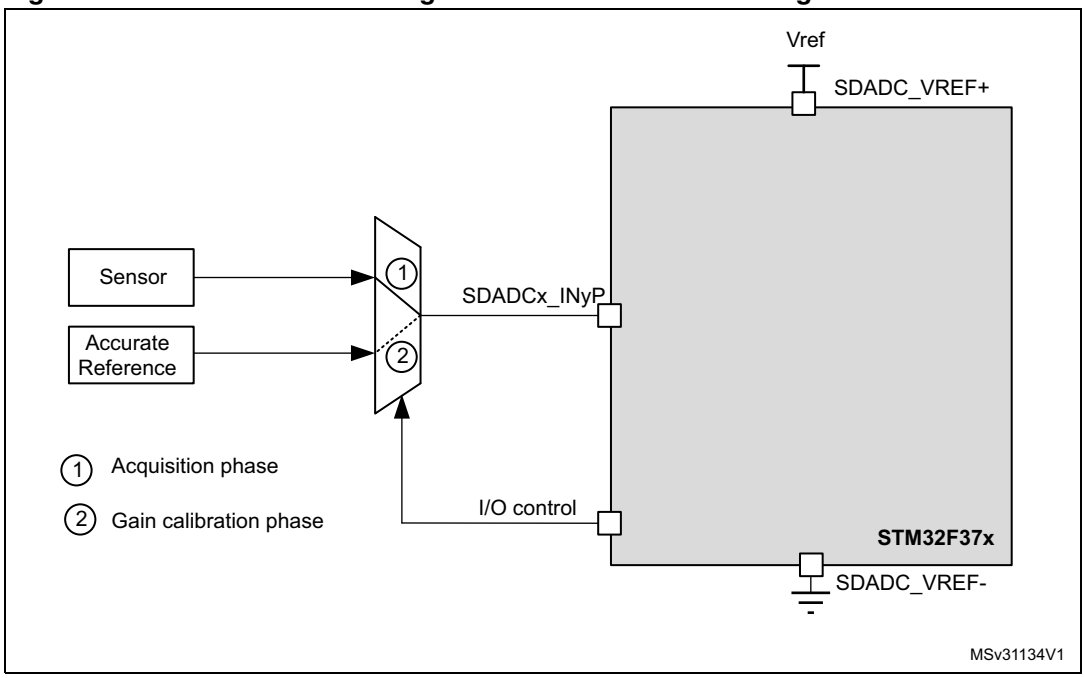
Only the analog gains are considered in gain calibration.

Gain calibration requires an external accurate reference and it is performed by applying the accurate reference voltage (AccRef) at the SDADC input and getting the SDADC output. The gain is computed as following: AccRef/(Output x Vref/65535)

The computed gain can be stored in non-volatile memory (Flash memory) and used during acquisition phase

Note: Before running gain calibration it is mandatory to run offset calibration.

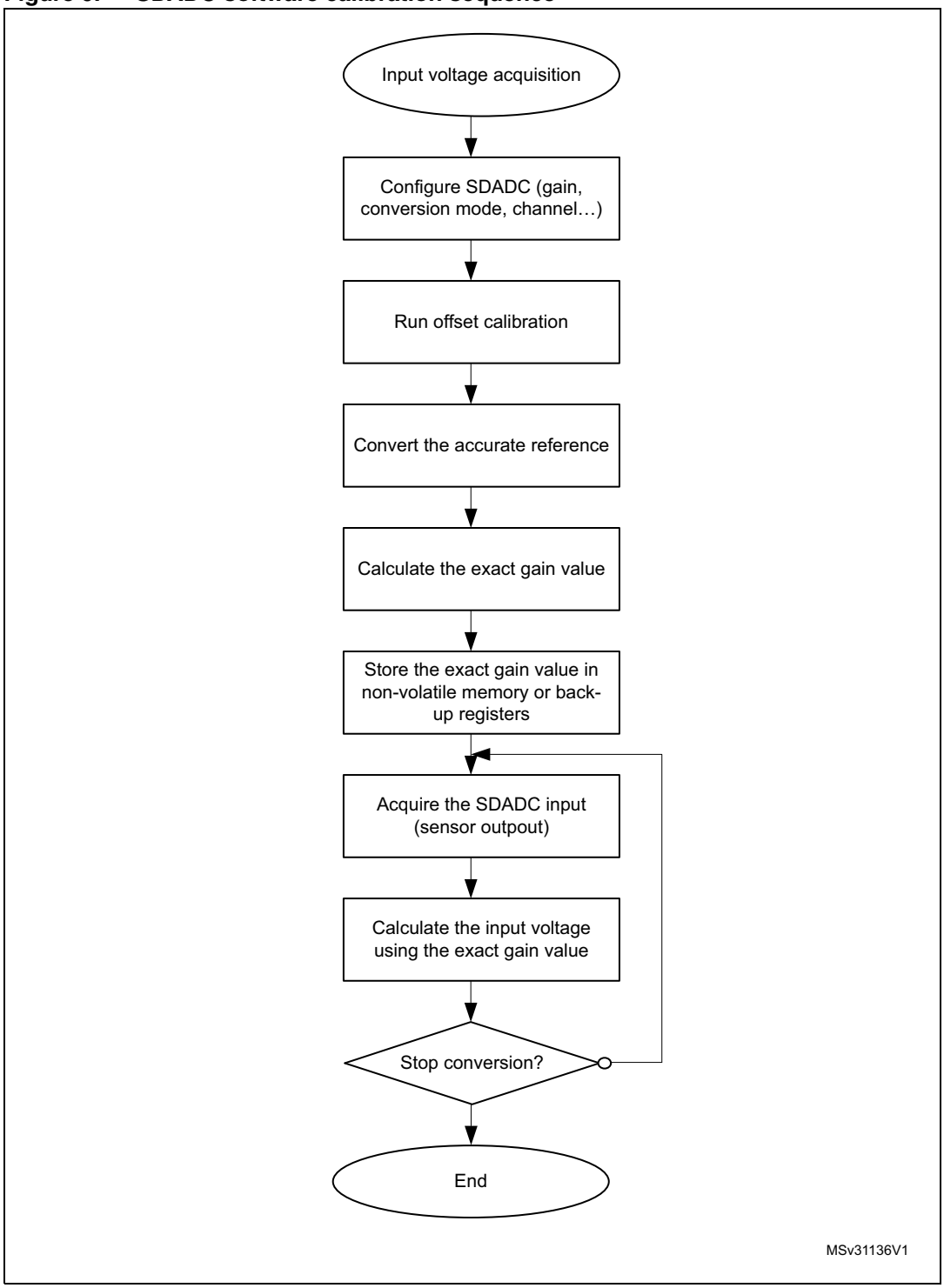
Figure 8. Gain calibration using the accurate reference voltage



Software procedure for offset and gain calibration

The flowchart below shows a typical SDADC application using both offset and gain calibration.

Figure 9. SDADC software calibration sequence



2.1.5 Matching impedance

The impedance of the analog signal source, or series resistance (R_{AIN}), between the source and the MCU pin may lead to a voltage drop across it because of the current flowing into the pin.

In SDADC, the channel input impedance depends on:

1. SDADC clock
2. Analog gain (0.5 - 8)

The figure below shows the equivalent input circuit for input channel where R_{in} is the input impedance of SDADC analog input and can be calculated using the formula below.

$$R_{in} = \frac{1}{2 \cdot f_{clk} \cdot C}$$

Figure 10. Equivalent input circuit for input channel

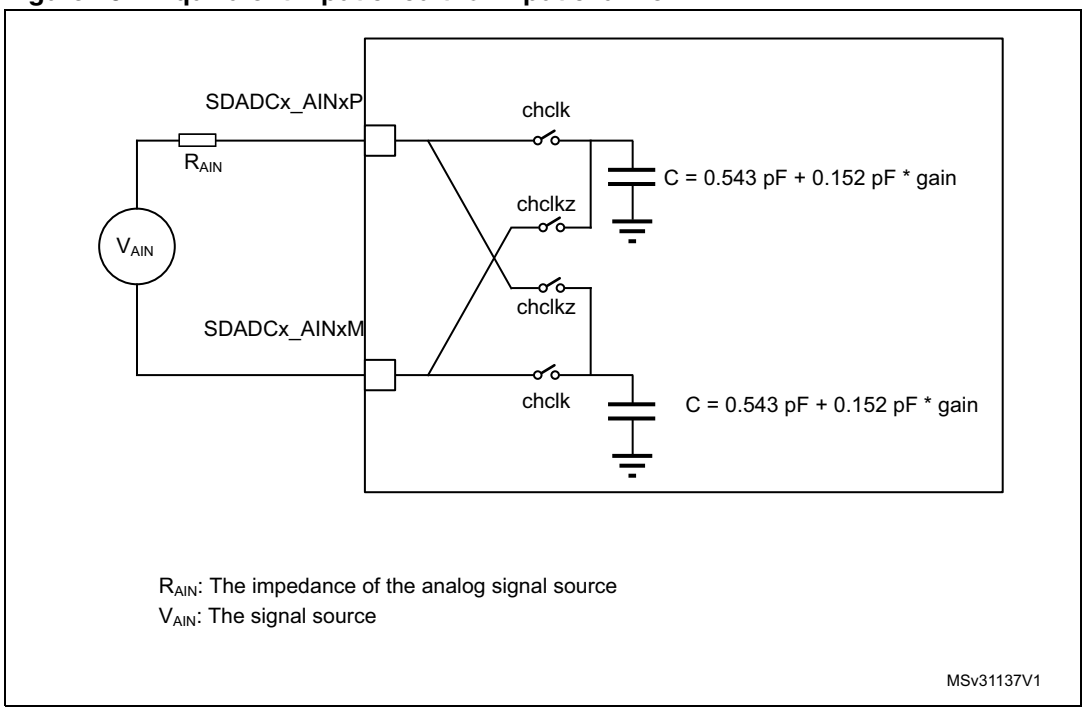


Table 3. Typical SDADC input channel input impedance

Frequency	Gain	R_{IN}
1.5 MHz	0.5	540 KΩ
6 MHz	0.5	135 KΩ
6 MHz	8	47 KΩ

2.1.6 Low power modes

The 16-bit SDADC combines both high resolution and low power consumption making it suitable for battery-powered products. If the SDADC is left powered-up continuously, it consumes 1.2 mA maximum (typically 800 µA). The SDADC has three main modes for reducing power consumption:

1. Slow mode: In this mode, the SDADC consumes 600 µA maximum but the sampling rate is limited to 12.5 Ksps maximum
2. Standby mode: In this mode, the SDADC consumes a maximum of about 200 µA but a stabilization time of 300 SDADC clock cycles (50 µs @ 6 MHz) is required each time it exits from Standby mode.
3. Power down mode: In this mode, the SDADC consumes a maximum of about 2.5 µA but a stabilization time of 600 SDADC clock cycles (100 µs @ 6 MHz) is required each time it exits from Standby mode.

3 Sigma-delta (SD) vs. successive approximation register (SAR) analog-to-digital converters

Analog to digital converters come in different architectures to be able to address the needs of different applications. The main types available in the market are:

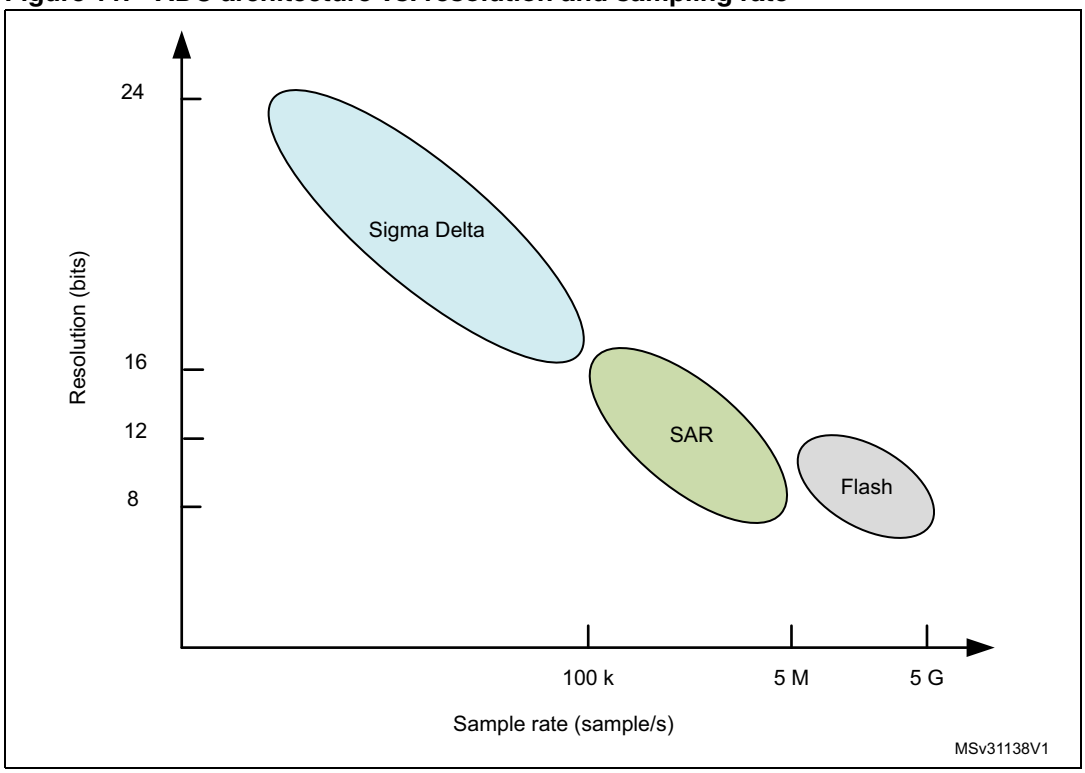
Successive approximation register (SAR) ADC: Successive-approximation-register (SAR) analog-to-digital converters (ADCs) are frequently used in embedded systems, with sample rates of less than 5 megasamples per second (Msps). Their resolution ranges from 8 to 16 bits. This type of ADC is used in industrial control applications.

Sigma-delta ADC (SDADC): Sigma-Delta analog-to-digital converters (ADCs) are used in lower speed applications requiring high resolution. The resolution may attain 24 bits by oversampling but the sampling rate is limited to only a few ksps.

Flash ADC: Flash analog-to-digital converters, are the fastest type of analog to a digital converter. They are suitable for applications requiring a very high sampling rate. However, flash converters have low resolution (12-bits). This type of ADC is used in oscilloscopes.

The *Figure 11* gives an overview of the different ADC architectures, comparing their resolution and sampling rate.

Figure 11. ADC architecture vs. resolution and sampling rate



The STM32F37x/38x devices have two types of embedded ADCs: 12-bit SAR ADC and 16-bit SDADC.

The *Table 4* summarizes the differences between the two types of ADC.

Table 4. SDADC vs. SAR ADC feature comparison

Feature	SDADC	SAR ADC
Max sampling rate	50 Ksps(1)	1 Msps
Resolution	16 bits	12 bits
Input mode	Single-ended differential	Single-ended
Embedded gains	0.5x to 32x	No
Number of channels	5 differential input pairs or 9 single-ended inputs	16 single-ended inputs
Number of instances	3 with synchro capability	1
Automatic Offset calibration	Yes	Yes
Analog watchdog	No	Yes
Trigger sources for regular conversion	– Software – Start of conversion of another SDADC	– Software – Embedded timers – External events
Trigger sources for injected conversion	– Software – Embedded timers – External events – Start of conversion of another SDADC	– Software – Embedded timers – External events
Input range		[V_{REF-}, V_{REF+}]
Reference voltage	1.22 V 1.8 V VDDSD VREFSD+	V_{REF+}
Input impedance(2)	47 KΩ to 540 KΩ	125 KΩ to 2500 KΩ

1. The sampling rate is 50 ksps when selecting a single channel and 16.6 ksps when multiplexing between different channels.
2. For SDADC, the input impedance depends on the selected gain and the selected operating frequency (1.5 MHz or 6 MHz).
   For SAR ADC, the input impedance depends on used sampling frequency (0.05 - 1 MHz) and sampling capacitor (8pF).

4 Application examples

This section presents how the 16-bit SDADC embedded in STM32F37x/38x devices can be used in application examples such as temperature measurement, pressure measurement, three-phase power meter, voice recorder...

4.1 Temperature measurement

This purpose of this application is to show how to use the 16-bit resolution Sigma-Delta Analog-to-Digital converter to perform accurate temperature measurement using the PT100 sensor connected to PE7 in the STM32373C-EVAL evaluation board.

The application source code is available in are available in the

Project\STM32F37x_StdPeriph_Examples\SDADC

folder in the STM32F37x DSP and standard peripherals library package stm32f37x_dsp_stdperiph_lib.

A current source circuit available on the STM32373C-EVAL board is used to provide a fixed 1 mA current (when V_{DD} = 3.3 V) to the temperature sensor PT100 which is connected to SDADC1 channel 3P (PE7) through a reference resistor 1K8 labeled R33.

The SDADC is configured in single-ended offset mode. The input range is from 0 V to V_{REF}/(2*gain).

In this application, the SDADC internal gain is set to 8 so the range is from 0 V to V_{REF}/16. The external reference V_{REF} (set to 3.3V on STM32373C-EVAL) is used as reference for SDADC using JP17 so the measurement ranges between 0 V and V_{REF}/16 = 0.20625V. The conversion is performed in continuous mode with interrupts enabled on End $_{Of}$ Regular Conversion.

The temperature is computed using the formula below:

Rpt100 = 100 + 0.385 * T

$\rightarrow$ T = (Rpt100 - 100) / 0.385

Vpt100 = Rpt100 * Ipt100 = Rpt100 * VDD_ANA / 2 * Rref

$\rightarrow$ Rpt100 = Vpt100 * 1800 * 2 / VDD_ANA

$\rightarrow$ T = ((Vpt100 * 1800 * 2 / VDD_ANA) - 100) / 0.385

where:

Rpt100 is the resistance of the PT100 sensor

Vpt100 is the voltage measured on PT100 sensor

Ipt100 is ~ 1mA current crossing the PT100 sensor

VDD_ANA is the analog voltage

Rref is the reference resistor 1K8 labeled R33 on STM32373C-EVAL

Table 5. Temperature sensor voltage range

V_{DD} = 3.3V	Temperature	Resistance (Ω)	Voltage (mV)
Rref = 1.8 K	0 °	100	91.667
	20°	107.7	98.725
	50 °	119.2	109.2667

The temperature measurement is performed in two steps:

1. **Temperature sensor calibration:** this phase is performed with JP18 fitted in 2-3(REF) position. A 100 Ohm resistor is connected to PE7 which is connected to VREF through the reference resistor. The SDADC converter measures the analog voltage applied on PE7 and then computes the correction coefficient. This calibrates the gain. The PT100 is not connected in this phase.
2. **Temperature measurement:** this phase is performed with JP18 fitted in 1-2 (PT100) position. The PT100 sensor is connected to PE7 which is connected to VREF through the reference resistor. The SDADC converter measures the analog voltage applied on PE7 and then computes the temperature which is given by the following formula:

TemperaturePT100 = (((((CoeffCorrection * (AvrgRegularConvData/SDADC_GAIN) * REFERENCE_RESISTOR * 2) / SDADCRESOL) - RESISTANCE_ZERODEGRE) / RESISTANCE_COEFFICIENT);

where:

AvrgRegularConvData is the average value of 256 samples

SDADC_GAIN is the internal SDADC gain. In this example it is set to 8

CoeffCorrection is the correction coefficient computed in phase 1.

REFERENCE_RESISTOR is the reference resistor 1K8 labeled R33 on STM32373C-EVAL

SDADCRESOL is the sigma delta converter: 2e16-1

RESISTANCE_ZERODEGRE is the resistance of PT100 at 0 °C

RESISTANCE_COEFFICIENT is the coefficient of PT100 sensor

4.2 Pressure measurement

This application is intended to show how to use the 16-bit sigma-delta analog-to-digital converter to perform pressure measurement using the absolute pressure sensor MPX2102A mounted on the STM32373C-EVAL evaluation board.

The application source code is available in the

Project\STM32F37x_StdPeriph_Examples\SDADC

folder in the STM32F37x DSP and standard peripherals library package *stm32f37x_dsp_stdperiph_lib*.

On the STM32373C-EVAL board, The MPX2102A sensor is connected to SDADC1 channel 8P (PE8) and channel 8N (PE9). The MPX2102A sensitivity when powered by 3.3 V is 3.3 V * 40 mV / 10 V = 13.2 mV/1000 mB = 13.2 microV/mB. To increase the sensitivity an external 45.1 gain is applied, using the TVS632 operational amplifier installed on the STM32373C-EVAL. The same operational amplifier is used to shift-down the input voltage by 3.3 V/10 = 0.33 V

Table 6. Pressure sensor voltage range

	Pressure (HPa)	Differential voltage on sensor outputs	Differential voltage on SDADC inputs
V_{DD} = 3.3V	800	10.56 mV	146.256 mV
	1000	13.2 mV	265.32 mV
	1200	15.84 mV	384.384 mV

Note: Refer to STM32373C-EVAL user manual for more details about how the MPX2102A is connected to PE8 and PE9

The SDADC channel 8 is configured in differential mode. The external reference VREF (set to 3.3 V on STM32373C-EVAL) is used as reference for SDADC. The conversion is triggered by the TIM19 timer with interrupt enabled on End of Injected Conversion.

The input voltage is calculated using the formula below:

inputvoltage = (InjectedConvData * (SDADC_VREF / (SDADC_RESOL * SDADC_GAIN))) + OFFSET_VOLTAGE;

Where:

InjectedConvData: The digital value read from SDADC data register

SDADC_VREF: is the sigma delta converter voltage reference: set externally to 3.3V

SDADC_RESOL: is the sigma delta converter resolution: 2e16-1

SDADC_GAIN: is the internal SDADC gain. In this example it is set to 4
OFFSET_VOLTAGE: The offset voltage added by the operational amplifier TVS632 (approximately 3.3 V/10 = 0.33 V)

And the pressure is calculated using the formula below:

PressuremB = ((1000000 * inputvoltage) / (MPX2102_SENSITIVITY * EXTERNGAIN));

4.3 Wave recorder

This application shows how to use the 16-bit Sigma-Delta Analog-to-Digital converter to record the human voice using the electric condenser microphone installed on the STM32373C-EVAL evaluation board.

The application source code is available in the

Project\STM32373C-EVAL\src\waverecorder.c

file in the STM32373C-EVAL demonstration firmware package *stm32373c-eval_fw*

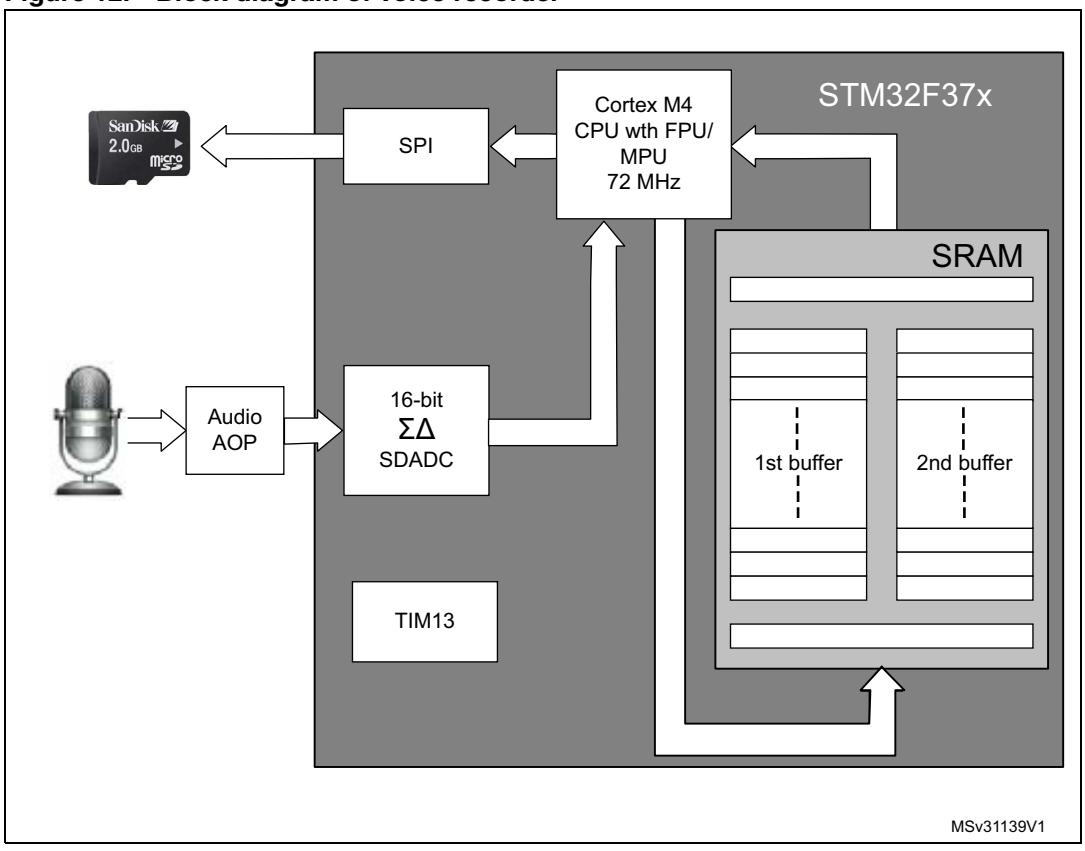
A microphone is connected to SDADC1 channel 6 (PB0) through an audio amplifier/filter. The SDADC is configured in Single-Ended Zero Reference mode and voice recording is triggered by TIM13 at a sampling rate of 8 KHz.

The wave recorder application uses a ping-pong buffer: one buffer is actively being written in the MicroSD memory card while the second buffer is filled with the new samples.

Writing access to the MicroSD memeory card uses the open source file system FatFS.

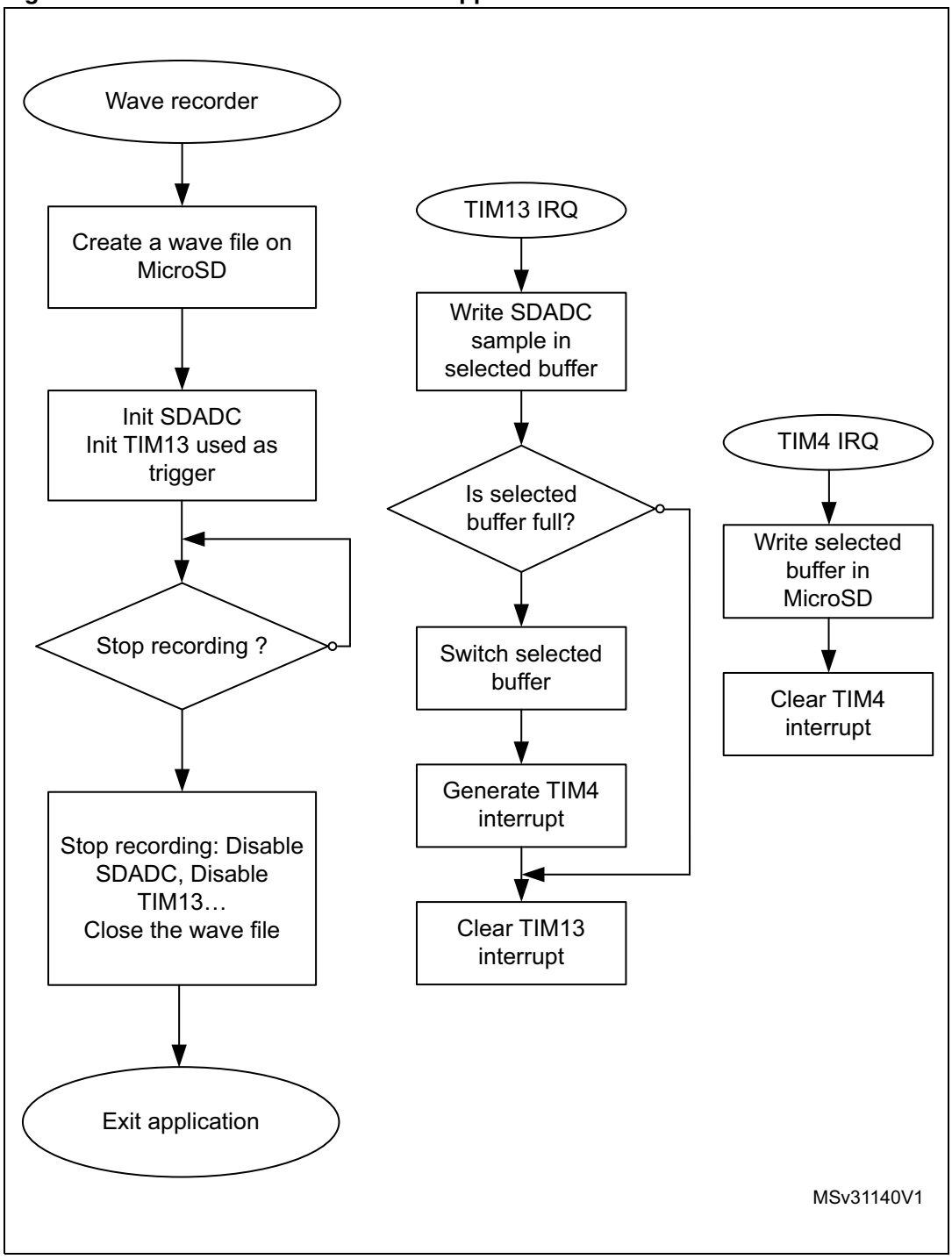
Figure 12 shows the block diagram of the voice recorder application.

Figure 12. Block diagram of voice recorder



The flowchart of this application is given in *Figure 13*.

Figure 13. Flowchart of wave recorder application



4.4 ElectroCardioGram (ECG) acquisition

This application shows how to use the 16-bit Sigma-Delta Analog-to-Digital converter to acquire a human ECG using two ECG electrodes TS1 and TS2 installed on the STM32373C-EVAL evaluation board.

The application source code is available in the

Project\STM32373C-EVAL\src\applications.c

file in the STM32373C-EVAL demonstration firmware package *stm32373c-eval_fw*

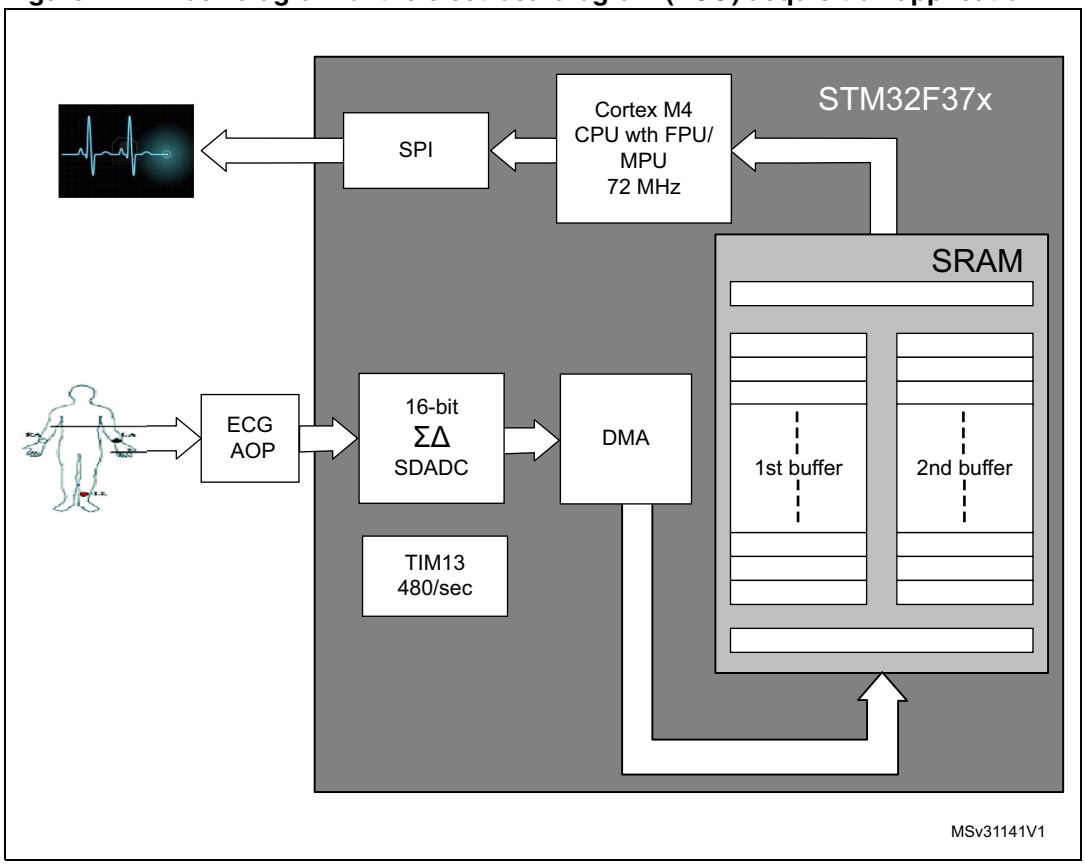
Two ECG electrodes TS1 and TS2 are connected to SDADC1 channel 0 (PE12) through an ECG amplifier/filter. The SDADC is configured in Single-Ended Zero Reference mode and conversion is triggered by the TIM3 timer at a sampling rate of 480 Hz.

The ECG acquisition application uses a ping-pong buffer: one buffer is actively being filtered (using a bandpass filter) and then displayed on the LCD while the second buffer is filled with the new ECG samples.

Note: ECG samples are filtered using the ARM DSP library

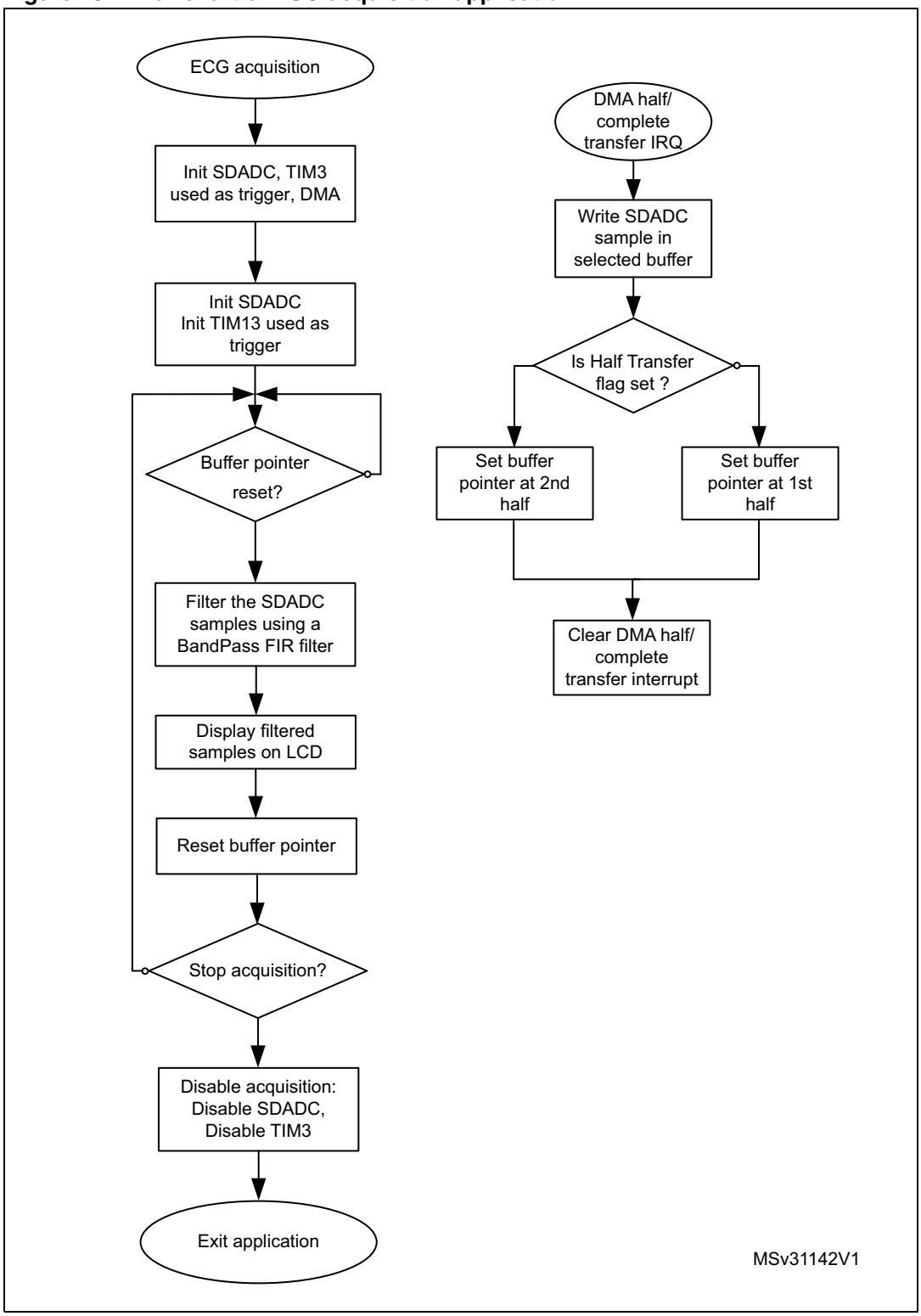
Figure 14 below shows the block diagram of the electrocardiogram acquisition application.

Figure 14. Block diagram of the electrocardiogram (ECG) acquisition application



The flowchart of this application is given in the figure below.

Figure 15. Flowchart of ECG acquisition application



4.5 Power meter application

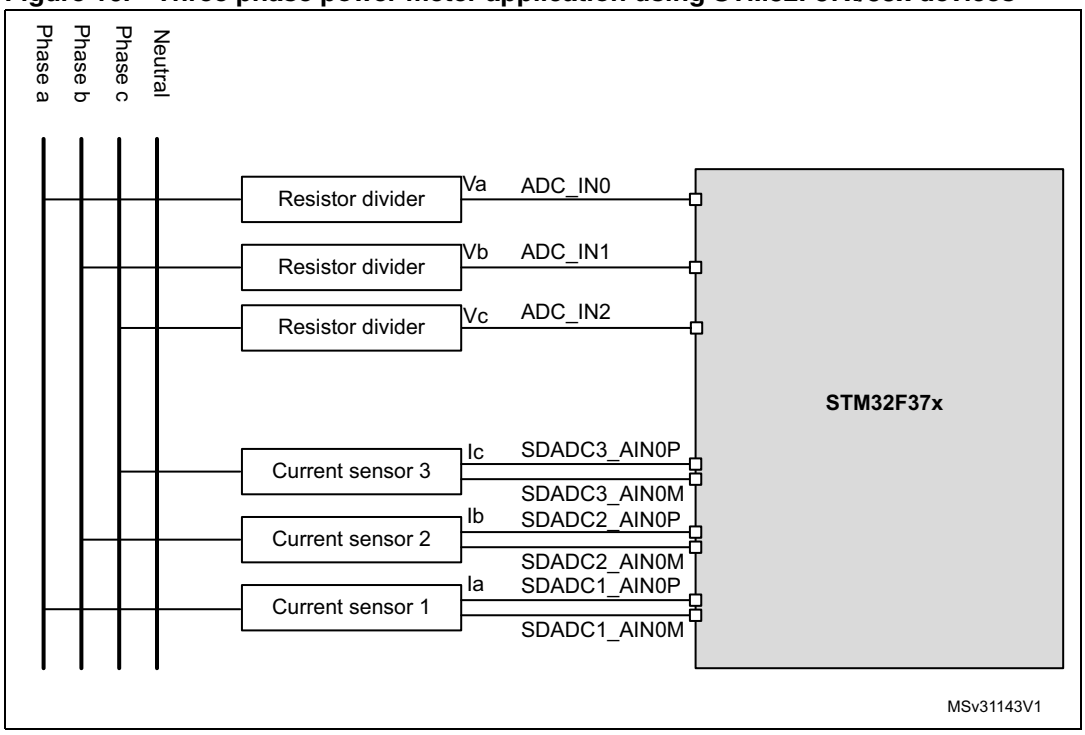
The analog to digital converter is the most important part of a power meter application and the SDADC embedded in STM32F37x/38x devices meets the requirements of this type of application. Typically a class B power meter requires 1.5% current measurement accuracy which means a 14-bit Effective Number Of Bits (ENOB) ADC.

For the voltage measurement there are no strict requirements and therefore the SAR ADC can be used for voltage measurement synchronized with the SDADC that is used for measuring the current.

Another constraining parameter of the Analog to Digital Converter is the sampling rate. For power meter applications, a sampling rate of up to 12.8 ksps is sufficient for harmonic spectrum analysis.

As shown in *Figure 16*, in the power meter application the phase measurement consists of measuring voltages: Va, Vb and Vc in single-ended mode using the SAR ADC while currents (Ia, Ib and Ic) are converted in differential mode using the SDADC. All are triggered by the same timer (for example TIM19).

Figure 16. Three phase power meter application using STM32F37x/38x devices



5 Revision history

Table 7. Document revision history

Date	Revision	Changes
13-Dec-2012	1	Initial release.