PETERMANN-TECHNIK GmbH
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HIGH TEMPERATURE LOW POWER OSCILLATOR

SERIES „HTLPO“ 1.0—110.0 MHz

FEATURES

+ 100% pin-to-pin drop-in replacement to quartz and MEMS based XO
+ High Temperature Low Power Oscillator for Low Cost
+ Excellent long time reliability-outperforms quartz-based XO
+ Operating temperature from -40°C to 125°C /-55°C to 125°C optional
+ Supply voltage of 1.8V, 2.5V to 3.3VDC
+ Excellent total frequency stability as low as ±20 ppm
+ LVCMOS/LVTTL compatible output
+ Express samples within 1 day ex works PETERMANN-TECHNIK
+ Pb-free, RoHS and REACH compliant / MSL1@260°C

APPLICATIONS

+ All high temperature applications for –40/+125°C (non AEQ-Q100 automotive and avionics)

GENERAL DATA[1,2]

PARAMETER AND CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
FREQUENCY RANGE						
Output Frequency Range	f	1	–	110	MHz	
FREQUENCY STABILITY AND AGING						
Frequency Stability	F_stab	-20	–	+20	PPM	Inclusive of initial tolerance at 25°C, 1st year aging at 25°C,
		-25	–	+25	PPM	and variations over operating temperature, rated power
		-30	–	+30	PPM	supply voltage and load (15 pF ± 10%).
		-50	–	+50	PPM	
OPERATING TEMPERATURE RANGE						
Operating Temperature Range	T_use	-40	–	+105	°C	
		-40	–	+125	°C	
Storage Temperature Range	T_stor	-55	–	+125	°C	Storage
SUPPLY VOLTAGE AND CURRENT CONSUMPTION						
Supply Voltage	V_{DD}	1.62	1.8	1.98	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.7	3.0	3.3	V	
		2.97	3.3	3.63	V	
		2.25	–	3.63	V	
Current Consumption	I_{DD}	–	3.8	4.5	mA	No load condition, f = 20 MHz, V_{DD}= 2.8V, 3.0V, or 3.3V
		–	3.6	4.2	mA	No load condition, f = 20 MHz, V_{DD} = 2.5V
		–	3.4	4	mA	No load condition, f = 20 MHz, V_{DD} = 1.8V
OE Disable Current	I_{OD}	–	–	4.1	mA	V_{DD} = 2.5V to 3.3V, OE = Low, output in high Z state
		–	–	3.8	mA	V_{DD} = 1.8V, OE = Low, output in high Z state
Standby Current	I_std	–	2.6	8.5	µA	V_{DD} = 2.8V to 3.3V, ST = Low, output is pulled down
		–	1.4	5.5	µA	V_{DD} = 2.5V, ST = Low, output is pulled down
		–	0.6	3.5	µA	V_{DD} = 1.8V, ST = Low, output is pulled down

Note: 1. All electrical specifications in the above table are specified with 15 pF output load at default drive strength and for all VDD(s) unless otherwise stated.
2.The typical value of any parameter in the Electrical Characteristic table is specified for the nominal value of the highest voltage option for that parameter and at 25 °C temperature.

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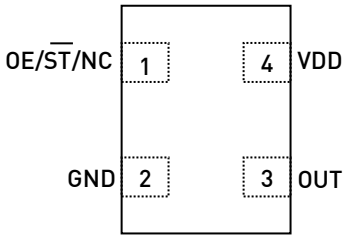
GENERAL DATA[1] (continued)

PARAMETER AND CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
LVCMOS OUTPUT CHARACTERISTICS						
Duty Cycle	DC	45	–	55	%	All V_{DDs}
Rise/Fall Time	Tr, Tf	–	1.0	2.0	ns	V_{DD} = 2.5V, 2.8V, 3.0V or 3.3V, 20% - 80%
		–	1.3	2.5	ns	V_{DD} =1.8V, 20% - 80%
		–	1.0	3.0	ns	V_{DD} = 2.25V - 3.63V, 20% - 80%
Output High Voltage	VOH	90%	–	–	V_{DD}	IOH = -4 mA (V_{DD} = 3.0V or 3.3V) IOH = -3 mA (V_{DD} = 2.8V and VDD= 2.5V) IOH = -2 mA (V_{DD}= 1.8V)
Output Low Voltage	VOL	–	–	10%	V_{DD}	IOL = 4 mA (V_{DD} = 3.0V or 3.3V) IOL = 3 mA (V_{DD}= 2.8V and VDD = 2.5V) IOL = 2 mA (V_{DD} = 1.8V)
INPUT CHARACTERISTICS						
Input High Voltage	VIH	70%	–	–	V_{DD}	Pin 1, OE or ST
Input Low Voltage	VIL	–	–	30%	V_{DD}	Pin 1, OE or ST
Input Pull-up Impedence	Z_in	50	87	150	kΩ	Pin 1, OE logic high or logic low, or ST logic high
		2	–	–	MΩ	Pin 1, ST logic low
STARTUP AND RESUME TIMING						
Startup Time	T_start	–	–	5	ms	Measured from the time V_{DD} reaches 90% of final value
Enable/Disable Time	T_oe	–	–	130	ns	f = 110 MHz. For other frequencies, T_oe = 100 ns + 3* clock periods
Resume Time	T_resume	–	–	5	ms	Measured from the time ST pin crosses 50% threshold
JITTER						
RMS Period Jitter	T_jitt	–	1.6	2.5	ps	f = 75 MHz, V_{DD} = 2.5V, 2.8V, 3.0V or 3.3V
		–	1.9	3	ps	f = 75 MHz, V_{DD} = 1.8V
Peak-to-peak Period Jitter	T_pk	–	12	20	ps	f = 75 MHz, V_{DD} = 2.5V, 2.8V, 3.0V or 3.3V
		–	14	30	ps	f = 75 MHz, V_{DD} = 1.8V
RMS Phase Jitter (random)	T_phj	–	0.5	0.8	ps	f = 75 MHz, Integration bandwidth = 900 kHz to 7.5 MHz
		–	1.3	2	ps	f = 75 MHz, Integration bandwidth = 12 kHz to 20 MHz
EXCELLENT RELIABILITY DATA						
MTBF				500 million hours		
Shock Resistance:				10.000 G		
Vibration Resistance:				70 g		

PIN DESCRIPTION

PIN	SYMBOL		FUNCTIONALITY
1	OE/ ST/NC	Output Enable	H[3]: specified frequency output L: output is high impedance. Only output driver is disabled.
		Standby	H[3]: specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std.
		No connect	Any voltage between 0 and V_{DD} or Open[3]: Specified frequency output. Pin 1 has no function.
2	GND	Power	Electrical ground[4]
3	OUT	Output	Oscillator output
4	V_{DD}	Power	Power supply voltage[4]

TOP VIEW



Note: 3. In OE or ST mode, a pull-up resistor of 10kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
4. A capacitor value of 0.1 µF between VDD and GND is required.

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TEST CIRCUIT AND WAVEFORM

FIGURE 1. TEST CIRCUIT

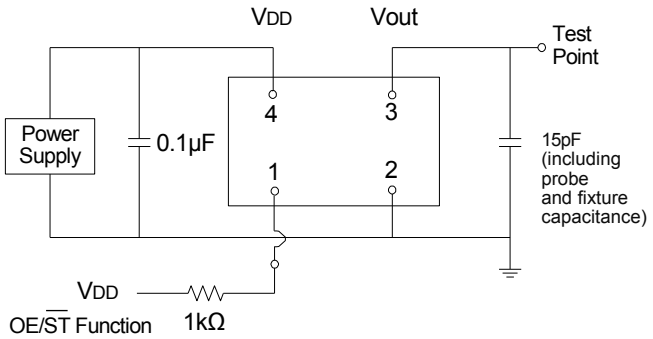
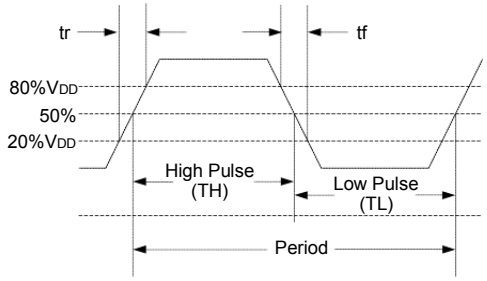
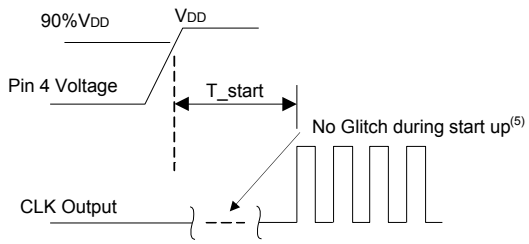


FIGURE 2. WAVEFORM



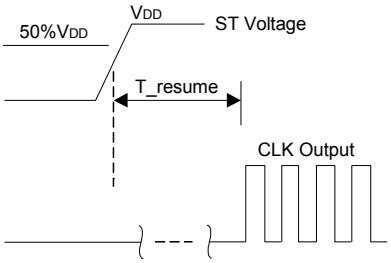
TIMING DIAGRAMS

FIGURE 3. STARTUP TIMING (OE/ST MODE)



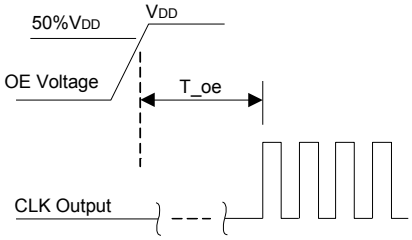
T_start: Time to start from power-off

FIGURE 4. STANDBY RESUME TIMING (ST MODE ONLY)



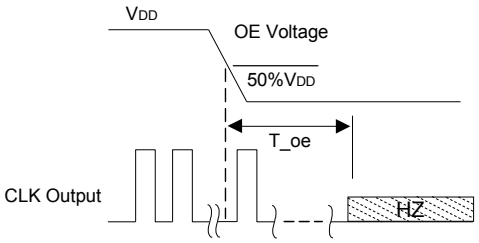
T_resume: Time to resume from ST

FIGURE 5. OE ENABLE TIMING (OE MODE ONLY)



T_OE: Time to re-enable the clock output

FIGURE 6. OE DISABLE TIMING (OE MODE ONLY)



T_OE: Time to put the output drive in High Z mode

Note: 5. HTLPO has "no runt" pulses and "no glitch" output during startup or resume.

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PROGRAMMABLE DRIVE STRENGTH

The HTLPO includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

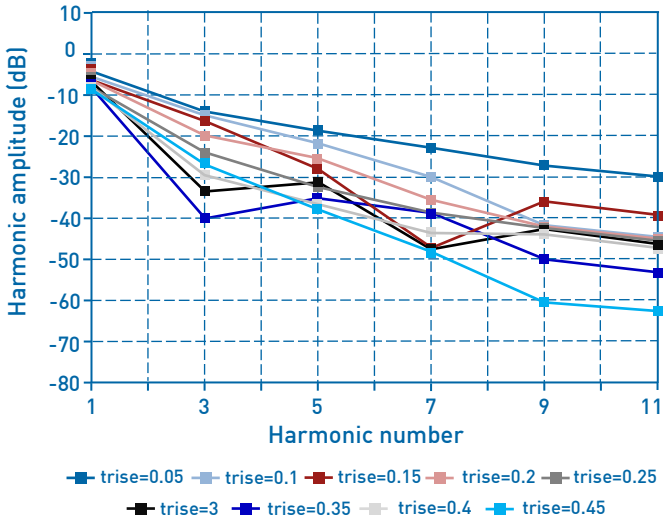
+ Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
+ Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
+ Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, please contact Petermann-Technik Application Engineers.

EMI REDUCTION BY SLOWING RISE/FALL TIME

Figure 7 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

FIGURE 7. HARMONIC EMI REDUCTION AS A FUNCTION OF SLOWER RISE/FALL TIME



JITTER REDUCTION WITH FASTER RISE/FALL TIME

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to increase rise/fall time (edge rate) of the input clock. Some chipsets would require faster rise/fall time in order to reduce their sensitivity to this type of jitter. The HTLPO provides up to 3 additional high drive strength settings for very fast rise/fall time. Refer to the Rise/Fall Time Tables to determine the proper drive strength.

HIGH OUTPUT LOAD CAPABILITY

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V HTLPO device with default drive strength setting, the typical rise/fall time is 1 ns for 15 pF output load. The typical rise/fall time slows down to 2.6 ns when the output load increases to 45 pF. One can choose to speed up the rise/fall time to 1.83ns by then increasing the drive strength setting on the HTLPO.

The HTLPO can support up to 60 pF or higher in maximum capacitive loads with drive strength settings. Refer to the Rise/Tall Time Tables (Table 1 to 5) to determine the proper drive strength for the desired combination of output load vs. rise/fall time.

HTLPO DRIVE STRENGTH SELECTION

Tables 1 through 5 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the HTLPO nominal supply voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V).
2. Select the capacitive load column that matches the application requirement (5 pF to 60 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

CALCULATING MAXIMUM FREQUENCY

Based on the rise and fall time data given in Tables 1 through 5, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

$$\text{Max. frequency} = \frac{1}{5 \times \text{Trf\_20/80}}$$

where Trf_20/80 is the typical value for 20%-80% rise/fall time.

EXAMPLE 1

Calculate f_{MAX} for the following condition:

+ V_{DD} = 1.8V (Table 1)
+ Capacitive Load: 30pF
+ Desired Tr/f time = 3 ns (rise/fall time part number code=E)

Part number for the above example:

HTLPO18-2520-E-25-Y-75.000MHz-T-S

Drive strength code is inserted here. Standard setting is "S"

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RISE/FALL TIME (20% TO 80%) vs C_{LOAD}

TABLE 1. VDD = 1.8V RISE/FALL TIMES FOR SPECIFIC C_{LOAD}

RISE/FALL TIME TYP (NS)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	6.16	11.61	22.00	31.27	39.91
A	3.19	6.35	11.00	16.01	21.52
R	2.11	4.31	7.65	10.77	14.47
B	1.65	3.23	5.79	8.18	11.08
T	0.93	1.91	3.32	4.66	6.48
E	0.78	1.66	2.94	4.09	5.74
U	0.70	1.48	2.64	3.68	5.09
S for standard	0.65	1.30	2.40	3.35	4.56

TABLE 2. VDD = 2.5V RISE/FALL TIMES FOR SPECIFIC C_{LOAD}

RISE/FALL TIME TYP (NS)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	4.13	8.25	12.82	21.45	27.79
A	2.11	4.27	7.64	11.20	14.49
R	1.45	2.81	5.16	7.65	9.88
B	1.09	2.20	3.88	5.86	7.57
T	0.62	1.28	2.27	3.51	4.45
S for standard	0.54	1.00	2.01	3.10	4.01
U	0.43	0.96	1.81	2.79	3.65
F	0.34	0.88	1.64	2.54	3.32

TABLE 3. VDD = 2.8V RISE/FALL TIMES FOR SPECIFIC C_{LOAD}

RISE/FALL TIME TYP (NS)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	3.77	7.54	12.28	19.57	25.27
A	1.94	3.90	7.03	10.24	13.34
R	1.29	2.57	4.72	7.01	9.06
B	0.97	2.00	3.54	5.43	6.93
T	0.55	1.12	2.08	3.22	4.08
S for standard	0.44	1.00	1.83	2.82	3.67
U	0.34	0.88	1.64	2.52	3.30
F	0.29	0.81	1.48	2.29	2.99

TABLE 4. VDD = 3.0V RISE/FALL TIMES FOR SPECIFIC C_{LOAD}

RISE/FALL TIME TYP (NS)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	3.60	7.21	11.97	18.74	24.30
A	1.84	3.71	6.72	9.86	12.68
R	1.22	2.46	4.54	6.76	8.62
B	0.89	1.92	3.39	5.20	6.64
S for standard	0.51	1.00	1.97	3.07	3.90
E	0.38	0.92	1.72	2.71	3.51
U	0.30	0.83	1.55	2.40	3.13
F	0.27	0.76	1.39	2.16	2.85

TABLE 5. VDD = 3.3V RISE/FALL TIMES FOR SPECIFIC C_{LOAD}

RISE/FALL TIME TYP (NS)					
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF	45 pF	60 pF
L	3.39	6.88	11.63	17.56	23.59
A	1.74	3.50	6.38	8.98	12.19
R	1.16	2.33	4.29	6.04	8.34
B	0.81	1.82	3.22	4.52	6.33
S for standard	0.46	1.00	1.86	2.60	3.84
E	0.33	0.87	1.64	2.30	3.35
U	0.28	0.79	1.46	2.05	2.93
F	0.25	0.72	1.31	1.83	2.61

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PROGRAMMABLE DRIVE STRENGTH

PIN 1 CONFIGURATION OPTIONS (OE, ST, OR NC)

Pin 1 of the HTLPO can be programmed to support three modes: Output enable (OE), standby (ST) or No Connect (NC).

OUTPUT ENABLE (OE) MODE

In the OE mode, applying logic Low to the OE pin only disables the output driver and puts it in Hi-Z mode. The core of the device continues to operate normally. Power consumption is reduced due to the inactivity of the output. When the OE pin is pulled High, the output is typically enabled in <1µs.

STANDBY (ST) MODE

In the ST mode, a device enters into the standby mode when Pin 1 pulled low. All internal circuits of the device are turned off. The current is reduced to a standby current, typically in the range of a few µA. When ST is pulled High, the device goes through the „resume" process, which can take up to 5 ms.

NO CONNECT (NC) MODE

In the NC mode, the device always operates in its normal mode and output the specified frequency regardless of the logic level on pin 1. Table 6 below summarizes the key relevant parameters in the operation of the device in OE, ST, or NC mode.

TABLE 6. OE vs. ST vs. NC

	OE	ST	NC
Active current 125 MHz (max, 1.8V)	4 mA	4 mA	4 mA
OE disable current (max. 1.8V)	3.8 mA	N/A	N/A
Standby current (typical 1.8V)	N/A	0.6 uA	N/A
OE enable time at 125 MHz (max)	162 ns	N/A	N/A
Resume time from standby (max, all frequency)	N/A	5 ms	N/A
Output driver in OE disable/ standby mode	High Z	pull-down	N/A

OUTPUT ON STARTUP AND RESUME

The HTLPO comes with gated output. Its clock output is accurate to the rated frequency stability within the first pulse from initial device startup or resume from the standby mode.

In addition, the HTLPO has NO RUNT, NO GLITCH output during startup or resume as shown in the waveform captures in Figure 8 and Figure 9.

FIGURE 8. STARTUP WAVEFORM vs. VDD

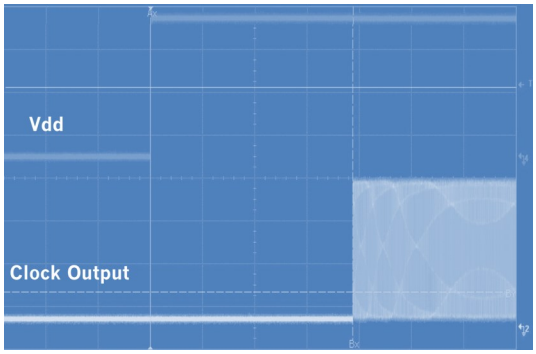
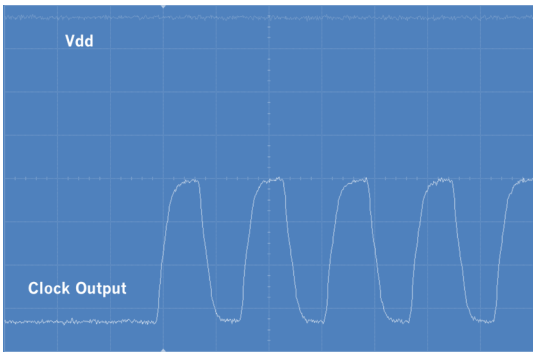


FIGURE 9. STARTUP WAVEFORM vs. VDD (ZOOMED-IN VIEW OF FIGURE 8)



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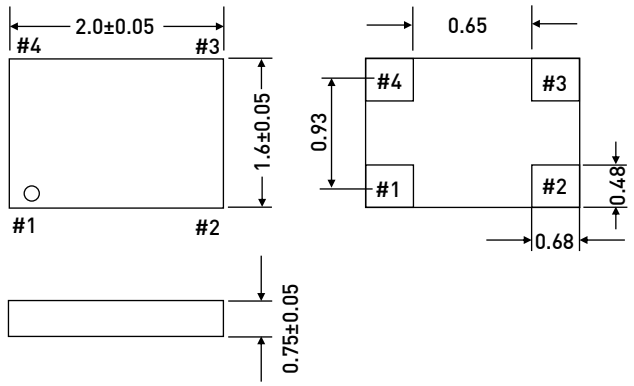
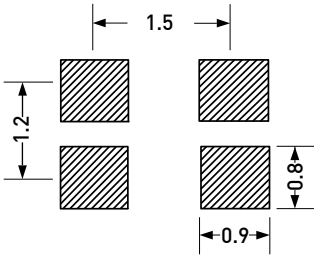
DIMENSIONS AND PATTERNS

PACKAGE SIZE – DIMENSIONS (UNIT:MM)

2.0 X 1.6 X 0.75 MM

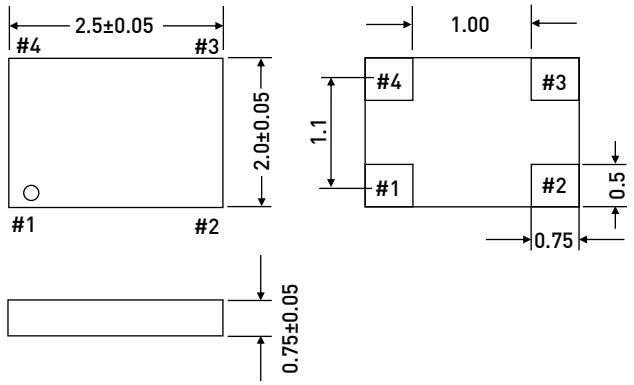


RECOMMENDED LAND PATTERN (UNIT:MM) [6]

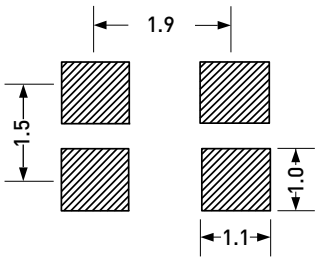


PACKAGE SIZE – DIMENSIONS (UNIT:MM)

2.5 X 2.0 X 0.75 MM

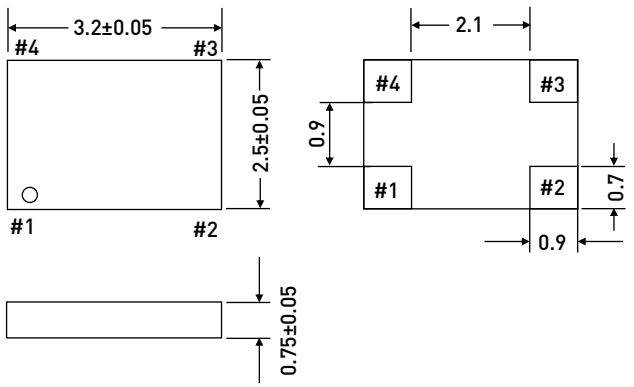


RECOMMENDED LAND PATTERN (UNIT:MM)

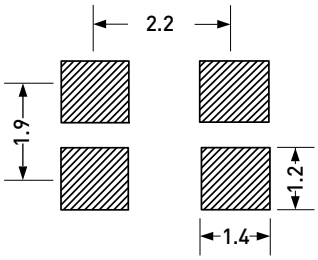


PACKAGE SIZE – DIMENSIONS (UNIT:MM)

3.2 X 2.5 X 0.75 MM



RECOMMENDED LAND PATTERN (UNIT:MM)



Note: 6. A capacitor value of 0.1 µF between VDD and GND is recommended.

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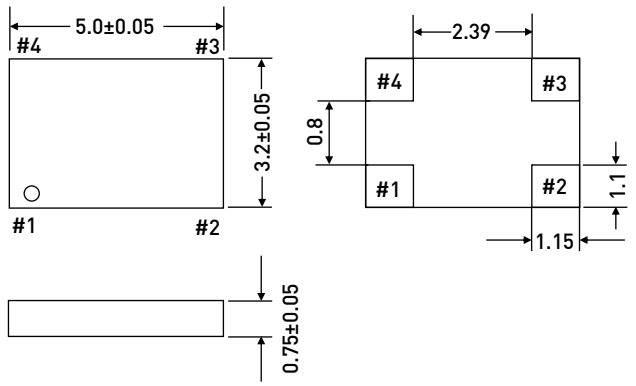
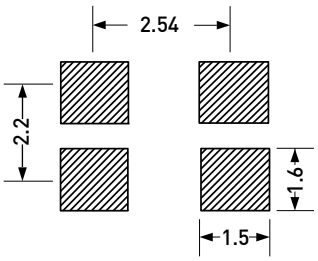
DIMENSIONS AND PATTERNS

PACKAGE SIZE – DIMENSIONS (UNIT:MM)

5.0 X 3.2 X 0.75 MM

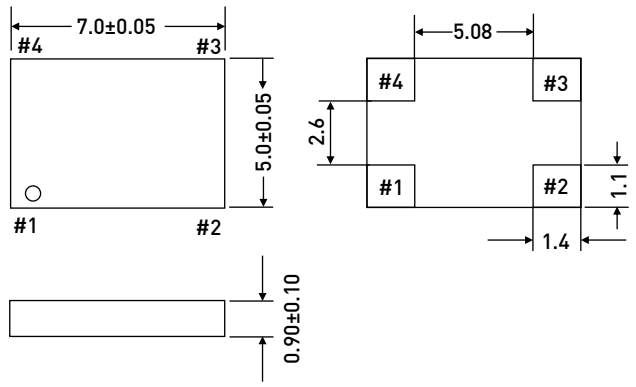


RECOMMENDED LAND PATTERN (UNIT:MM) [7]

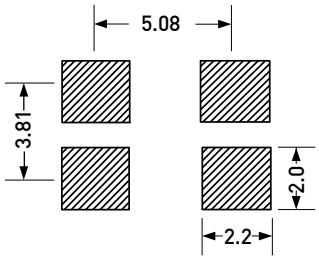


PACKAGE SIZE – DIMENSIONS (UNIT:MM)

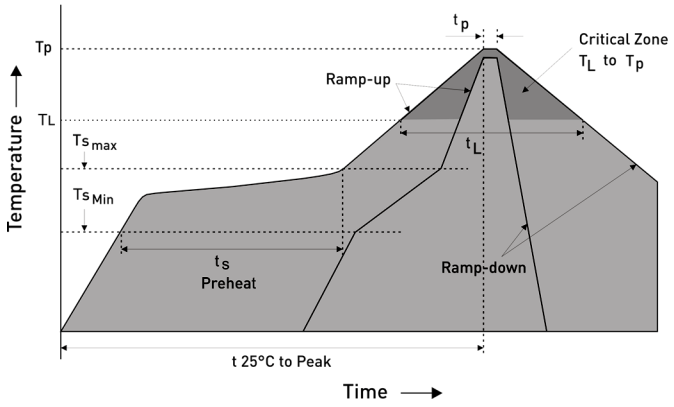
7.0 X 5.0 X 0.90 MM



RECOMMENDED LAND PATTERN (UNIT:MM)



REFLOW SOLDER PROFILE



Profile Feature	Pb-Free Assembly
Average ramp-up rate (TL to TP)	3°C/second max.
Preheat:	
Temperature Min (Tsmin)	150°C
Temperature Max (Tsmax)	200°C
Time (min to max) (ts)	60-180 seconds
Time maintained above:	
Temperature (TL)	217°C
Time (tL)	60-150 seconds
Peak/Classification Temperature (Tp)	240°C
Time within 5°C of actual Peak Temperature (tp)	20-40 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

Note: 7. A capacitor value of 0.1 µF between VDD and GND is recommended.

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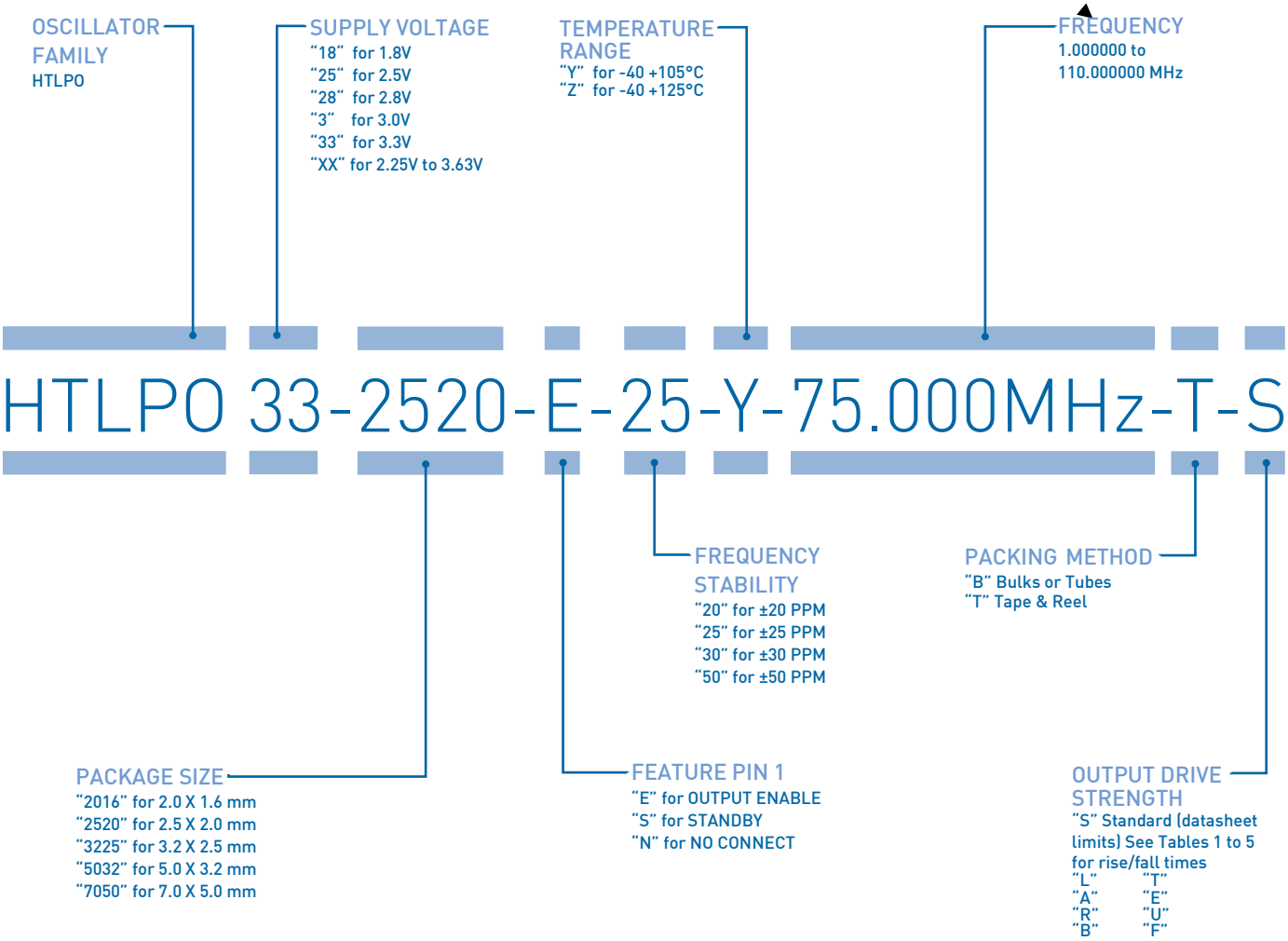
ORDERING INFORMATION



EXAMPLE: HTLPO33-2520-E-25-Y-75.000MHz-T-S

PLEASE INDICATE YOUR REQUIRED PARAMETERS

SAMPLES ARE AVAILABLE WITHIN A SHORT DELIVERY PERIOD!

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PREMIUM QUALITY BY PETERMANN-TECHNIK

DMSZ certified according to ISO 9001 QM 00886

OUR COMPANY IS CERTIFIED ACCORDING TO ISO 9001:2008 IN OCTOBER 2013 BY THE DMSZ CERTIFIKATION GMBH.

THIS IS FOR YOU TO ENSURE THAT THE PRINCIPLES OF QUALITY MANAGEMENT ARE FULLY IMPLEMENTED IN OUR QUALITY MANAGEMENT SYSTEM AND QUALITY CONTROL METHODS ALSO DOMINATE OUR QUALITY STANDARDS.