

TOPAZ SEMICONDUCTOR

2N7104, 2N7105, 2N7106 2N7107, 2N7108, 2N7109

N-CHANNEL ENHANCEMENT-MODE D-MOS FET SWITCHES

ORDERING INFORMATION

TO-206AF (TO-72) PACKAGE SHORTING RINGS ON LEADS		2N7104	2N7105+	2N7106	2N7107+	2N7108	2N7109+
Sorted chips in Waffle Pack		SD210CHP	SD211CHP	SD212CHP	SD213CHP	SD214CHP	SD215CHP
DESCRIPTION	BV _{DS} min.	30V	30V	10V	10V	20V	20V
	BV _{SD} min.	10V	10V	10V	10V	20V	20V
	r _{DS(on)} MAX.	70 ohms	70 ohms	70 ohms	70 ohms	70 ohms	70 ohms

+ Gate Protective Diode

FEATURES

- High Input to Output Isolation—120dB typical
- Low feedthrough and feedback transients
- Low inter-electrode Capacitances

APPLICATIONS

- +30V Switch Drivers—2N7104, 2N7105
- ±10V Analog Switches—2N7108, 2N7109
- ±5V Analog Switches—2N7106, 2N7107

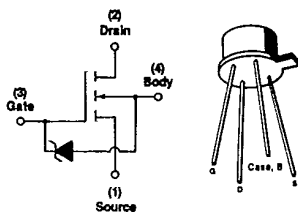
ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

PARAMETER	2N 7104	2N 7105	2N 7106	2N 7107	2N 7108	2N 7109	UNIT
Breakdown Voltages							
V _{DS}	+30	+30	+10	+10	+20	+20	V
V _{SD}	+10	+10	+10	+10	+20	+20	V
V _{DB}	+30	+30	+15	+15	+25	+25	V
V _{SB}	+15	+15	+15	+15	+25	+25	V
V _{GS}	±40*	-15	±40*	-15	±40*	-25	V
		+25		+25		+30	V
V _{GB}	±40	-0.3	±40	-0.3	±40	-0.3	V
		+25		+25		+30	V
V _{GD}	±40	-30	±40	-15	±40	-25	V
		+25		+25		+30	V
V _{DG}	+40*	+25*	+40*	+25*	+40*	+30*	V

I _D	Continuous Drain Current	50mA*
P _T	Power Dissipation (at or below T _C = +25°C)	1.2W
	Linear Derating Factor	12mW/°C
P _D	Power Dissipation (at or below T _A = +25°C)	300mW*
	Linear Derating Factor	2.4 mW/°C*
T _J	Operating Junction Temperature Range	-55 to +150°C*
T _S	Storage Temperature Range	-65 to +200°C
T _L	Lead Temperature (1/16" from mounting surface for 10 sec)	+300°C

*JEDEC Registered Value

SCHEMATIC DIAGRAM



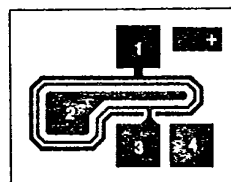
Body Internally connected to Case.
Diode protection on 2N7105/2N7107/2N7109

PACKAGE DIMENSIONS

TO-72

(See Package 3)

CHIP CONFIGURATION



PAD

- 1 — Source
- 2 — Drain
- 3 — Gate
- 4 — Diode

For SD211/213/215 CHP, bond Gate and Diode to common point. Body is backside contact.
Dimensions: .022x.025x.013 Inches

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 2N7107, 2N7108, 2N7109**
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

7-35-25

#	PARAMETER	2N7104, 2N7105			2N7106, 2N7107			2N7108, 2N7109			UNIT	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
1	BV _{DS} Drain-Source Breakdown Voltage	30	35								V	I _D = 10 μ A V _{GS} = V _{BS} = 0
2		10	25		10	25		20	25			I _D = 10nA V _{GS} = V _{BS} = -5V
3	I _{OSS} Zero Gate Voltage Drain Current			10*							μ A	V _{DS} = 30V V _{GS} = V _{BS} = 0
4	BV _{SD} Source-Drain Breakdown Voltage	10			10			20			V	I _S = 10nA V _{GD} = V _{BD} = -5.0V
5	BV _{DS} Drain-Substrate Breakdown Voltage	15			15			25				I _D = 10nA, V _{GS} = 0 Source OPEN
6	BV _{SB} Source-Substrate Breakdown Voltage	15			15			25				I _S = 10 μ A, V _{GS} = 0 Drain OPEN
7	I _{D (off)} Drain-Source OFF Current			10*			10*				nA	V _{DS} = 10V V _{GS} = V _{BS} = -5V
8										10*	μ A	V _{DS} = 20V V _{GS} = V _{BS} = -5V
9				5.0*			5.0*					V _{DS} = 10V V _{GS} = V _{BS} = -5V
10	I _{S (off)} Source-Drain OFF Current									5.0*	μ A	T _A = +125°C
11				10*			10*					V _{SD} = 10V V _{GD} = V _{BD} = -5V
12										10*	nA	V _{SD} = 20V V _{GD} = V _{BD} = -5V
13	I _{S (off)} Source-Drain OFF Current			5.0*			5.0*				μ A	V _{SD} = 10V V _{GD} = V _{BD} = -5V
14										5.0*		T _A = +125°C
15												
16	I _{GSS} Gate Reverse Current	2N7104		0.1*							nA	V _{GS} = 12V
17		2N7106					0.1*					V _{DS} = V _{BS} = 0
18		2N7108								0.1*		
19		2N7105		1.0*							μ A	V _{GS} = 25V
20		2N7107				1.0*						V _{GS} = 30V
21		2N7109						1.0*				
22		2N7104		1.0*							μ A	V _{GS} = 12V
23		2N7106				1.0*						V _{DS} = V _{BS} = 0
24		2N7108								1.0*		
25		2N7105		100*								T _A = +125°C
26		2N7107				100*						
27	V _{GS(th)} Gate Threshold Voltage	0.5*	1.0	2.0*	0.1*	1.0	2.0*	0.1*	1.0	2.0*	V	V _{DS} = V _{GS} , I _D = 1 μ A, V _{SB} = 0
28	r _{DS(on)} Drain-Source ON Resistance		50	70*		50	70*		50	70*	ohms	V _{GS} = 5V I _D = 1mA
29			30	45		30	45		30	45		V _{GS} = 10V V _{SB} = 0

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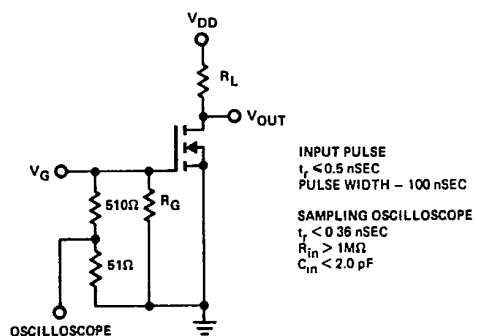
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ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted), continued

T-35-25

#	PARAMETER		2N7104, 2N7105			2N7106, 2N7107			2N7108, 2N7109			UNIT	TEST CONDITIONS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
30	DYNAMIC	g_{fs} Common-Source Forward Transcond.	10	12		10	12		10	12		mmhos	$V_{DS} = 10V$, $I_D = 20mA$, $f = 1KHz$, $V_{SB} = 0$
31		C_{iss} Input Capacitance		2.4	3.5*		2.4	3.5*		2.4	3.5	pF	$V_{DS} = 10V$ $V_{GS} = V_{BS} = -15V$ $f = 1MHz$
32		$C_{igd + db}$ Drain Node Capacitance		1.3	1.5		1.3	1.5		1.3	1.5		
33		$C_{igs + sb}$ Source Node Capacitance		3.5	4.0		3.5	4.0		3.5	4.0		
34		C_{rss} Reverse Transfer Capacitance		0.3	0.5*		0.3	0.5*		0.3	0.5*		
35		$t_{d(on)}$ Turn ON Delay Time		0.7	1.0*		0.7	1.0*		0.7	1.0*	nSec	$V_{DD} = 5V$, $V_{G(on)} = 5V$ $R_L = 680\Omega$, $R_G = 51\Omega$
36		t_r Rise Time		0.8	1.0*		0.8	1.0*		0.8	1.0*		
37	t_{off} Turn OFF Time		10			10			10				

*JEDEC Registered Value

SWITCHING TIMES TEST CIRCUIT

TEST WAVEFORMS
