Data Sheet No. PD-3.082

INTERNATIONAL RECTIFIER IOR

T-25-17

2N1792, 2N1805, 2N1909, 2N2023 SERIES

110 Amp RMS SCRs

A

Major Ratings and Characteristics

	2N1792 thru 2N1804	2N1909 thru 2N1916 2N1805 thru 2N1807	2N2023 thru 2N2030	Units
$I_{T(RMS)}$	110	110	110	A
$I_{T(AV)}$	70*	70*	70*	A
@ T_C	65*	62*	85*	°C
I_{TSM} @ 50 Hz	955	955	955	A
@ 60 Hz	1,000*	1,000*	1,000*	
I^2t @ 50 Hz	4,550	4,550	4,550	A^2s
@ 60 Hz	4,150	4,150	4,150	
I_{GT}	70	70	70	mA
dv/dt	200	200	50	V/µs
di/dt	100	100	100	A/µs
T_J	-65* to 125*	-40* to 125*	-65* to 150*	°C
V_{RRM}, V_{DRM} range	50* to 1,200*	25* to 840*	25* to 400*	V

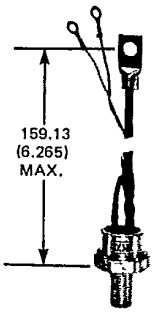
*JEDEC registered values

Description/Features

- For general purpose phase control applications
- Forward and reverse voltage ratings up to 1200V
- High temperature series
- High surge rating
- Standard 1/2" – 20 stud
- Can be supplied as JAN and JAN-TX devices in accordance with MIL-S-19500/203 or MIL-S-19500/204.

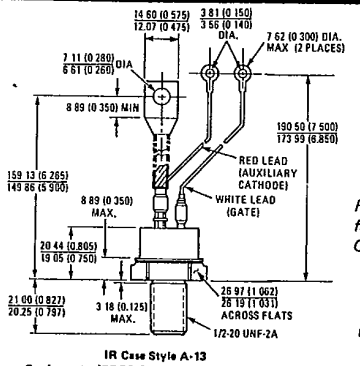
*JEDEC registered values.

CASE STYLE AND DIMENSIONS



Case style (ceramic) A-11 furnished when part is rated 1000V or higher. A-13 (glass) for parts below 1000V.

JAN and/or JAN/TX types available.



IR Case Style A-13
Conforms to JEDEC Outline TO-209AC (TO-94)

Refer to Page A-34 for flag terminal Case Style

All Dimensions in Millimeters and (Inches)

VOLTAGE RATINGS (Applied gate voltage zero or negative)

Part Numbers			V_{RRM} – Max. Repetitive Peak Reverse Voltage (V)	V_{DRM} – Max. Repetitive Peak Off-State Voltage (V) ①	V_{RSM} – Max. Non-Repetitive Peak Reverse Voltage $t_p \leq 5$ ms (V)
TO-208AD Case	TO-209AC Case	TO-209AC Case	T_J = –40°C to 125°C	T_J = –40°C to 125°C	T_J = 25°C to 125°C
–	2N1909	2N2023	25*	25*	35*
2N1792	2N1910	2N2024	50*	50*	70*
2N1793	2N1911	2N2025	100*	100*	150*
2N1794	2N1912	2N2026	150*	150*	225*
2N1795	2N1913	2N2027	200*	200*	300*
2N1796	2N1914	2N2028	250*	250*	350*
2N1797	2N1915	2N2029	300*	300*	400*
2N1798	2N1916	2N2030	400*	400*	500*
2N1799	2N1805	–	600*	500*	625*
2N1800	2N1806	–	720*	600*	750*
2N1801	2N1807	–	840*	700*	880*
2N1802	–	–	960*	800*	1000*
2N1803	–	–	1080*	900*	1130*
2N1804	–	–	1200*	1000*	1250*

ELECTRICAL SPECIFICATIONS

		2N1792 to 2N1804	2N1909-16 2N1805-07	2N2023-30	Units	Conditions
	ON-STATE					
$I_{T(RMS)}$	Max. RMS on-state current	110	110	110	A	
$I_{T(AV)}$	Max. average on-state current @ Max. T_C =	70*	70*	70*	A	180° half sine wave condition.
		65*	62*	85*	°C	
I_{TSM}	Max. peak one cycle, non-repetitive surge current	955	955	955	A	50 Hz half cycle sine wave or 6 ms rectangular pulse — Following any rated load condition, and with rated V_{RRM} applied
		1000*	1000*	1000*		60 Hz half cycle sine wave or 5 ms rectangular pulse — following surge. SCR turned fully on.
		1150	1150	1150	A	50 Hz half cycle sine wave or 6 ms rectangular pulse — Same conditions as above except with V_{RRM} applied following
		1200	1200	1200		60 Hz half cycle sine wave or 5 ms rectangular pulse — surge = 0.
I^2t	Max. I^2t capability, for fusing	4550	4550	4550	A^2s	t = 10 ms — Rated V_{RRM} applied following surge,
		4150	4150	4150		t = 8.3 ms — initial T_J = max. rated
I^2t	Max. I^2t capability, for individual device fusing	6450	6450	6450	A^2s	t = 10 ms — V_{RRM} = 0 following surge,
		5900	5900	5900		t = 8.3 ms — initial T_J = max. rated
$I^2\sqrt{t}$	Max. $I^2\sqrt{t}$ capability, for individual device fusing ②	64 500	64 500	64 500	$A^2\sqrt{s}$	t = 0.1 to 10 ms, V_{RRM} following surge = 0, initial T_J = max. rated
V_{TM}	Max. peak on-state voltage	1.85*	1.85*	1.9*	V	T_J = 25°C, $I_{T(AV)}$ = 70A (220A peak)
		2.0*	–	–		T_J = 25°C, $I_{T(AV)}$ = 70A (220A peak) 2N1803 & 2N1804 only
I_H	Typical holding current.	20	20	20	mA	T_C = 25°C, anode supply = 22V, initial I_T = 2A.

*JEDEC registered values.

① Units may be broken over non-repetitively without damage if di/dt does not exceed 20 A/μs.

② I^2t for time $t_x = I^2\sqrt{t}\ \sqrt{t_x}$.

ELECTRICAL SPECIFICATIONS (Continued)

		2N1792 to 2N1804	2N1909-16 2N1805-07	2N2023-30	Units	Conditions
	BLOCKING					
dv/dt	Min. critical rate-of-rise of off-state voltage	200	200	50	V/μs	T_J = 125°C Exponential to 100% rated V_{DRM}. Gate open circuit. T_J = 150°C for 2N2023-30.
$I_{R(AV)}$ & $I_{D(AV)}$	Max. average reverse and off-state current V_{RRM} & V_{DRM} = 25V to 150V	6.5*	6.5*	6.5*		At rated V_{RRM}, V_{DRM}, T_J = max. rated, gate open circuited.
	= 200V	6.0*	6.5*	6.0*		
	= 250V	5.5*	5.5*	5.5*		
	= 300V	5.0*	5.0*	5.0*		
	= 400V	4.0*	4.0*	4.0*		
	= 500V to 600V	3.3*③	3.3*③	–		
	= 700V to 800V	3.0*③	3.0*③	–		
	= 900V to 1200V	2.7*③	–	–		
	SWITCHING					
t_d	Typical delay time	1	1	1	μs	T_C = 25°C, V_{DM} = rated V_{DRM}, I_{TM} = 50A dc resistive circuit. Gate pulse: 10V, 25Ω source, t_p = 6μs, t_r = 0.1μs
t_r	Typical rise time	1.5	1.5	1.5		
t_q	Typical turn-off time	40	40	40 (70 @ 150°C)	μs	T_C = 125°C, I_{TM} = 50A, commutating di/dt = –5 A/μs, min. V_R during turn-off interval = 50V, dv/dt = 20 V/μs linear to rated V_{DRM}.
di/dt	Max. non-repetitive rate-of-rise of turned-on current V_{DRM} = 25V to 600V	100	100	100	A/μs	T_C = 125°C, V_{DM} = rated V_{DRM} I_{TM} = (2 x rated di/dt) A Gate pulse: 20V, 15Ω, $t_p \geq 6\mu s$, t_r = 0.1 μs Per JEDEC Standard RS-297, 5.2.2.6.
	= 700V to 1200V	75	75	75		
	TRIGGERING					
P_{GM}	Max. peak gate power	5*	5*	5*	W	t_p = 5 ms max.
$P_{G(AV)}$	Max. average gate power	0.5*	0.5*	0.5*	W	
$+I_{GM}$	Max. peak positive gate current	2*	2*	2*	A	
$+V_{GM}$	Max. peak positive gate voltage	10*	10*	10*	V	
$-V_{GM}$	Max. peak negative gate voltage	5*	5*	5*	V	
I_{GT}	Max. required DC gate current to trigger	130* ④	130*	150* @ –65°C	mA	T_C = –40°C. Max. required gate trigger current is the lowest value which will trigger all units with +6V anode-to-cathode.
		70④	70	70		T_C = 25°C
		40④	40	–		T_C = 125°C
		–	–	35		T_C = 150°C
	Typical DC gate current to trigger	35	35	35		T_C = 25°C +6V anode-to-cathode

*JEDEC registered values.
③ V_{RRM} 20% greater than V_{DRM}.
④ For 2N1803, 1804: I_{GT} = 200 mA* @ –40°C; 110mA @ 25°C; 50 mA @ 125°C.

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2N1792, 2N1805, 2N1909, 2N2023 Series

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ELECTRICAL SPECIFICATIONS (Continued)

		2N1792 to 2N1804	2N1909-16 2N1805-07	2N2023-30	Units	Conditions
	TRIGGERING (Cont.)					
V_{GT}	Max. required DC gate voltage to trigger	–	–	3*	V	T_C = –65°C. Max. required gate trigger voltage is the lowest value which will trigger all units with +6V anode-to-cathode.
		3*	3*	–		T_C = –40°C
		2.5	2.5	2.0		T_C = 25°C
	Typical DC gate voltage to trigger	1.2	1.2	1.2		T_C = 25°C +6V anode-to-cathode
V_{GD}	Max. DC gate voltage not to trigger	0.25*	0.25*	0.25* @ 150°C	V	T_C = 125°C. Max. gate voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode-to-cathode.

THERMAL-MECHANICAL SPECIFICATIONS

T_J	Operating junction temperature range	–65* to 125*	–40* to 125*	–65* to 150*	°C	
T_{stg}	Storage temperature range	–40* to 150*	–40* to 125*	–65* to 150*	°C	
R_{thJC}	Max. internal thermal resistance, junction-to-case	0.4* ⑥	0.4*	0.4*	deg. C/W	DC operation
R_{thCS}	Thermal resistance, case-to-sink	0.1	0.1	0.1	deg. C/W	Mounting surface smooth, flat and greased.
T	Mounting torque Min.	14.5 (125)			N•m	Non-lubricated threads
	Max.	17 (150)			(lbf•in)	
	Max. torque on screw in flagterminal	1.4 (12)	–	–	N•m (lbf•in)	Non-lubricated threads TO-208AD (TO-83) only
wt	Approximate weight	100 (3.5)			g (oz)	
	Case style	21N1805-07; 2N1909-16; 2N2023-30; TO-209AC (TO-94) (A-13)				JEDEC
		2N1792-1804; TO-208AD (TO-83) (A-14)				JEDEC

*JEDEC registered values.
⑥2N1803, 2N1804: R_{thJC} = 0.35 deg. C/W.

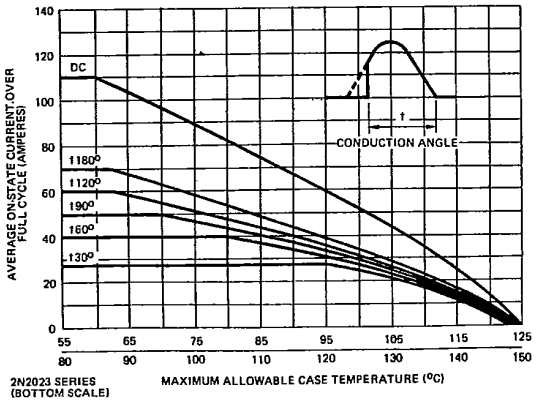

Fig. 1 — On-State Current Vs. Case Temperature (Sinusoidal Current Waveform, 50 to 400 Hz)

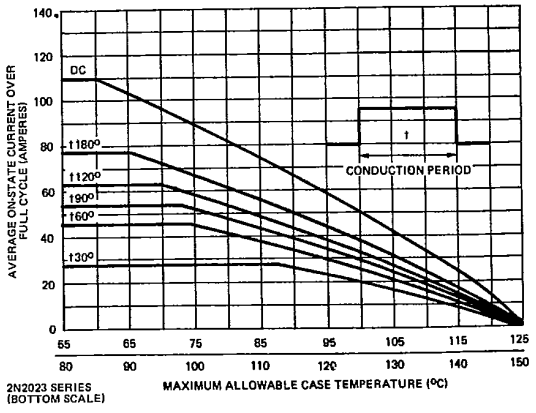

Fig. 2 — On-State Current Vs. Case Temperature (Rectangular Current Waveform, 50 to 400 Hz)

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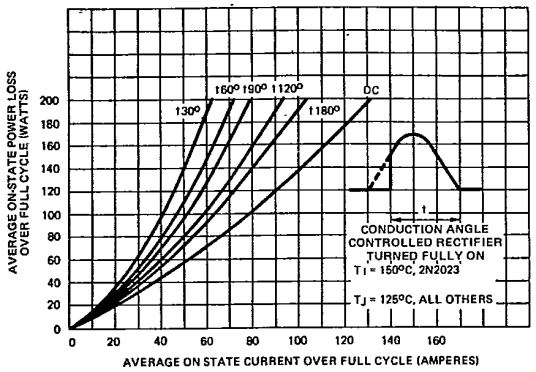


Fig. 3 – Maximum Low-Level On-State Power Loss Vs. Current (Sinusoidal Current Waveform)

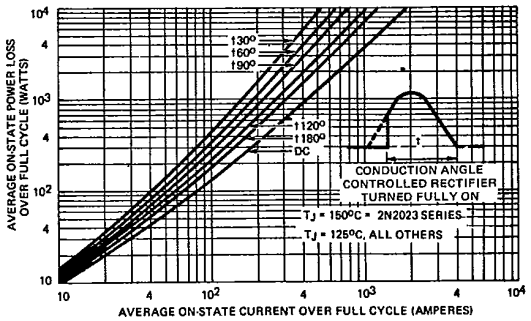


Fig. 4 – Maximum High-Level On-State Power Loss Vs. Current (Sinusoidal Current Waveform)

A

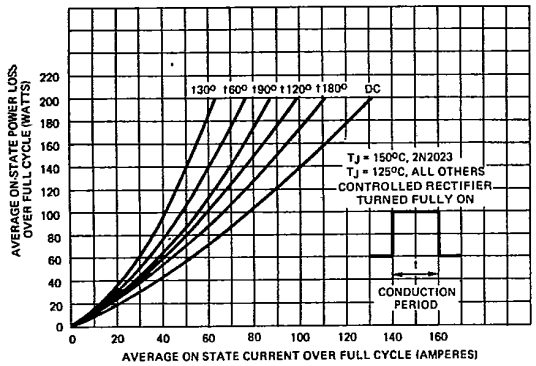


Fig. 5 – Maximum Low-Level On-State Power Loss Vs. Current (Rectangular Current Waveform)

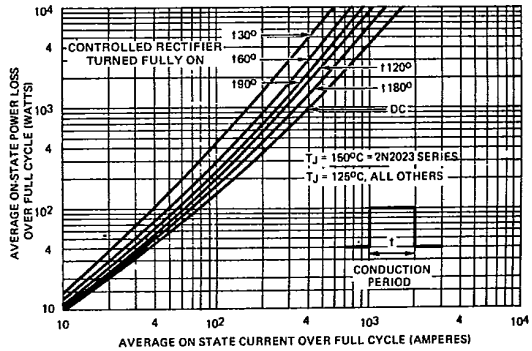


Fig. 6 – Maximum High-Level On-State Power Loss Vs. Current (Rectangular Current Waveform)

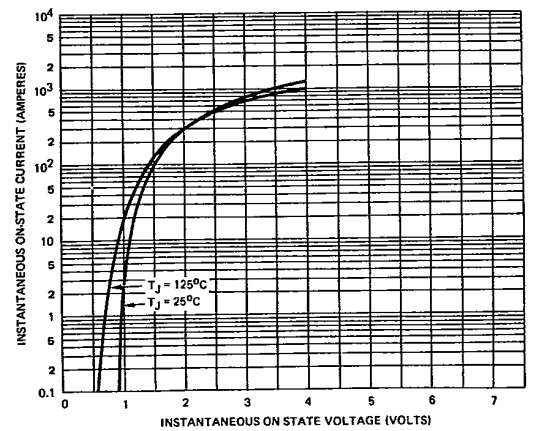


Fig. 7 – Maximum Instantaneous On-State Voltage Vs. Current (2N1792, 2N1805 and 2N1909 Series)

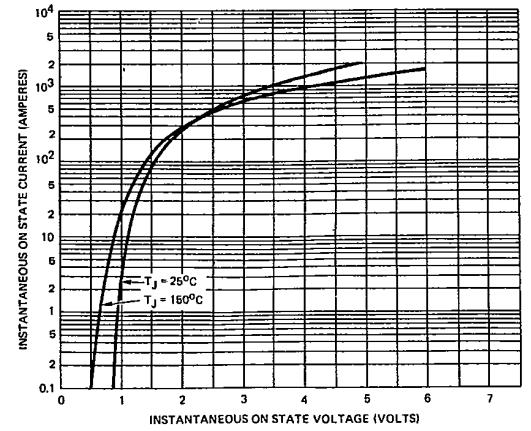


Fig. 8 – Maximum Instantaneous On-State Voltage Vs. Current (2N2023 Series)

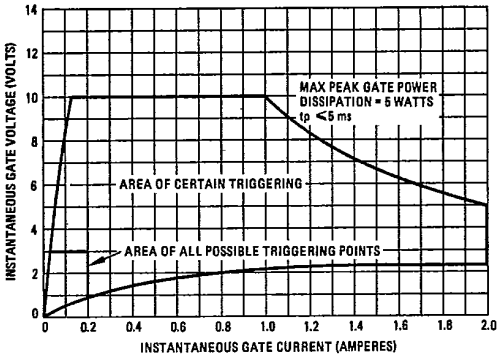


Fig. 9 — Gate Characteristics

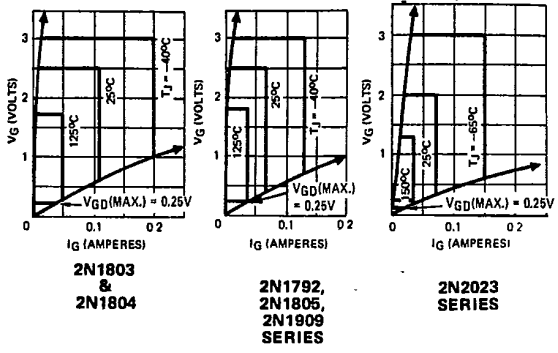


Fig. 9A — Areas of All Possible Triggering Points Vs. Junction Temperature

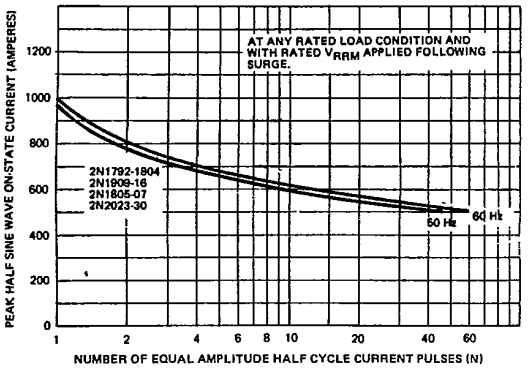


Fig. 10 — Maximum Non-Repetitive Surge Current Vs. Number of Current Pulses

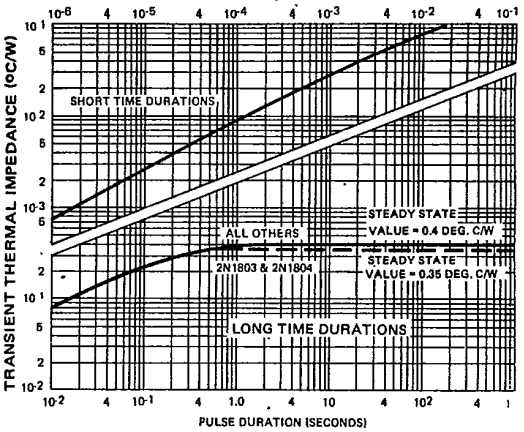
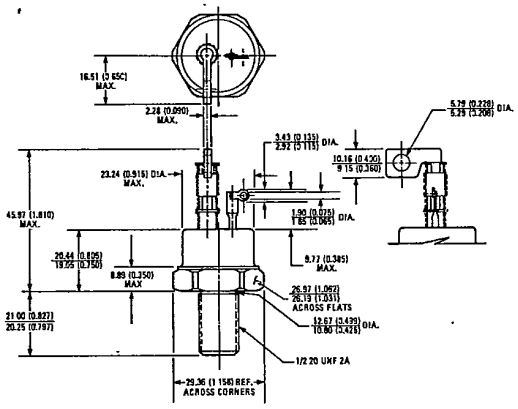


Fig. 11 — Transient Thermal Impedance, Junction to Case, Vs. Pulse Duration



IR Case Style A-14
Conforms to JEDEC Outline TO-208AD (TO-83)
All Dimensions in Millimeters and (Inches)''