## **STRH100N10**



## Rad-Hard 100 V, 48 A N-channel Power MOSFET

**Datasheet - production data** 

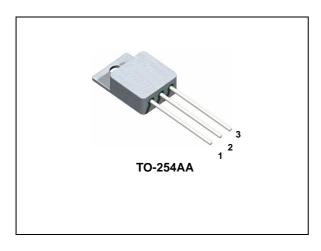
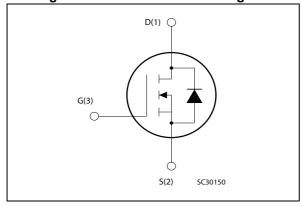


Figure 1. Internal schematic diagram



#### **Features**

V <sub>BDSS</sub>	I <sub>D</sub>	R <sub>DS(on)</sub>	$Q_g$
100 V	48 A	30 mΩ	135 nC

- Fast switching
- 100% avalanche tested
- Hermetic package
- 70 krad TID
- SEE radiation hardened

### **Applications**

- Satellite
- High reliability

### **Description**

This N-channel Power MOSFET is developed with STMicroelectronics unique STripFET™ process. It has specifically been designed to sustain high TID and provide immunity to heavy ion effects. This Power MOSFET is fully ESCC qualified.

**Table 1. Device summary** 

Part number	ESCC part number	Quality level	Package	Lead finish	Mass (g)	Temp. range	EPPL
STRH100N10HY1	-	Engineering model		Gold		_	-
STRH100N10HYG	5205/021/01	ESCC flight	TO-254AA		10	-55 to 150°C	Yes
STRH100N10HYT	5205/021/02	Loco Iligiti		Solder dip			-

Note: Contact ST sales office for information about the specific conditions for product in die form and for other packages.

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STRH100N10 Electrical ratings

# 1 Electrical ratings

(T<sub>C</sub>= 25 °C unless otherwise specified)

Table 2. Absolute maximum ratings (pre-irradiation)

Symbol	Parameter	Value	Unit
V <sub>DS</sub> (1)	Drain-source voltage (V <sub>GS</sub> = 0)	100	V
V <sub>GS</sub> (2)	Gate-source voltage	±20	V
I <sub>D</sub> <sup>(3)</sup>	Drain current (continuous)	48	Α
I <sub>D</sub> <sup>(3)</sup>	Drain current (continuous) at T <sub>C</sub> = 100 °C	30	Α
I <sub>DM</sub> <sup>(4)</sup>	Drain current (pulsed)	192	Α
P <sub>TOT</sub> (3)	Total dissipation	170	W
dv/dt (5)	Peak diode recovery voltage slope	2.6	V/ns
T <sub>stg</sub>	Storage temperature	- 55 to 150	°C
T <sub>J</sub>	Operating junction temperature	- 55 (0 150	°C

- 1. This rating is guaranteed @ T $_{\rm J}~\ge~25~{\rm ^{\circ}C}$  (see Figure 10: Normalized BV $_{\rm DSS}$  vs temperature).
- 2. This value is guaranteed over the full range of temperature.
- 3. Rated according to the Rthj-case + Rthc-s.
- 4. Pulse width limited by safe operating area.
- 5.  $I_{SD} \le 48 \text{ A}$ , di/dt  $\le 100 \text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case	0.52	°C/W
R <sub>thc-s</sub>	Case-to-sink typ	0.21	°C/W

**Table 4. Avalanche characteristics** 

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max)	24	Α
E <sub>AS</sub> <sup>(1)</sup>	Single pulse avalanche energy (starting T <sub>J</sub> =25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> =50 V)	954	mJ
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>J</sub> =110 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> =50 V)	280	mJ
E <sub>AR</sub>	Repetitive avalanche ( $V_{dd}$ = 50 V, $I_{AR}$ = 24 A, f = 10 KHz, $T_{J}$ = 25 °C, duty cycle = 50%)	60	mJ

Electrical ratings STRH100N10

Table 4. Avalanche characteristics (continued)

Symbol	Parameter	Value	Unit
E	Repetitive avalanche ( $V_{dd}$ = 50 V, $I_{AR}$ = 24 A, f = 100 kHz, $T_{J}$ = 25 °C, duty cycle = 10%)	24	ml
E <sub>AR</sub>	Repetitive avalanche ( $V_{dd}$ = 50 V, $I_{AR}$ = 24 A, f = 100 kHz, $T_{J}$ = 110 °C, duty cycle = 10%)	7.7	mJ

<sup>1.</sup> Maximum rating value.

### 2 Electrical characteristics

( $T_C = 25$  °C unless otherwise specified).

Pre-irradiation

Table 5. Pre-irradiation on/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	80% BV <sub>Dss</sub>			10	μΑ
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = 20 V V <sub>GS</sub> = -20 V	-100		100	nA nA
BV <sub>DSS</sub> (1)	Drain-to-source breakdown voltage	V <sub>GS</sub> = 0, I <sub>D</sub> = 1 mA	100			V
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 1 \text{ mA}$	2		4.5	٧
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 12 V; I <sub>D</sub> = 24 A		0.030	0.035	W

<sup>1.</sup> This rating is guaranteed @  $T_J \ge 25$  °C (see Figure 10: Normalized BV<sub>DSS</sub> vs temperature).

Table 6. Pre-irradiation dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C <sub>iss</sub>	Input capacitance		3940	4925	5910	pF
C <sub>oss</sub> (1)	Output capacitance	$V_{GS} = 0, V_{DS} = 25 V,$	543	679	814	pF
C <sub>rss</sub>	Reverse transfer capacitance	f=1 MHz	190	237	284	pF
C <sub>oss eq.</sub> <sup>(1)</sup>	Equivalent output capacitance (2)	V <sub>GS</sub> = 0, V <sub>DD</sub> = 80 V		480		pF
Qg	Total gate charge		108	135	162	nC
Q <sub>gs</sub>	Gate-to-source charge	$V_{DD} = 50 \text{ V}, I_D = 48 \text{ A},$	21	27	33	nC
Q <sub>gd</sub>	Gate-to-drain ("Miller") charge	V <sub>GS</sub> =12 V	36	45	54	nC
R <sub>G</sub> <sup>(3)</sup>	Gate input resistance		1.2	1.7	2	Ω
L <sub>G</sub>	Gate inductance	f=1 MHz gate DC bias=0 test signal level=20mV open drain		4.5		nΗ
L <sub>S</sub>	Source inductance			7.5		nH
L <sub>D</sub>	Drain inductance			7.5		nΗ

 $<sup>{\</sup>bf 1.} \quad {\bf This \ value \ is \ guaranteed \ over \ the \ full \ range \ of \ temperature.}$ 



<sup>2.</sup> This value is defined as the ratio between the  $\mathbf{Q}_{\mathrm{oss}}$  and the voltage value applied.

<sup>3.</sup> Not tested, guaranteed by process.

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Table 7. Switching times (pre-irradiation)

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
t <sub>d(on)</sub>	Turn-on delay time	$V_{DD} = 50 \text{ V}, I_{D} = 24 \text{ A},$ $R_{G} = 4.7 \Omega, V_{GS} = 12 \text{ V}$	23	29.5	36	ns
t <sub>r</sub>	Rise time		29	40	52	ns
t <sub>d(off)</sub>	Turn-off-delay time		79	99	119	ns
t <sub>f</sub>	Fall time		33	64	95	ns

Table 8. Source drain diode (pre-irradiation) (1)

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
I <sub>SD</sub>	Source-drain current				48	Α
I <sub>SDM</sub> <sup>(2)</sup>	Source-drain current (pulsed)				192	Α
V <sub>SD</sub> (3)	Forward on voltage	I <sub>SD</sub> = 48 A, V <sub>GS</sub> = 0			1.5	V
t <sub>rr</sub> <sup>(4)</sup>	Reverse recovery time	I <sub>SD</sub> = 48 A,	328	413	498	ns
Q <sub>rr</sub> <sup>(4)</sup>	Reverse recovery charge	$di/dt = 100 A/\mu s$		5		μC
I <sub>RRM</sub> <sup>(4)</sup>	Reverse recovery current	V <sub>DD</sub> = 50 V, T <sub>J</sub> = 25 °C		24		Α
t <sub>rr(4)</sub>	Reverse recovery time	I <sub>SD</sub> = 48 A,	400	500	600	ns
Q <sub>rr</sub> <sup>(4)</sup>	Reverse recovery charge	di/dt = 100 A/μs		7		μC
I <sub>RRM</sub> <sup>(4</sup>	Reverse recovery current	V <sub>DD</sub> = 50 V, T <sub>J</sub> = 150 °C		28		Α

<sup>1.</sup> Refer to the Figure 16.

<sup>2.</sup> Pulse width limited by safe operating area.

<sup>3.</sup> Pulsed: pulse duration = 300  $\mu$ s, duty cycle 1.5%.

<sup>4.</sup> Not tested in production, guaranteed by process.

### 3 Radiation characteristics

The technology of the STMicroelectronics Rad-Hard Power MOSFETs is extremely resistant to radiative environments. Every manufacturing lot is tested, using the TO-3 package, in total ionizing dose (irradiation done according to the ESCC 22900 specification, window 1) and single event effect according to the MIL-STD-750E TM1080 up to a fluence level of 3e+5 ions/cm². Both pre-irradiation and post-irradiation performances are tested and specified using the same circuitry and test conditions in order to provide a direct comparison.

 $(T_{amb} = 22 \pm 3 \, ^{\circ}C \text{ unless otherwise specified}).$ 

### Total dose radiation (TID) testing

One bias conditions using the TO-3 package:

V<sub>GS</sub> bias: + 15 V applied and V<sub>DS</sub>= 0 V during irradiation

The following parameters are measured (see *Table 9*, *Table 10* and *Table 11*):

- before irradiation
- after irradiation
- after 24 hrs @ room temperature
- after 240 hrs @ 100 °C anneal

Table 9. Post-irradiation on/off states @ T<sub>.J</sub>= 25 °C, (Co60 γ rays 70 K Rad(Si))

Symbol	Parameter	Test conditions	Drift values $\Delta$	Unit
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	80% BV <sub>Dss</sub>	+4	μΑ
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = 20 V V <sub>GS</sub> = -20 V	15 -15	nA
BV <sub>DSS</sub>	Drain-to-source breakdown voltage	V <sub>GS</sub> = 0, I <sub>D</sub> = 1 mA	-25%	V
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 1 \text{ mA}$	-50% / + 5%	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 36 A	±10%	W

Table 10. Dynamic post-irradiation @  $T_J$ = 25 °C, (Co60  $\gamma$  rays 70 K Rad(Si)) (1)

Symbol	Parameter	Test conditions	Drift values $\Delta$	Unit
$Q_g$	Total gate charge		-5% / +50%	
$Q_{gs}$	Gate-source charge	$I_G = 1 \text{ mA}, V_{GS} = 12 \text{ V}, V_{DS} = 50 \text{ V}, I_{DS} = 40 \text{ A}$	±35%	nC
$Q_{gd}$	Gate-drain charge	, , , , , , , , , , , , , , , , , , ,	-5% / +130%	

<sup>1.</sup> Post irradiation data guaranteed at 25°C per ESCC 22900 specification.

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Table 11. Source drain diode post-irradiation @  $T_J$ = 25 °C, (Co60  $\gamma$  rays 70 K Rad(Si))<sup>(1)</sup>

Symbol	Parameter	Test conditions	Drift values $\Delta$ .	Unit
V <sub>SD</sub> (2)	Forward on voltage	$I_{SD} = 50 \text{ A}, V_{GS} = 0$	±10%	V

<sup>1.</sup> Refer to Figure 16.

#### Single event effect, SOA

The technology of the STMicroelectronics rad-hard Power MOSFETs is extremely resistant to heavy ion environment for single event effect according to MIL-STD-750E method 1080 (bias circuit in *Figure 3: Single event effect, bias circuit*) SEB and SEGR tests have been performed with a fluence of 3e+5 ions/cm<sup>2</sup>.

The accept/reject criteria are:

- SEB test: drain voltage checked, trigger level is set to V<sub>ds</sub> = 5 V. Stop condition: as soon as a SEB occurs or if the fluence reaches 3e+5 ions/cm<sup>2</sup>.
- SEGR test: the gate current is monitored every 100 ms. A gate stress is performed before and after irradiation. Stop condition: as soon as the gate current reaches 100 nA (during irradiation or during PIGS test) or if the fluence reaches 3e+5 ions/cm².

#### The results are:

- SEB immune at 60 MeV/mg/cm2
- SEGR immune at 60 MeV/mg/cm2 within the safe operating area (SOA) given in Table 12: Single event effect (SEE), safe operating area (SOA) and Figure 2: Single event effect, SOA)

Table 12. Single event effect (SEE), safe operating area (SOA)

lon	Let (Mev/(mg/cm <sup>2</sup> )	Energy (MeV)	Range (µm)	V <sub>DS</sub> (V)					
				@V <sub>GS</sub> =0	@V <sub>GS</sub> = -2 V	@V <sub>GS</sub> = -5 V	@V <sub>GS</sub> = -10 V	@V <sub>GS</sub> = -20 V	
Kr	32	768	94	100	80	60	30	10	
Xe	60	1217	89	40	30	30	-	0	

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<sup>2.</sup> Pulsed: pulse duration = 300  $\mu$ s, duty cycle 1.5%

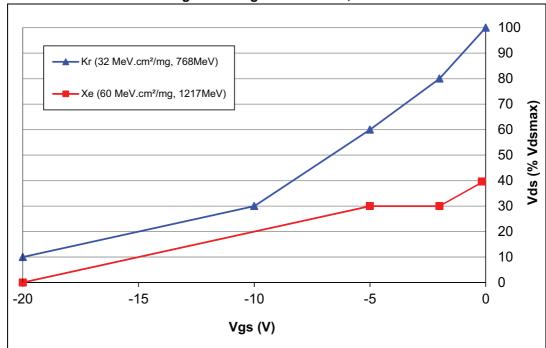
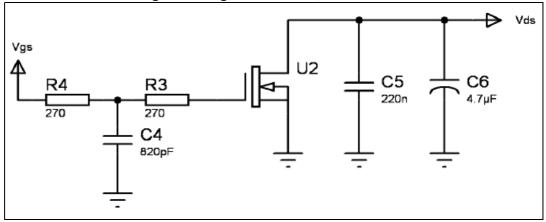


Figure 2. Single event effect, SOA





a. Bias condition during radiation refer to Table 12: Single event effect (SEE), safe operating area (SOA) .



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# 4 Electrical characteristics (curves)

Figure 4. Safe operating area

1000
AM049652/2
100
AM049652/2
100
T=150°C
10ms
1 Tc=25°C
Single pulse
0.1 1 10 100 1000

Figure 5. Thermal impedance

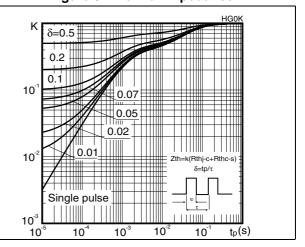


Figure 6. Output characteristics

100 AM01494v1

(A) VGS=12V

7V

150

50

Figure 7. Transfer characteristics

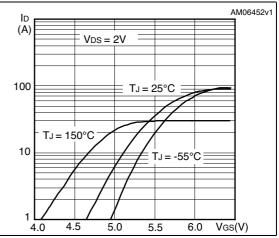


Figure 8. Gate charge vs gate-source voltage

5V

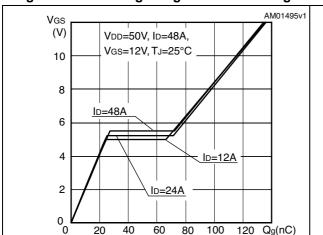
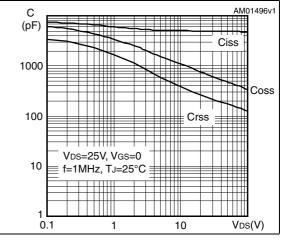


Figure 9. Capacitance variations



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Figure 10. Normalized  $\mathrm{BV}_{\mathrm{DSS}}$  vs temperature

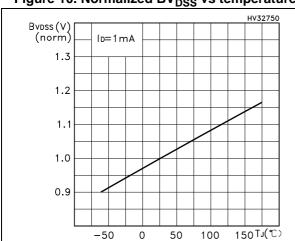


Figure 11. Static drain-source on resistance

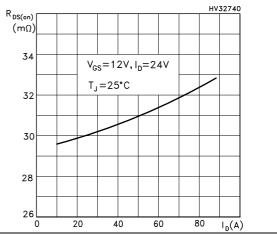


Figure 12. Normalized gate threshold voltage vs temperature

50

100

0

-50

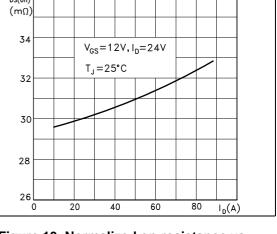
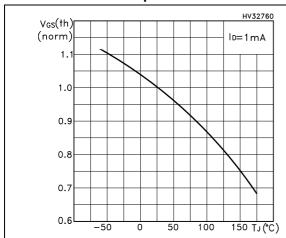


Figure 13. Normalized on-resistance vs temperature



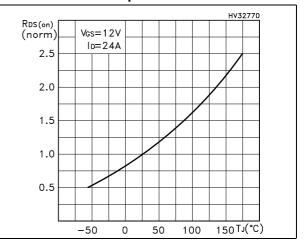
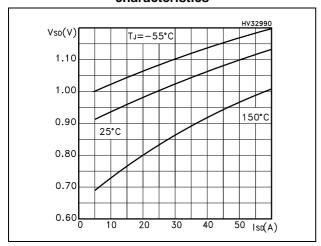


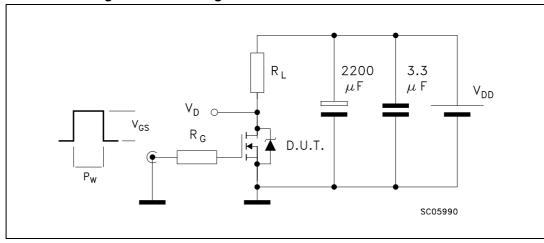
Figure 14. Source drain-diode forward characteristics



Test circuits STRH100N10

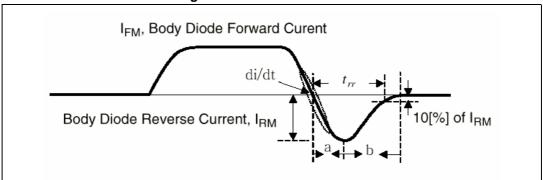
## 5 Test circuits

Figure 15. Switching times test circuit for resistive load <sup>(1)</sup>



1. Max driver V<sub>GS</sub> slope = 1V/ns (no DUT)

Figure 16. Source drain diode



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STRH100N10 Test circuits

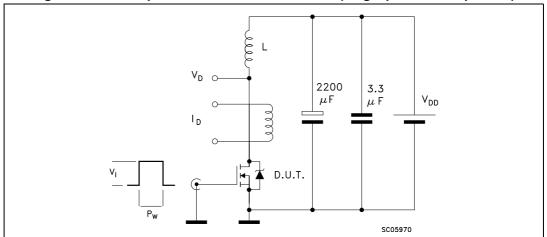


Figure 17. Unclamped inductive load test circuit (single pulse and repetitive)

# 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: <a href="https://www.st.com">www.st.com</a>. ECOPACK<sup>®</sup> is an ST trademark.

Table 13. TO-254AA mechanical data

Dim		mm		Inch			
Dim.	Min.	Тур.	Max.	Min.	Тур.	Max.	
Α	13.59		13.84	0.535		0.545	
В	13.59		13.84	0.535		0.545	
С	20.07		20.32	0.790		0.800	
D	6.32		6.60	0.249		0.260	
E	1.02		1.27	0.040		0.050	
F	3.56		3.81	0.140		0.150	
G	16.89		17.40	0.665		0.685	
Н		6.86			0.270		
I	0.89	1.02	1.14	0.035	0.040	0.045	
J		3.81			0.150		
K		3.81			0.150		
L	12.95		14.50	0.510		0.571	
М	2.92		3.18				
N			0.71				
R1			1.00			0.039	
R2	1.52	1.65	1.78	0.060	0.065	0.070	

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Figure 18. TO-254AA mechanical drawing

Order codes STRH100N10

### 7 Order codes

**Table 14. Ordering information** 

Order code	ESCC part number	Quality level	EPPL	Package	Lead finish	Marking	Packing
STRH100N10HY1	-	Engineering model	-		Gold	STRH100N10HY1+ BeO	
STRH100N10HYG	5205/021/01		Yes	TO-254AA		520502101F + BeO	Strip pack
STRH100N10HYT	5205/021/02	ESCC flight	-		Solder dip	520502102F + BeO	, , ,

For specific marking only the complete structure is:

- ST Logo
- ESA Logo
- Date code (date of sealing of the package): YYWWA
  - YY: year
  - WW: week number
  - A: week index
- ESCC part number (as mentioned in the table)
- Warning signs (e.g. BeO)
- Country of origin: FR (France)
- · Part serial number within in the assembly lot

Contact ST sales office for information about the specific conditions for products in die form and for other packages.

### 7.1 Other information

#### Date code

The date code for "ESCC flight" is structured as follows: yywwz

#### where:

- yy: last two digits of year
- ww: week digits
- z: lot index in the week

#### **Documentation**

The table below provide a summary of the documentation provided with each type of products.

STRH100N10 Order codes

Table 15. Summary of the documentation provided

Quality level	Radiation level	Documentation
Engineering model	-	-
ESCC flight	70Krad	Certificate of conformance radiation verification test report

Revision history STRH100N10

# 8 Revision history

**Table 16. Document revision history** 

Date	Revision	Changes
13-May-2010	1	First release.
14-Jun-2010	2	Updated Table 1: Device summary.
18-Oct-2010	3	Updated Table 1, 5, 9 and 14.
23-Dec-2010	4	Updated Figure 2: Single event effect, SOA. and TO-254AA mechanical data.
25-Jul-2011	5	Updated part numbers in <i>Table 1: Device summary</i> and <i>Table 14: Ordering information</i> .  Minor text changes to improve readability.
09-Nov-2011	6	Updated dynamic values on <i>Table 6: Pre-irradiation dynamic</i> , <i>Table 7: Switching times (pre-irradiation)</i> and <i>Table 8: Source drain diode (pre-irradiation)</i> .
31-May-2013	7	Updated <i>Table 1</i> , <i>Table 12</i> , <i>Table 14</i> , <i>Figure 2</i> and <i>Section 7: Order codes</i> .  Minor text changes in <i>Section 3: Radiation characteristics</i>
09-Apr-2014	8	Modified: Figure 2 Minor text changes

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