PRELIMINARY

NEC NEC LCD Technologies, Ltd.

TFT COLOR LCD MODULE

NL10276BC30-24D

38.0cm (15.0 Type)
XGA
LVDS Interface (1 port)

PRELIMINARY DATA SHEET

DOD-PD-0306 (2nd edition)

This PRELIMINARY DATA SHEET is updated document from DOD-PD-0258(1).

All information is subject to change without notice. Please confirm the sales representative before starting to design your system.

INTRODUCTION

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NL10276BC30-24D

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1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Color LCD module NL10276BC30-24D is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color (Red, Green, Blue) data signals from a host system (e.g. PC, signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATION

- Notebook PC

1.3 FEATURES

- LVDS interface
- High luminance
- Wide viewing angle
- High contrast
- Wide color gamut
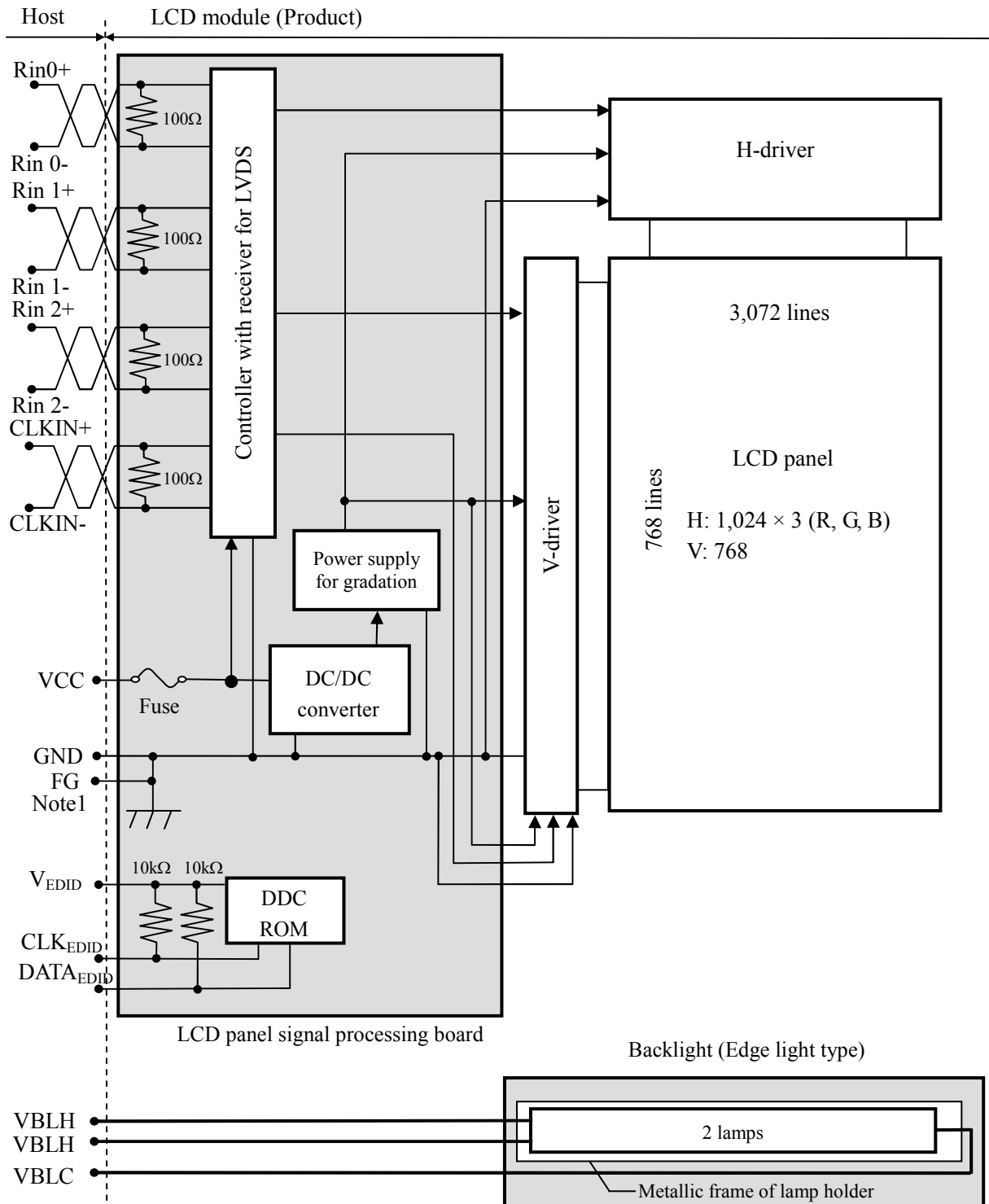- Edge light type backlight   **Note1**

Note1: Backlight is not replaceable by customers.

2. GENERAL SPECIFICATIONS

Display area	304.128 (H) × 228.096 (V) mm (typ.)
Diagonal size of display	38.0 cm (15.0 inches)
Drive system	a-Si TFT active matrix
Display color	262,144 colors
Pixel	1,024 (H) × 768 (V) pixels
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe
Dot pitch	0.099 (H) × 0.297 (V) mm
Pixel pitch	0.297 (H) × 0.297 (V) mm
Module size	317.3 (W) × 242.2 (H) × 9.8 (D) mm (typ.)
Weight	TBD g (typ.)
Contrast ratio	400:1 (typ.)
Viewing angle	*At the contrast ratio* $\geq 10:1$ • Horizontal: Right side 60° (typ.), Left side 60° (typ.) • Vertical: Up side 40° (typ.), Down side 60° (typ.)
Designed viewing direction	Viewing angle with optimum grayscale (γ=2.2): normal axis
Polarizer surface	Clear hard coat + Low reflection
Polarizer pencil-hardness	2H (min.) [by JIS K5400]
Color gamut	*At LCD panel center* 72% (typ.) [against NTSC color space]
Response time	*Ton+Toff (White90%←→Black10%)* TBD ms (typ.)
Luminance	*At lamp current IBL= 6.0mArms / lamp* 320 cd/m^2 (typ.)
Signal system	1port LVDS (Receiver: THC63LVDF84A, THine Electronics Inc. or equivalent) [6bit digital signals for data of RGB colors, Dot clock (CLK), Data enable (DE)]
Power supply voltage	LCD panel signal processing board: 3.3V
Backlight	Edge light type: 2 cold cathode fluorescent lamps (without inverter)
Power consumption	*At lamp current IBL=6.0mArms / lamp and checkered flag pattern* TBD W (typ., Power dissipation of the inverter does not include.)

3. BLOCK DIAGRAM

Host   LCD module (Product)

Rin0+
Rin 0-
Rin 1+
Rin 1-
Rin 2+
Rin 2-
CLKIN+
CLKIN-

100Ω
100Ω
100Ω
100Ω

Controller with receiver for LVDS

H-driver

3,072 lines

LCD panel

H: 1,024 × 3 (R, G, B)
V: 768

768 lines

V-driver

Power supply for gradation

VCC
Fuse

DC/DC converter

GND
FG
Note1

V_{EDID} 10kΩ 10kΩ
CLK$_{EDID}$
DATA$_{EDID}$

DDC ROM

LCD panel signal processing board

Backlight (Edge light type)

VBLH
VBLH
VBLC

2 lamps

Metallic frame of lamp holder

Note1: GND (Signal ground) and FG (Frame ground) are connected in the product.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS 4.1

Parameter	Specification		Unit
Module size	317.3 ± 0.5 (W) $\times$ $242.2 \pm$ TBD (H) $\times$ $9.8 \pm$ TBD (D)	Note1	mm
Display area	304.128 (H) $\times$ 228.096 (V)	Note1	mm
Weight	TBD (typ.), TBD (max.)		g

Note1: See **"7. OUTLINE DRAWINGS"**.

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board	VCC	-0.3 to +4.0	V	Ta = 25°C
	DDC (EDID) ROM	V_{EDID}	-0.3 to +6.5	V	
	Lamp voltage	VBLH	TBD	Vrms	
Input voltage for signals	Display signals Note1	VD	-0.3 to VCC+0.3	V	
	Function signal Note2	VF	-0.3 to V_{EDID} +0.3	V	
Storage temperature		Tst	-20 to +60	°C	-
Operating temperature		TopF	0 to +50	°C	Note3
		TopR	0 to +50	°C	Note4
Relative humidity Note5		RH	≤ 95	%	Ta $\leq$ 40°C
			≤ 85	%	40 < Ta $\leq$ 50°C
Absolute humidity Note5		AH	≤ 73 Note6	g/m^3	Ta > 50°C

Note1: Display signals are Rin0+/-, Rin1+/-, Rin2+/- and CLKIN+/-.
Note2: Function signal is $DATA_{EDID}$, CLK_{EDID}
Note3: Measured at center of LCD panel surface (including self-heat)
Note4: Measured at center of LCD module's rear shield surface (including self-heat)
Note5: No condensation
Note6: Ta = 55°C, RH = 85%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 Signal processing board for driving LCD panel

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VCC	3.0	3.3	3.6	V	-
Power supply current		ICC	-	TBD Note1	TBD Note2	mA	at VCC=3.3V
Permissible ripple voltage		VRP	-	-	100	mVp-p	for VCC
Differential input threshold voltage for LVDS receiver	High	VTH	-	-	+100	mV	at VCM=1.2V Note3
	Low	VTL	-100	-	-	mV	
Termination resistor		RT	-	100	-	Ω	-
Power supply voltage for DDC		V_{EDID}	1.8	-	5.5	V	-
Input voltage for DDC signal	High	VFIH	0.7VCC	-	-	V	1.8V≤V_{EDID}<5.5V
	Low	VFIL	-	-	0.3VCC	V	
Output voltage for DDC signal	Low	VFOL	-	-	0.4	V	at IFOL= 3.0mA and V_{EDID}=2.5V

Note1: Checkered flag pattern [by EIAJ ED-2522]
Note2: Pattern for maximum current
Note3: Common mode voltage for LVDS receiver

4.3.2 Backlight lamp

(Ta=25°C, Note1)

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Lamp current	IBL	3.5	6.0	6.5	mArms	at IBL=6.0mArms: 320cd/m^2 Note3, Note4
Lamp voltage	VBLH	-	TBD	-	Vrms	Note2,Note3
Lamp starting voltage	VS	TBD	-	-	Vrms	Ta = 25°C Note2, Note3
		1,500	-	-	Vrms	Ta = 0°C Note2, Note3
Lamp oscillation frequency	FO	40	-	60	kHz	Note5

Note1: This product consists of 2 backlight lamps, and these specifications are for each lamp.

Note2: The lamp voltage cycle between lamps should be kept on a same phase. "VS" and "VBLH" are the voltage value between low voltage side (Cold) and high voltage side (Hot).

Note3: The asymmetric ratio of working waveform for lamps (Lamp voltage peak ratio, Lamp current peak ratio and waveform space ratio) should be less than 5 % (See the following figure.). If the waveform is asymmetric, DC (Direct current) element apply into the lamp. In this case, a lamp lifetime may be shortened, because a distribution of a lamp enclosure substance inclines toward one side between low voltage terminal (Cold terminal) and high voltage terminal (Hot terminal).

$$\frac{|Pa - Pb|}{Pb} \times 100 \leq 5\%$$

$$\frac{|Sa - Sb|}{Sb} \times 100 \leq 5\%$$
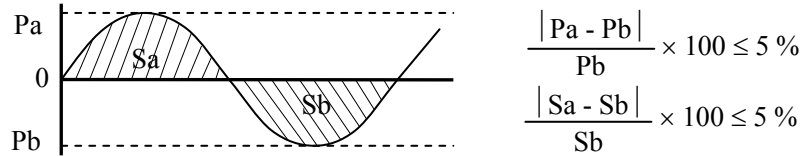
Pa: Supply voltage/current peak for positive, Pb: Supply voltage/current peak for negative
Sa: Waveform space for positive part, Sb: Waveform space for negative part

Note4: This product consists of 2 lamps. 2 lamps contain in the 1 lamp holder, and both lamps are connected to 1 low voltage cable. Lamp current must be 6.0mArms typical for each lamp, and sum of 2 lamps must be 12mArms typical. The lamp current should be measured by high-frequency current meter at the low voltage terminal.

Note5: In case "FO" is not the recommended value, beat noise may display on the screen, because of interference between "FO" and "1/th". Recommended value of "FO" is as following.

$$FO = \frac{1}{4} \times \frac{1}{th} \times (2n-1)$$

th: Horizontal cycle period (See "**4.7.2 Timing characteristics**".)
n: Natural number (1, 2, 3 ········)

Note6: Method of lamp cable installation may invite fluctuation of lamp current and voltage or asymmetric of lamp working waveform. When design the backlight inverter, evaluate the fluctuation of lamp current and voltage or asymmetric of lamp working waveform sufficiently.

4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Parameter	Power supply voltage	Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VCC	3.3 V	≤ 100	mVp-p

Note1: The permissible ripple voltage includes spike noise.

4.3.4 Fuses

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VCC	TBD	TBD	TBD	TBD	Note1
			TBD		

Note1: The power supply capacity should be more than the fusing current. If the power supply capacity is less than the fusing current, the fuse may not blow for a short time, and then nasty smell, smoking and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

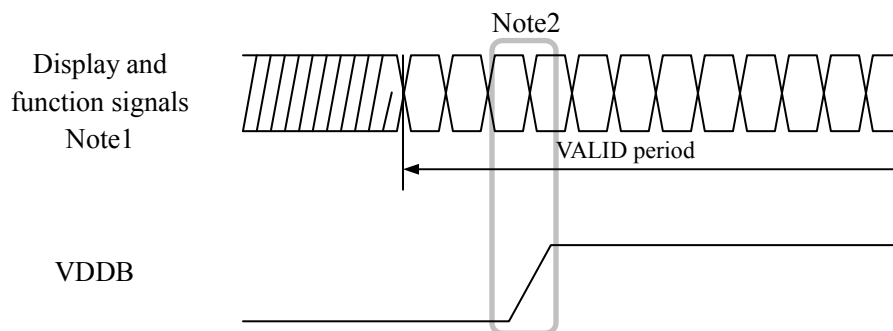### 4.4.1 Sequence for LCD panel signal processing board
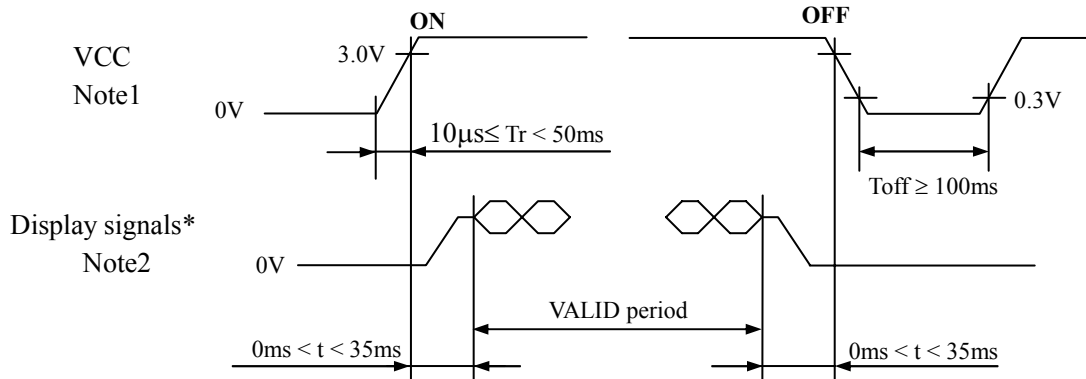
* These signals should be measured at the terminal of 100Ω resistance.

Note1: In terms of voltage variation (voltage drop) while VCC rising edge is below 3.0V, a protection circuit may work, and then this product may not work.

Note2: Display signals (Rin0+/-, Rin1+/-, Rin2+/- and CLKIN+/-) must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.

If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. If customer stops the display and function signals, they should be cut VCC.

4.4.2 Sequence for backlight inverter

Note1: These are the display and function signals for LCD panel signal processing board.

Note2: The backlight inverter voltage (VDDB) should be inputted within the valid period of display and function signals, in order to avoid unstable data display.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): FI-XB30SL-HF10 (Japan Aviation Electronics Industry Limited (JAE))

Adaptable plug: FI-X30∗ (Japan Aviation Electronics Industry Limited (JAE))

No.	Signal	Function	Remarks
1	GND	Ground	Connect to system ground.
2	VCC	Power supply 3.3V±0.3V	Supply +3.3V.
3	VCC	Power supply 3.3V±0.3V	
4	V EDID	DDC 3.3V	-
5	N.C.	No Connection (Reserved)	Keep this pin Open.
6	CLK EDID	DDC Clock	-
7	DATA EDID	DDC Data	-
8	Rin0-	LVDS Differential Data Input	Note1
9	Rin0+	LVDS Differential Data Input	
10	GND	Ground	Connect to system ground.
11	Rin1-	LVDS Differential Data Input	Note1
12	Rin1+	LVDS Differential Data Input	
13	GND	Ground	Connect to system ground.
14	Rin2-	LVDS Differential Data Input	Note1
15	Rin2+	LVDS Differential Data Input	
16	GND	Ground	Connect to system ground.
17	CLKIN-	LVDS Differential Clock Input	Note1
18	CLKIN+	LVDS Differential Clock Input	
19	GND	Ground	Connect to system ground.
20	N.C.	No Connection	Keep this pin Open.
21	N.C.	No Connection	
22	GND	Ground	Connect to system ground.
23	N.C.	No Connection	Keep this pin Open.
24	N.C.	No Connection	
25	GND	Ground	Connect to system ground.
26	N.C.	No Connection	Keep this pin Open.
27	N.C.	No Connection	
28	GND	Ground	Connect to system ground.
29	N.C.	No Connection	Keep this pin Open.
30	N.C.	No Connection	

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be connected between LCD panel signal processing board and LVDS transmitter.
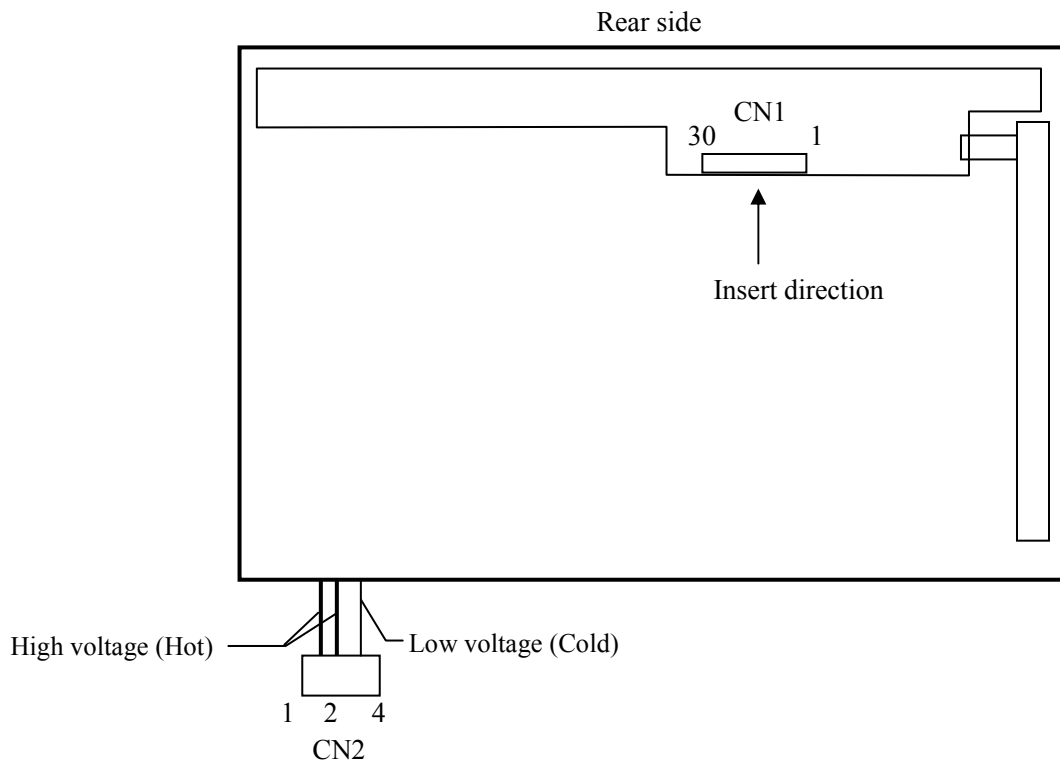
4.5.2 Backlight lamp

Attention: VBLH and VBLC must be connected correctly. If customer connects wrongly, customer will be hurt and the module will be broken.

CN2 plug (LCD module side): BHR-04VS-1 (J.S.T Mfg. Co., Ltd.)
Adaptable socket: SM04 (4.0) B-BHS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH	High voltage (Hot)	Cable color: White
2	VBLH	High voltage (Hot)	Cable color: White
3	N.C.	No Connection	Keep this pin Open
4	VBLC	Low voltage (Cold)	Cable color: Gray

4.5.3 Positions of plug and socket

Rear side

CN1

30   1

Insert direction

High voltage (Hot)   Low voltage (Cold)

1 2 4
CN2

4.5.4 Connection between receiver and transmitter for LVDS

Note1: Recommended transmitter THC63LVDM83R (THine Electronics Inc.) or equivalent
Note2: R0, G0, B0–LSB (Least Significant Bit), R5, G5, B5– MSB (Most Significant Bit)
Note3: Twist pair wires with 100Ω (Characteristic impedance) should be connected between LCD panel signal processing board and LVDS transmitter.

4.6 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 262,144 colors in 64 scale. Also the relation between display colors and input data signals is as the following table.

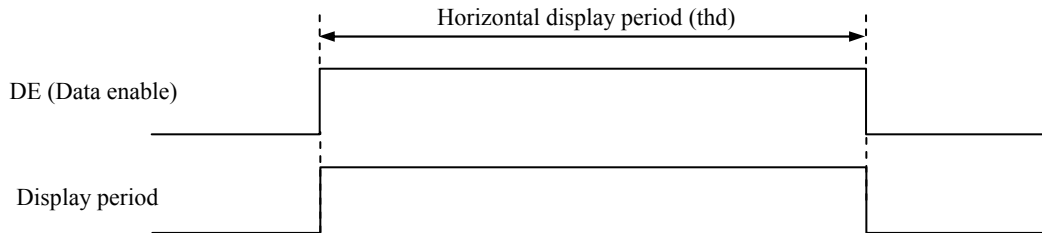| Display colors		Data signal (0: Low level, 1: High level)																	
		R 5	R 4	R 3	R 2	R 1	R 0	G 5	G 4	G 3	G 2	G 1	G 0	B 5	B 4	B 3	B 2	B 1	B 0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑			:						:						:			
	↓			:						:						:			
	bright	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	↑			:						:						:			
	↓			:						:						:			
	bright	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
		0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑			:						:						:			
	↓			:						:						:			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

4.7 INPUT SIGNAL TIMINGS FOR LCD PANEL SIGNAL PROCESSING BOARD
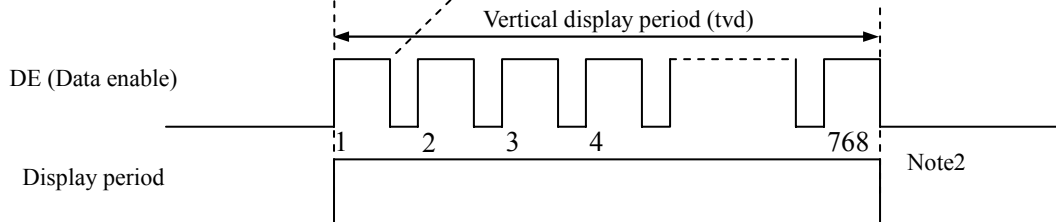
4.7.1 Outline of input signal timings

- Horizontal signal

  Note1

Horizontal display period (thd)

DE (Data enable)

Display period

- Vertical signal

  Note1

Vertical display period (tvd)

DE (Data enable)

1   2   3   4   768   Note2

Display period

Note1: This diagram indicates virtual signal for set up to timing.
Note2: See "**4.7.3 Input signal timing chart**" for numeration of pulse.

4.7.2 Timing characteristics

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/ tc	60.0	65.0	68.0	MHz	15.385 ns (typ.)
	Duty		-		-		-	Note2
	Rise time, Fall time		-				ns	
DATA	CLK-DATA	Setup time	-				ns	Note2
		Hold time	-		-		ns	
	Rise time, Fall time		-				ns	
DE	Horizontal	Cycle	th	19.67	20.676	22.4	μs	48.363 kHz (typ.) Note1, Note2, Note3
				-	1,344	-	CLK	
		Display period	thd		1,024		CLK	
	Vertical (One frame)	Cycle	tv	13.3	16.666	18.5	ms	60.0 Hz (typ.) Note1
				780	806	-	H	
		Display period	tvd		768		H	
	CLK-DE	Setup time	-				ns	Note2
		Hold time	-		-		ns	
	Rise time, Fall time		-				ns	

Note1: Definition of parameters is as follows.

tc = 1CLK, th = 1H

Note2: See the data sheet of LVDS transmitter.

Note3: "th" must keep the fluctuation within ±1 CLK, because of avoidance of image sticking.

4.7.3 Input signal timing chart

Horizontal timing

CLK

DATA
(R0-R5)
(G0-G5)
(B0-B5)

INVALID   1   2   1023 1024   INVALID

DE

thd

th

Vertical timing

DATA
(R0-R5)
(G0-G5)
(B0-B5)

INVALID   1   2   767 768   INVALID

DE

tvd

tv
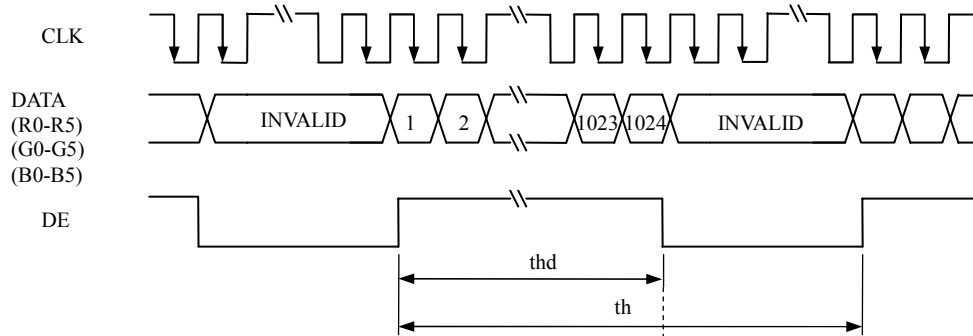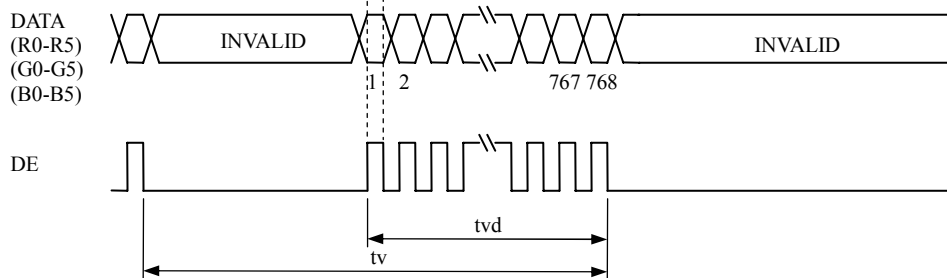
4.7.4 DISPLAY POSITIONS

The following table is the coordinates per pixel (See "**4.7.5 SCANNING DIRECTIONS**".).

C(0, 0)	C(1, 0)	• • •	C(X, 0)	• • •	C(1022, 0)	C(1023, 0)
C(0, 1)	C(1, 1)	• • •	C(X, 1)	• • •	C(1022, 1)	C(1023, 1)
• • •	• • •	• • •	• • •	• • •	• • •	• • •
C(0, Y)	C(1, Y)	• • •	C(X, Y)	• • •	C(1022, Y)	C(1023, Y)
• • •	• • •	• • •	• • •	• • •	• • •	• • •
C(0,766)	C(1,766)	• • •	C(X, 766)	• • •	C(1022,766)	C(1023,766)
C(0,767)	C(1,767)	• • •	C(X, 767)	• • •	C(1022,767)	C(1023,767)

4.7.5 SCANNING DIRECTIONS

The following figure is seen from a front view. Also the arrow shows the direction of scan.
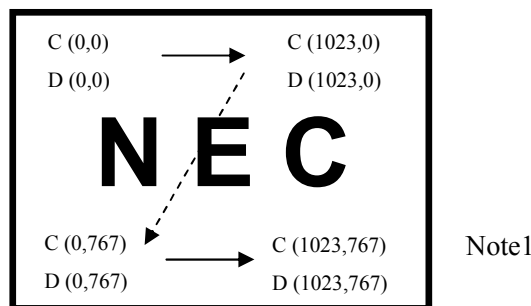
Figure 1. Scanning direction

Note1: Meaning of C (X, Y) and D (X, Y)
 C (X, Y): The coordinates of the display position (See "**4.7.4 DISPLAY POSITIONS**".)
 D (X, Y): The data number of input signal for LCD panel signal processing board

4.7.6 DDC function

This product has a memory (24LC21A, Microchip Technology Inc. or equivalent) to write the EDID for the DDC.
The internal equivalent circuit is following figure.
Control method and usage are according to SPWG (corresponding to Version 2) and IC specifications.

DDC: Display Data Channel
EDID: Extended Display Identification Data
SPWG: STANDARD PANELS WORKING GROUP

CN1

24LC21A,
Microchip Technology Inc. or equivalent
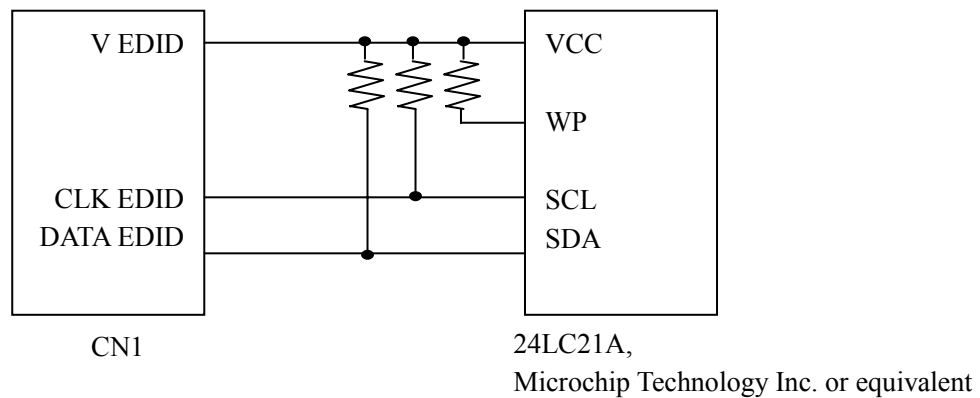
4.8 OPTICS

4.8.1 Optical characteristics

(Note1,Note2)

Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks
Luminance		White at center $\theta R = 0°, \theta L = 0°, \theta U = 0°, \theta D = 0°$	L	TBD	320	-	cd/m^2	BM-5A	-
Contrast ratio		White/Black at center $\theta R = 0°, \theta L = 0°, \theta U = 0°, \theta D = 0°$	CR	TBD	400	-	-	BM-5A	Note3
Luminance uniformity		-	LU	-	1.25	1.40	-	BM-5A	Note4
Chromaticity	White	x coordinate	Wx	0.283	0.313	0.343	-	SR-3	Note5
		y coordinate	Wy	0.299	0.329	0.359	-		
	Red	x coordinate	Rx	-	TBD	-	-		
		y coordinate	Ry	-	TBD	-	-		
	Green	x coordinate	Gx	-	TBD	-	-		
		y coordinate	Gy	-	TBD	-	-		
	Blue	x coordinate	Bx	-	TBD	-	-		
		y coordinate	By	-	TBD	-	-		
Color gamut		$\theta R = 0°, \theta L = 0°, \theta U = 0°, \theta D = 0°$ at center, against NTSC color space	C	TBD	72	-	%		
Response time		Black to White	Ton	-	TBD	TBD	ms	BM-5A	Note6 Note7
		White to Black	Toff	-	TBD	TBD	ms		
Viewing angle	Right	$\theta U = 0°, \theta D = 0°, CR \geq 10$	θR	TBD	60	-	°	BM-5A	Note8
	Left	$\theta U = 0°, \theta D = 0°, CR \geq 10$	θL	TBD	60	-	°		
	Up	$\theta U = 0°, \theta D = 0°, CR \geq 10$	θU	TBD	40	-	°		
	Down	$\theta U = 0°, \theta D = 0°, CR \geq 10$	θD	TBD	60	-	°		

Note1: These are initial characteristics.
Note2: Measurement conditions are as follows.
   Ta = 25°C, VCC = 3.3V, IBL = 6.0mArms/lamp, Display mode: XGA,
   Horizontal cycle = 48.363kHz, Vertical cycle = 60.0Hz

   Optical characteristics are measured at luminance saturation after 20minutes from working the product, in the dark room. Also measurement method for luminance is as follows.
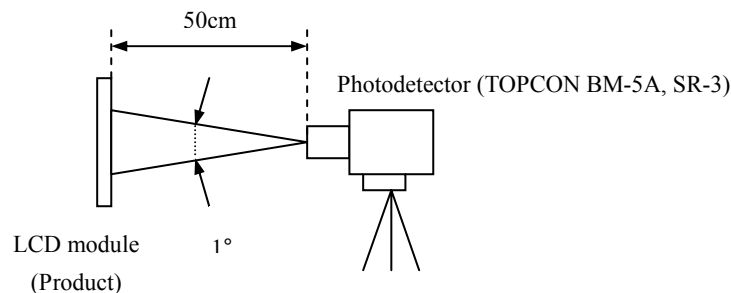
Note3: See "**4.8.2 Definition of contrast ratio**".
Note4: See "**4.8.3 Definition of luminance uniformity**".
Note5: These coordinates are found on CIE 1931 chromaticity diagram.
Note6: Product surface temperature: TopF = TBD°C
Note7: See "**4.8.4 Definition of response times**".
Note8: See "**4.8.5 Definition of viewing angles**".

4.8.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.8.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.
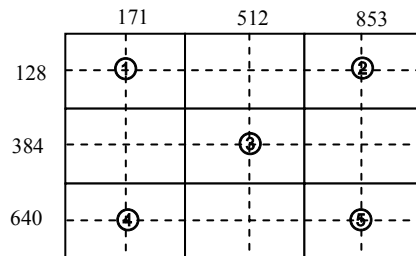
4.8.4 Definition of response times

Response time is measured, the luminance changes from "white" to "black", or "black" to "white" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 90% down to 10%. Also Toff is the time it takes the luminance change from 10% up to 90% (See the following diagram.).
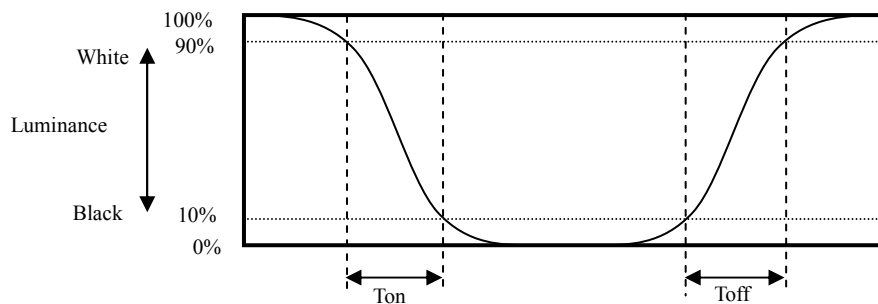
4.8.5 Definition of viewing angles
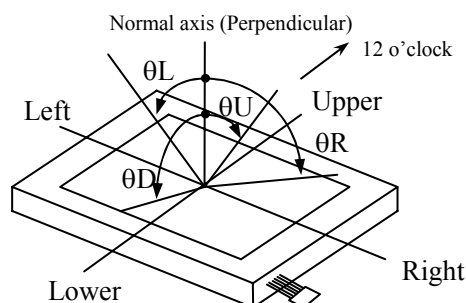
5. RELIABILITY TESTS

Test item	Condition	Judgment
High temperature and humidity (Operation)	① 50 ± 2°C, RH = 85%, 240hours ② Display data is white.	No display malfunctions Note1
Heat cycle (Operation)	① 0 ± 3°C…1hour 55 ± 3°C…1hour ② 50cycles, 4hours/cycle ③ Display data is white.	
Thermal shock (Non operation)	① -20 ± 3°C…30minutes 60 ± 3°C…30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
ESD (Operation)	① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	
Dust (Operation)	① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	
Vibration (Non operation)	① 5 to 100Hz, 19.6m/s^2 ② 1 minute/cycle ③ X, Y, Z direction ④ 120 times each directions	No display malfunctions No physical damages Note1
Mechanical shock (Non operation)	① 539m/ s^2, 11ms ② X, Y, Z direction ③ 5 times each directions	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: See the following figure for discharge points.
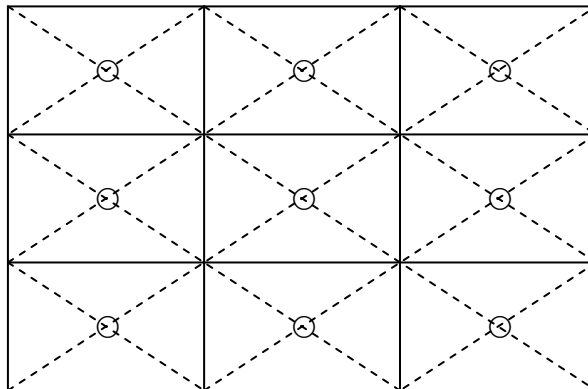
6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding these contents!**

⚠	This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.
⚡	This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.
✍	This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS

⚡

* **Do not touch the working backlight. Customer will be in danger of an electric shock.**

✍

* **Do not touch the working backlight. Customer will be in danger of burn injury.**
* **Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater $539m/s^2$ and to be not greater 11ms, Pressure: To be not greater 19.6 N)**

6.3 ATTENTIONS ⚠

6.3.1 Handling of the product

① Take hold of both ends without touch the circuit board cover when customer pulls out products (LCD modules) from inner packing box. If customer touches it, products may be broken down or out of adjustment, because of stress to mounting parts.

② Do not hook cables nor pull connection cables such as lamp cable and so on, for fear of damage.

③ If customer puts down the product temporarily, the product puts on flat subsoil as a display side turns down.

④ Take the measures of electrostatic discharge such as earth band, ionic shower and so on, when customer deals with the product, because products may be damaged by electrostatic.

⑤ The torque for mounting screws must never exceed TBD N·m. Higher torque values might result in distortion of the bezel.

⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area) except mounting hole portion.
Bends or twist described above and undue stress to any portion except mounting hole portion may cause display un-uniformity.

⑦ Do not press or rub on the sensitive display surface. If customer clean on the panel surface, NEC recommends using the cloth with ethanolic liquid such as screen cleaner for LCD.

⑧ Do not push-pull the interface connectors while the product is working, because wrong power sequence may break down the product.

⑨ Do not bend or unbend the lamp cable at the near part of the lamp holding rubber, to avoid the damage for high voltage side of the lamp. This damage may cause a lamp breaking and abnormal operation of high voltage circuit.

6.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in antistatic pouch in room temperature, because of avoidance for dusts and sunlight, if customer stores the product.
② In order to prevent dew condensation occurring by temperature difference, the product packing box must be opened after leave under the environment of an unpacking room temperature enough. Because a situation of dew condensation occurring is changed by the environmental temperature and humidity, evaluate the leaving time sufficiently. (Recommendation leaving time: 6 hour or more with packing state)
③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
④ This product is not designed as radiation hardened.
⑤ Use an original protection sheet on the product surface (polarizer). Adhesive type protection sheet should be avoided, because it may change color or properties of the polarizer.

6.3.3 Characteristics

The following items are neither defects nor failures.

① Response time, luminance and color may be changed by ambient temperature.
② The LCD may be seemed luminance non-uniformity, flicker, vertical seam or small spot by display patterns.
③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
⑤ The display color may be changed by viewing angle because of the use of condenser sheet in the backlight.
⑥ Optical characteristics may be changed by input signal timings.
⑦ The interference noise of input signal frequency for this product's signal processing board and luminance control frequency of customer's backlight inverter may appear on a display. Set up luminance control frequency of backlight inverter so that the interference noise does not appear.

6.3.4 Other

① All GND, backlight inverter ground (GNDB), VCC and backlight inverter power supply voltage (VDDB) terminals should be used without a non-connected line.
② Do not disassemble a product or adjust variable resistors without permission of NEC.
③ Pay attention not to insert waste materials inside of products, if customer uses screwnails.
④ Pack the product with original shipping package, because of avoidance of some damages during transportation, when customer returns it to NEC for repair and so on.
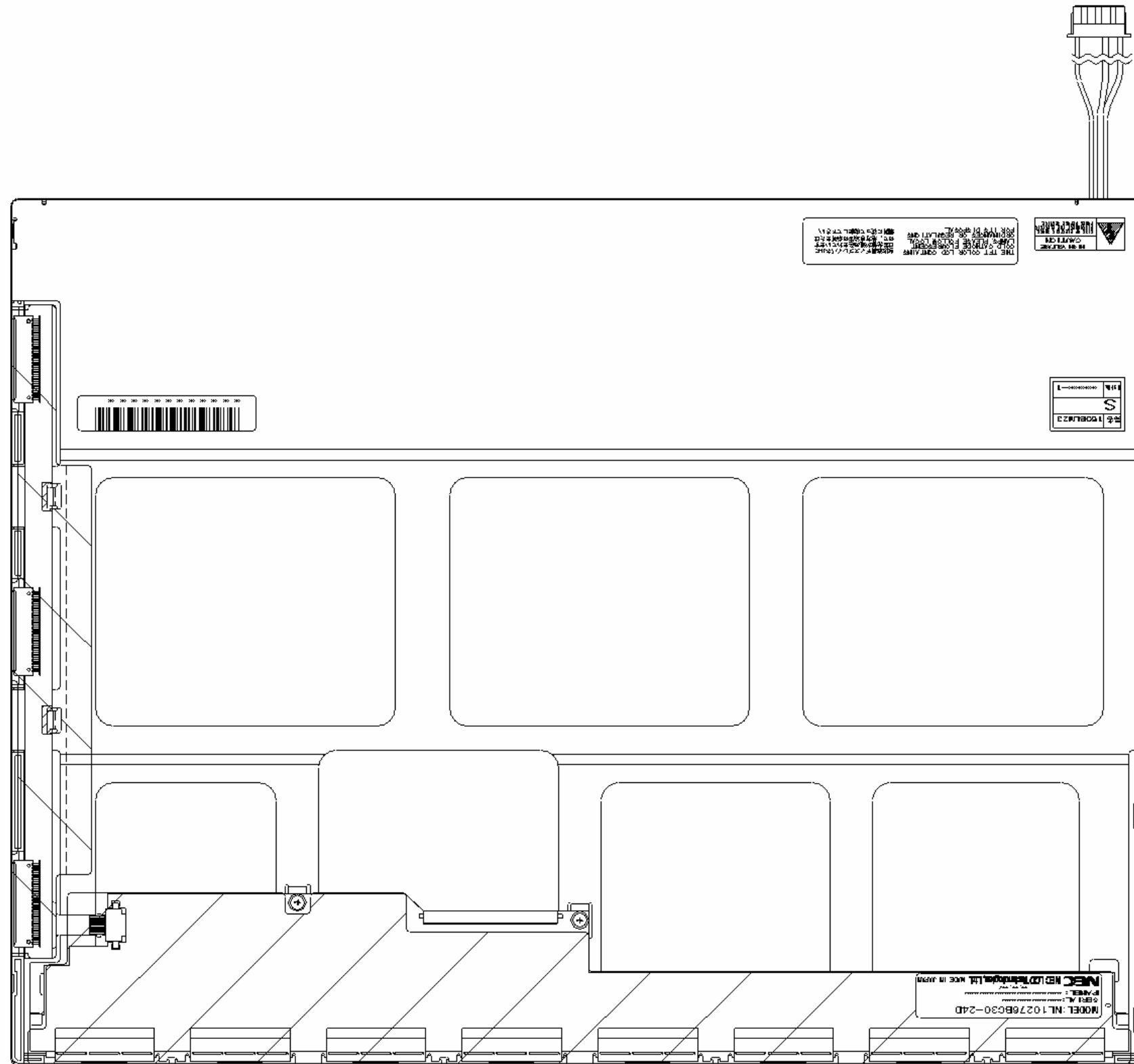
7. OUTLINE DRAWINGS
7.1 FRONT VIEW
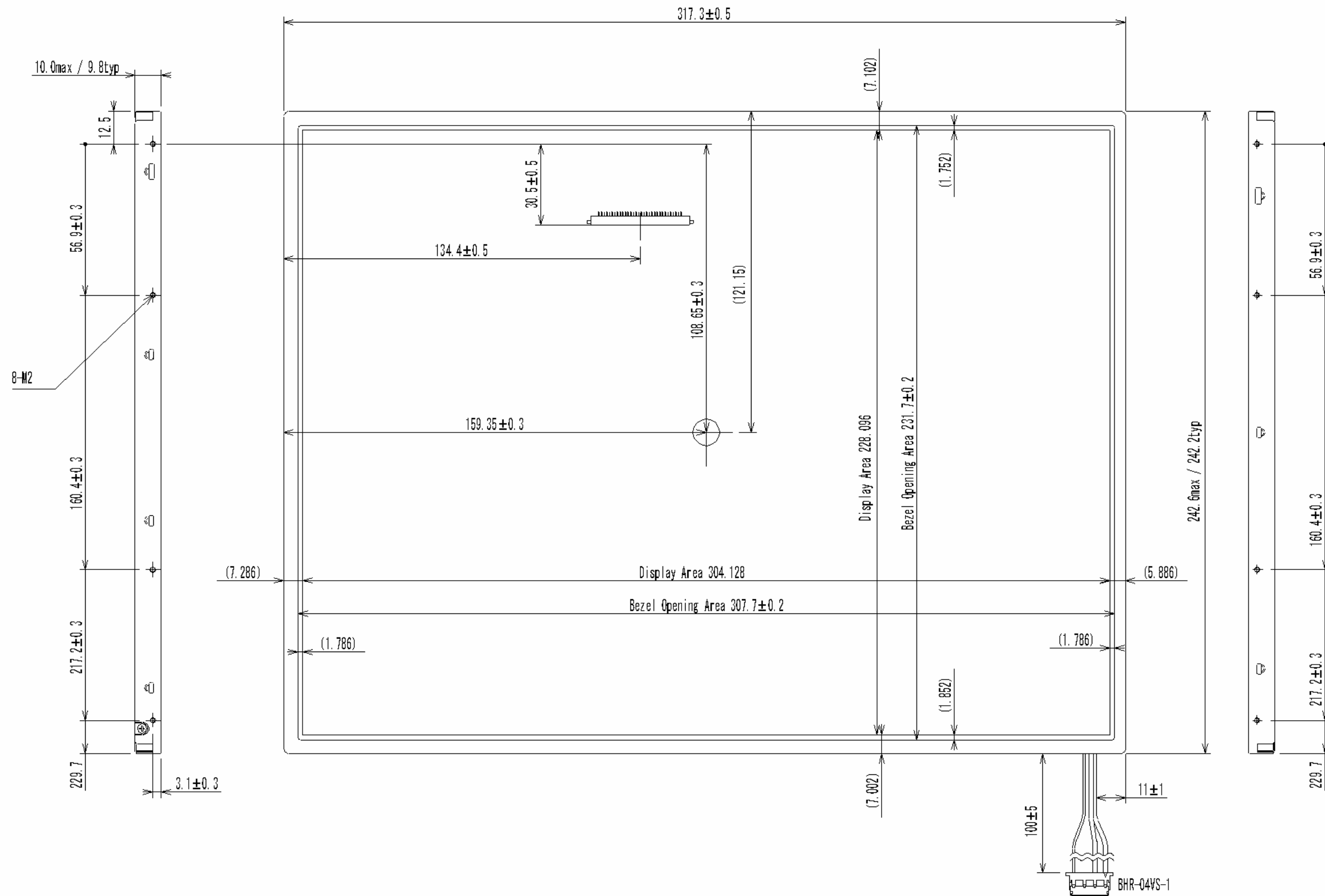
Unit: mm

Note1: The values in parentheses are for reference.

7.2 REAR VIEW
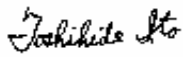

Unit: mm

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-PD-0258	Nov.7, 2003	**Revision contents** New issue **Signature of writer** *Approved by* *Checked by* *Prepared by* T. ITO R. KAWASHIMA
2nd edition	DOD-PD-0306	Dec.5, 2003	**Revision contents** P27, P28 Outline drawings are revised. **Signature of writer** *Approved by* *Checked by* *Prepared by* T. ITO R. KAWASHIMA