# W85C178

# REAL TIME CLOCK (WITH 114-BYTE SRAM)

## GENERAL DESCRIPTION

The W85C178 Real Time Clock with 128-byte RAM is a peripheral device for use with various microprocessors. The W85C178 is designed to be a direct replacement for the MC146818A. The device's functions include a time-of-day clock, an alarm, a one-hundred-year calendar, a square wave generator, programmable interrupts, and 114 bytes of nonvolatile static RAM. The W85C178 uses CMOS technology and interfaces with most microprocessor buses. The device consumes very little power.

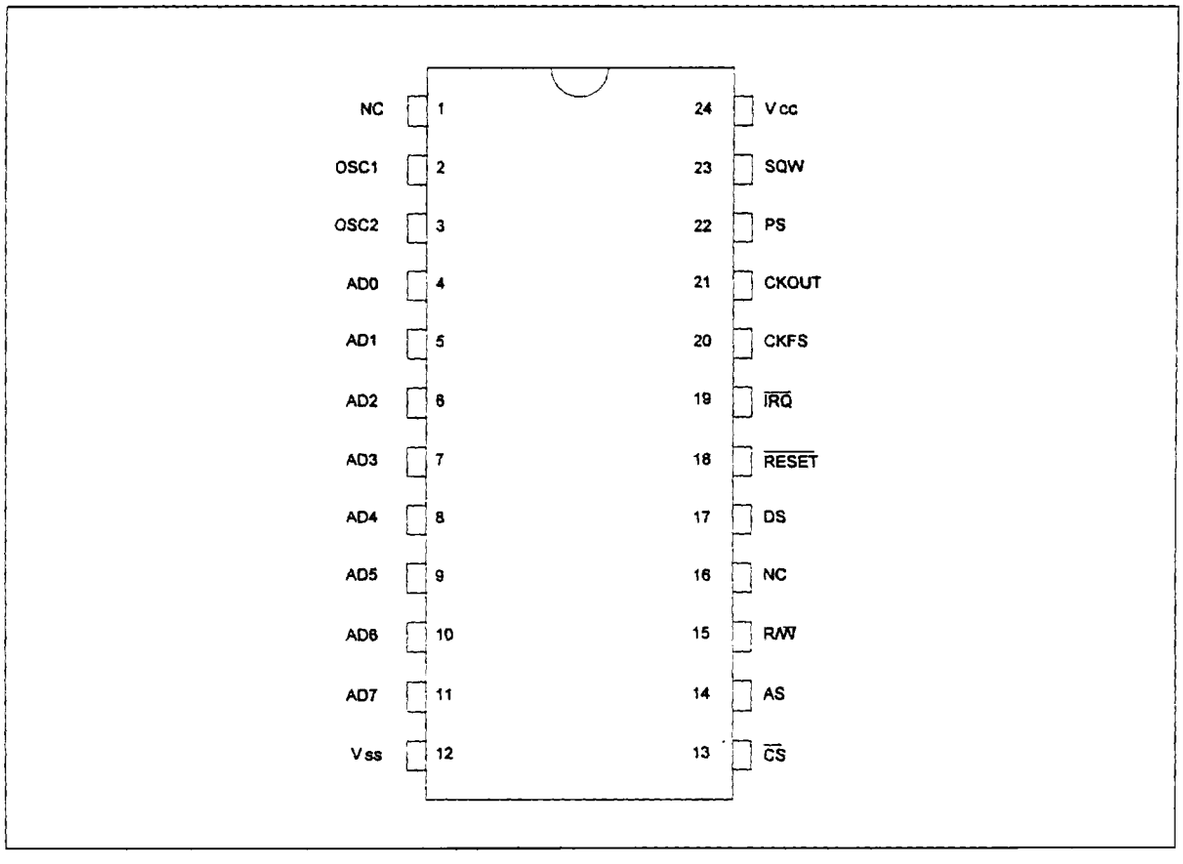
## FEATURES

- 14 bytes of clock and control/status registers
- 114 bytes of general nonvolatile storage
- BCD or binary representation of time, calendar, and alarm registers
- Counts seconds, minutes, hours, days of the week, days of the month, months, years
- 12-hour to 24-hour clock with AM and PM in 12-hour mode
- Daylight savings time option
- Automatic leap-year adjustment
- Programmable square wave output signal
- Time base input option: 4.194304 MHz, 1.048576 MHz, 32.768 KHz
- Automatic end of month recognition
- 24-pin DIP package



*Publication Release Date: October 1994*
*Revision A1*

## PIN CONFIGURATION




## PIN DESCRIPTIONS

### Vcc, Vss

DC power is provided to the device on these pins. The maximum and minimum supply voltages are listed in the electrical characteristics table.

### OSC1, OSC2 - Time Base, Input

Oscilator or crystal frequency at 32.768 KHz, 1.048576 MHz, 4.194304 MHz may be connected to these pins. The internal time base clock to be used is chosen in bit[6:4] of register A.

### AD[7:0] - Multiplexed Address/Data Bus, Bidirectional Data Bus

AD[7:0] is an 8-bit multiplexed address/data bus and bidirectional data bus. The bus cycle consists of two phases. In the first phase, an address placed on AD[7:0] is latched on the falling edge of the AS signal to the internal address decoder. In the second phase, the AD[7:0] bus acts as a bidirectional data bus. AD[7:0] must be valid during writes. The chip will output data on AD[7:0] during a read operation.

### $\overline{CS}$ - Chip Select, Input

The chip select signal must be low when the chip is being accessed.

### AS - Address Strobe, Input

The rising edge of AS latches the state of the DS. The latch automatically creates functionally identical internal read and write enable signals. The falling edge of AS causes the address to be latched within the W85C178.

### R/$\overline{W}$ - Read/Write, Input

The R/$\overline{W}$ pin has two operating modes. A read function is indicated by a high level on R/$\overline{W}$ when DS is high. A write function is indicated by a low on R/$\overline{W}$ when DS is high.

### $\overline{RESET}$ - RESET, Input

The $\overline{RESET}$ pin does not affect the timer, calendar counter, or RAM function. When $\overline{RESET}$ is active, the following occur:

- $\overline{IRQ}$ pin enters high impedance state.
- The interrupt flags (IRQF, PF, AF, UF) in register C are cleared.
- The interrupt enable signals (PE,AE,UE) in register B and the SQW pin are cleared.

### $\overline{IRQ}$ - Interrupt Request, Output Tri-State

$\overline{IRQ}$ is a tri-state output pin which is an active low output to interface. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt enable bit is set. To clear the $\overline{IRQ}$ pin, the processor program normally reads register C. The $\overline{RESET}$ pin also clears pending interrupts.

### CKFS - Clock Out Frequency Select, Input

When the CKFS pin is tied to Vcc, CKOUT is the same frequency as the OSC1 pin. When CKFS is tied to Vss, CKOUT is the OSC1 input frequency divided by four.

### CKOUT - Clock Out, Output

The CKOUT pin is an output equal to the OSC1 frequency divided by 1 or 4.

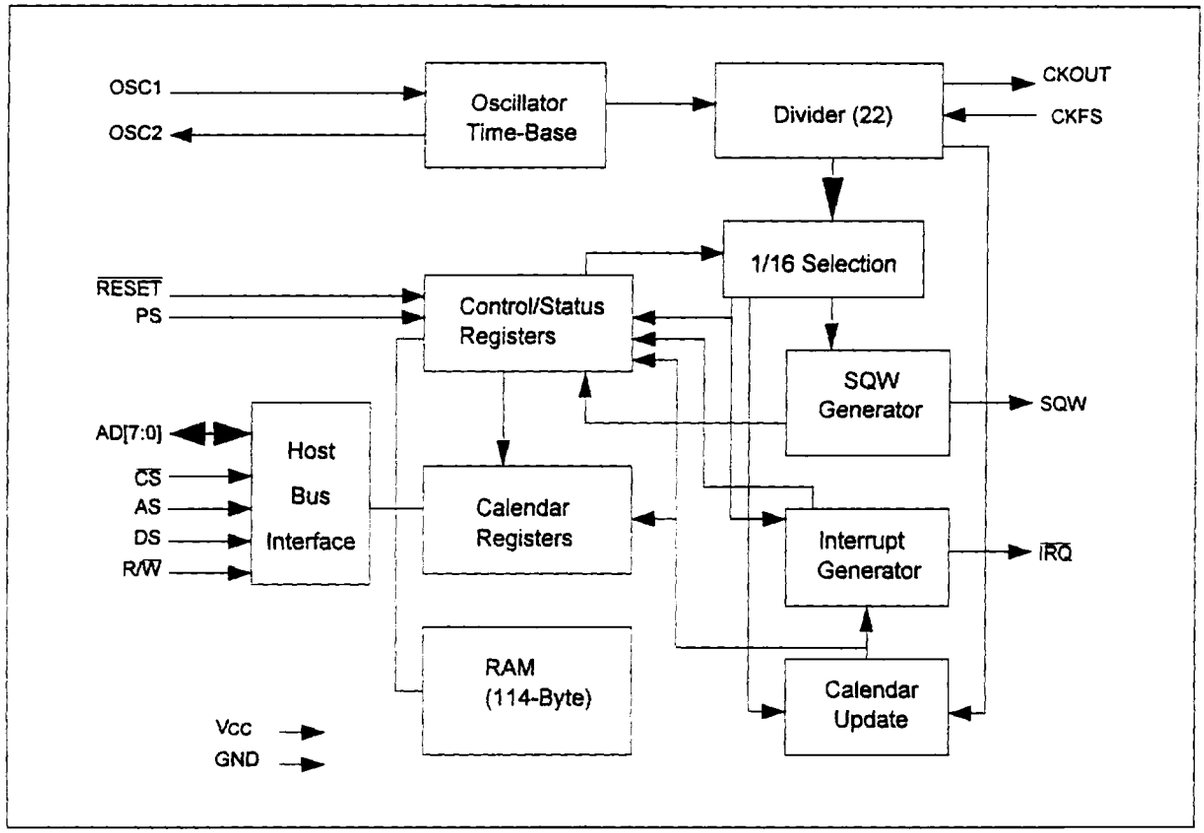
### PS - Power Sense, Input

The PS pin is used in the control of the VRT bit in register D. When the PS pin is low, the VRT bit is cleared to low.

### SQW - Square Wave, Output

SQW outputs a programmable frequency. Any one of the 15 specific frequencies may be selected through register A. This pin is held low when bit 3 of register B is low.

## BLOCK DIAGRAM




## FUNCTIONAL DESCRIPTION

### Address Map

The W85C178 consists of 10 bytes of RAM for the time, calendar, and alarm registers and the control and status bytes and another 114 bytes of general nonvolatile RAM. All 128 bytes can be directly read and written by the host program except for the following:

- Registers C and D are read-only.
- Bit 7 of register A is read-only.

Figure 2 depicts the address map for the W85C178.

**Address Map Table**

| ADDRESS | FUNCTION | BINARY OR BCD CONTENTS |
|---|---|---|
| 0/00 | SECONDS | Yes |
| 1/01 | SECONDS ALARM | Yes |
| 2/02 | MINUTES | Yes |
| 3/03 | MINUTES ALARM | Yes |
| 4/04 | HOURS | Yes |
| 5/05 | HOURS ALARM | Yes |
| 6/06 | DAY OF WEEK | Yes |
| 7/07 | DATE OF MONTH | Yes |
| 8/08 | MONTH | Yes |
| 9/09 | YEAR | Yes |
| 10/0A | REGISTER A | |
| 11/0B | REGISTER B | |
| 12/0C | REGISTER C | |
| 13/0D | REGISTER D | |
| 14/0E<br><br>127/7F | 114 BYTES<br>USER RAM | |

**Time, Calendar, and Alarm Data Modes**

| REGISTER LOCATION | FUNCTION | RANGE (DATA MODE) | | EXAMPLE | |
|---|---|---|---|---|---|
| | | BINARY | BCD | BINARY | BCD |
| 0 | Seconds | 00H-3BH | 00H-59H | 1EH | 30H |
| 1 | Seconds Alarm | 00H-3BH | 00H-59H | 1EH | 30H |
| 2 | Minutes | 00H-3BH | 00H-59H | 0FH | 15H |
| 3 | Minutes Alarm | 00H-3BH | 00H-59H | 0FH | 15H |
| 4 | Hours<br>(12-Hour Mode)<br>(24-Hour Mode) | 01H-0CH (AM)<br>81H-8CH (PM)<br>00H-17H | 01H-12H (AM)<br>81H-92H (PM)<br>00H-23H | 08H<br><br>08H | 08H<br><br>08H |
| 5 | Hours Alarm<br>(12-Hour Mode)<br>(24-Hour Mode) | 01H-0CH (AM)<br>81H-8CH (PM)<br>00H-17H | 01H-12H (AM)<br>81H-92H (PM)<br>00H-23H | 08H<br><br>08H | 08H<br><br>08H |
| 6 | Day of Week | 01H-07H | 01H-07H | 02H | 02H |
| 7 | Day of Month | 01H-1FH | 01H-31H | 04H | 04H |
| 8 | Month | 01H-0CH | 01H-12H | 07H | 07H |
| 9 | Year | 00H-63H | 00H-99H | 5EH | 94H |

Example: 8:15:30AM Monday 4 July 1994

### Update Cycle

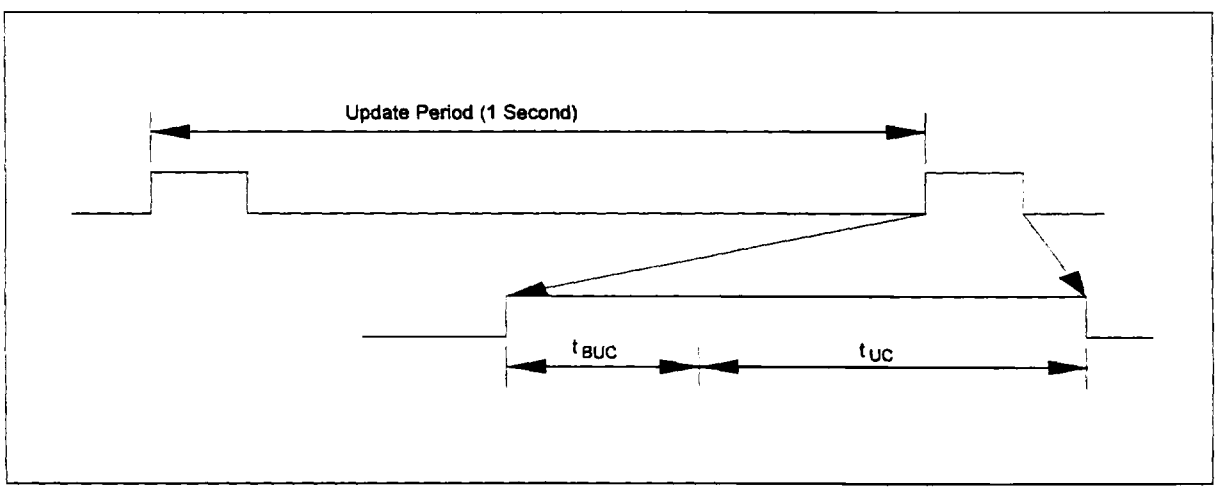
The W85C178 executes an update cycle once per second. During the update cycle, the W85C178 updates the contents of the clock and calendar registers. The update cycle also compares each alarm byte with the corresponding timer byte and generates an alarm flag if a match or a "don't care" condition (0C0Hex) is present in the alarm register.

The update-in-progress bit (UIP) in register A pulses once per second. The update cycle occurs 244 μS after the UIP bit goes high. This bit is cleared and the update-ended flag (UF) is set at the end of the update cycle.

### Update Cycle Times Table

| UIP BIT | OSC1 INPUT | UPDATE CYCLE TIME ($T_{UC}$) | BEFORE UPDATE CYCLE TIME ($T_{BUC}MIN$) |
|---|---|---|---|
| 1 | 4.194304 MHz | 248 μS | - |
| 1 | 1.048576 MHz | 248 μS | - |
| 1 | 32.768 KHz | 1984 μS | - |
| 0 | 4.194304 MHz | - | 244 μS |
| 0 | 1.048576 MHz | - | 244 μS |
| 0 | 32.768 KHz | - | 244 μS |

### Update Period and UIP Timing




### Registers

The W85C178 has four control/status registers, which are accessable at all times.

**Register A**

- All bits are unaffected by $\overline{\text{RESET}}$.

- Register A is a read/write register except for bit 7 (UIP read-only).

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | UIP | DV2 | DV1 | DV0 | RS3 | RS2 | RS1 | RS0 |

UIP–Read-Only Bit

When UIP equals "1," an update cycle is in progress. The UIP is cleared at the end of each update cycle and also cleared when the SET bit in register B is "1."

DV[2:0]–Divider Control

These three bits are used to select various frequencies for the internal divider. The divider chain may be held reset for precision setting. When the divider changes from reset to operating state, the first update cycle takes place 500 mS later. The divider bits are also used to facilitate testing.

Divider Configuration Table

| TIME-BASE FREQUENCY | DV2 | DV1 | DV0 | OPERATION MODE | DIVIDER RESET |
|---|---|---|---|---|---|
| 4.194304 MHz | 0 | 0 | 0 | Yes | - |
| 1.048576 MHz | 0 | 0 | 1 | Yes | - |
| 32.768 KHz | 0 | 1 | 0 | Yes | - |
| - | 1 | 0 | - | No | * |
| - | 1 | 1 | - | No | Yes |

* For test purposes only.

RS[3:0] Periodic Interrupt Rate, Square Wave Output Frequency Selector

Periodic Interrupt Rate, Square Wave Output Frequency Table

| RS[3:0] | TIME BASE | |
|---|---|---|
| 3 2 1 0 | 4.194304 MHZ OR 1.048576 MHZ | 32.768 KHZ |
| 0 0 0 0 | None | |
| 0 0 0 1 | 30.517 µS/32.768 KHz | 3.90625 mS/256 Hz |
| 0 0 1 0 | 61.035 µS/16.384 KHz | 7.8125 mS/128 Hz |
| 0 0 1 1 | 122.070 µS/8.192 KHz | |
| 0 1 0 0 | 244.141 µS/4.096 KHz | |
| 0 1 0 1 | 488.281 µS/2.048 KHz | |
| 0 1 1 0 | 976.562 µS/1.024 KHz | |
| 0 1 1 1 | 1.953125 mS/512 Hz | |
| 1 0 0 0 | 3.90625 mS/256 Hz | |
| 1 0 0 1 | 7.8125 mS/128 Hz | |
| 1 0 1 0 | 15.625 mS/64 Hz | |
| 1 0 1 1 | 31.25 mS/32 Hz | |
| 1 1 0 0 | 62.5 mS/16 Hz | |
| 1 1 0 1 | 125 mS/8 Hz | |
| 1 1 1 0 | 250 mS/4 Hz | |

| | |
|---|---|
| 1 1 1 1 | 500 mS/2 Hz |

**Register B (Read/Write)**

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SET | PE | AE | UE | SE | DM | 24/12 | DSE |

SET

When the SET bit is a "1," any update cycle in progress is aborted and registers (0-9) may be modified without an update occurring. When this bit is a "0," the update cycle function occurs once each second. This bit is not affected by any other internal functions or by $\overline{\text{RESET}}$.

PE

A "1" on the periodic interrupt enable bit causes the periodic interrupt flag (PF) bit in register C to drive the $\overline{\text{IRQ}}$ pin low. A "0" on this bit blocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt. This bit is not modified by any internal functions, but it is cleared to "0" by $\overline{\text{RESET}}$.

AE

A "1" on the alarm enable bit permits the alarm flag (AF) bit in register C to assert the $\overline{\text{IRQ}}$ pin low. A "0" on this bit does not initiate an $\overline{\text{IRQ}}$ signal. The $\overline{\text{RESET}}$ pin clears AE to "0." This bit is not modified by any internal functions.

UE

A "1" on the update-ended interrupt enable bit enables the update-end flag (UF) bit in register C to assert $\overline{\text{IRQ}}$. A "0" on this bit does not initiate an $\overline{\text{IRQ}}$ signal. The UE bit is cleared by the SET bit going high or the $\overline{\text{RESET}}$ pin going low.

SE

A "1" on the square-wave enable bit causes a square-wave signal at the frequency specified in RS[3:0] in register A to appear on the SQW pin. A "0" on this bit causes the SQW pin to be held low. This bit cleared by the $\overline{\text{RESET}}$ pin.

DM

The data mode bit determines whether time and calendar updates are to use binary or binary-coded decimal (BCD) format. A "1" on this bit signifies binary data. A "0" on this bit specifies BCD data. This bit is not modified by $\overline{\text{RESET}}$ pin or by any internal functions.

24/12

A "1" on this bit selects 24-hour mode for the time-of-day function. A "0" on this bit selects 12-hour mode. This bit is not modified by the $\overline{\text{RESET}}$ pin or by any internal function.

DSE

A "1"on this bit allows two special updates:

- On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM.
- On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM

A "0" on this bit disables these special updates. DSE is not changed by any internal operations or by $\overline{\text{RESET}}$.

**Register C (Read Only)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | IRQF | PF | AF | UF | 0 | 0 | 0 | 0 |

IRQF

The interrupt request flag is set to a "1" if one or more of the following are true:
PF * PE = "1"
AF * AE = "1"
UF * UE = "1"
(i.e., IRQF = PF * PE + AF * AE + UF * UE)
Any time the IRQF bit is a "1," the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after this register is read by the program or when the $\overline{RESET}$ pin is low.

PF

The periodic interrupt flag is set to "1" when a rising edge is detected on the selected tap of the divider chain (RS[3:0], register A). PF is set to a "1" independent of the state of the PE bit. This bit is cleared after the $\overline{RESET}$ pin goes low or this register is read by the program.

AF

A "1" on this bit indicates that the current time has reached the alarm time setting. A $\overline{RESET}$ or a read of this register clears the alarm flag.

UF

The update-ended interrupt flag bit is set after each update cycle ends. This bit is cleared by a $\overline{RESET}$ or when this register is read.

B3-B0

These bits all read "0." They cannot be written to.

**Register D (Read Only)**

| Bit | 7 | 6-0 |
|---|---|---|
| Name | VRT | 0 |

VRT

The valid RAM and time bit. A "0" appears on this bit when the PS pin is low, indicating the data integrity of the real time clock and storage registers is not guaranteed. This bit can be set only by reading this register, which is not modified by the $\overline{RESET}$ pin.

### Reading and Writing the W85C178

```
Read:     mov   al,index      ; load address value
          mov   dx,RTC        ; load RTC index port
          out   dx,al         ; generate AS
          ...
          mov   dx,RTC+1      ; load RTC data port
          in    al,dx         ; generate DS, get data
          ...

Write:    mov   al,index      ; load address value
          mov   dx,RTC        ; load RTC index port
          out   dx,al         ; generate AS
          ...
          mov   al,data       ; load write data
          mov   dx,RTC+1      ; load RTC data port
          out   dx,al         ; generate WR, store data
```

## ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$)

| RATINGS | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to + 8.0 | V |
| All Input Voltages (Except OSC1) | $V_{IN}$ | $V_{SS}$ - 0.5 to $V_{DD}$ + 0.5 | V |
| Operating Temperature Range | $T_A$ | 0 to 70 | °C |
| Storage Temperature Range | $T_{STG}$ | -40 to 70 | °C |

## D.C. CHARACTERISTICS

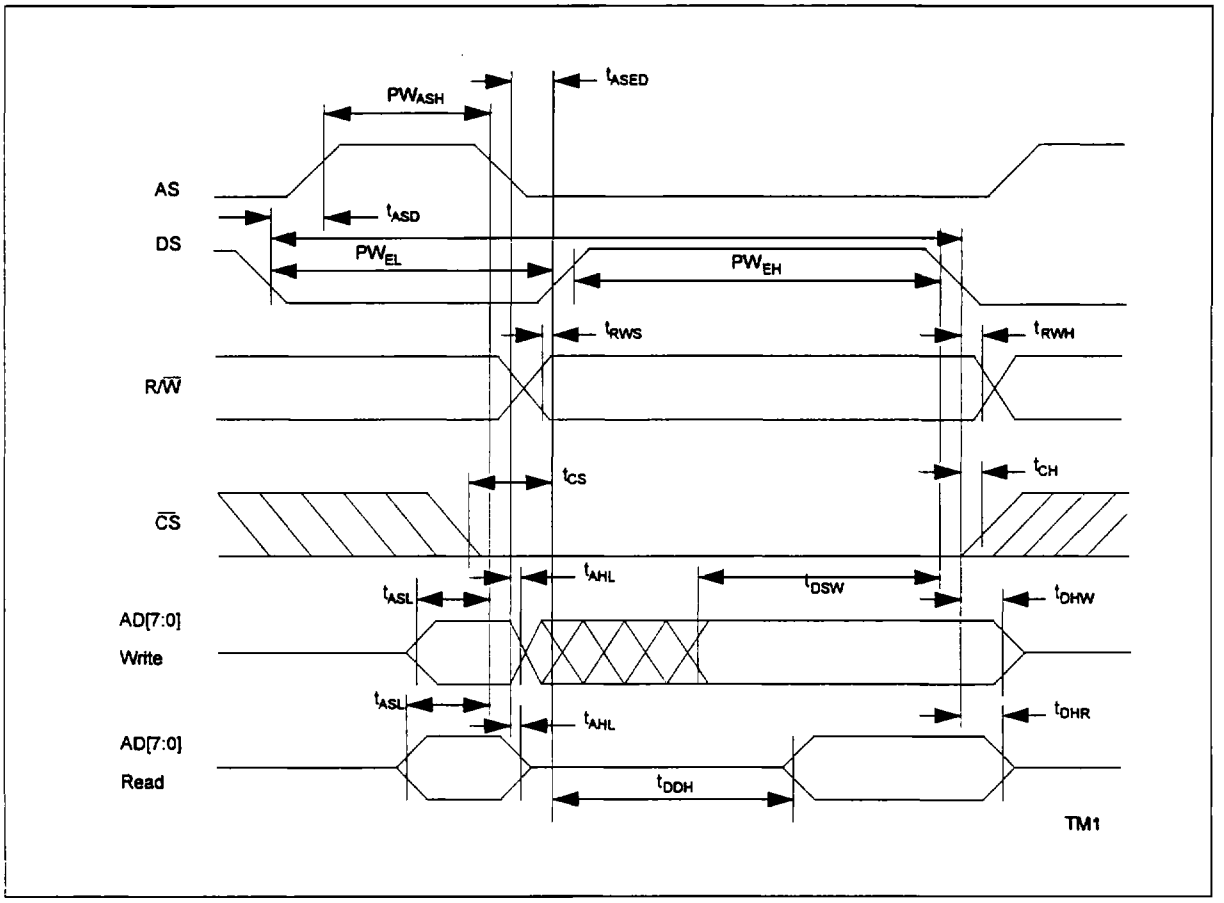
| CHARACTERISTICS | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Power Supply Current (with no load) | $I_{CC}$ | | 15 | mA |
| Output Low Voltage ($I_{load}$ = 2 mA) | $V_{OL}$ | - | 0.4 | V |
| Output High voltage ($I_{load}$ = -1 mA) | $V_{OH}$ | 2.4 | - | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | 0.8 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | $V_{CC}$ + 0.3 | V |
| Input Current (DS, AS, R/W) | $I_I$ | -1 | 1 | mA |
| Input Leakage Current | $I_{LI}$ | -1 | 1 | uA |
| I/O Leakage Current (SQW,/IRQ, AD[7:0]) | $I_{LIO}$ | -1 | 1 | uA |

## A.C. CHARACTERISTICS

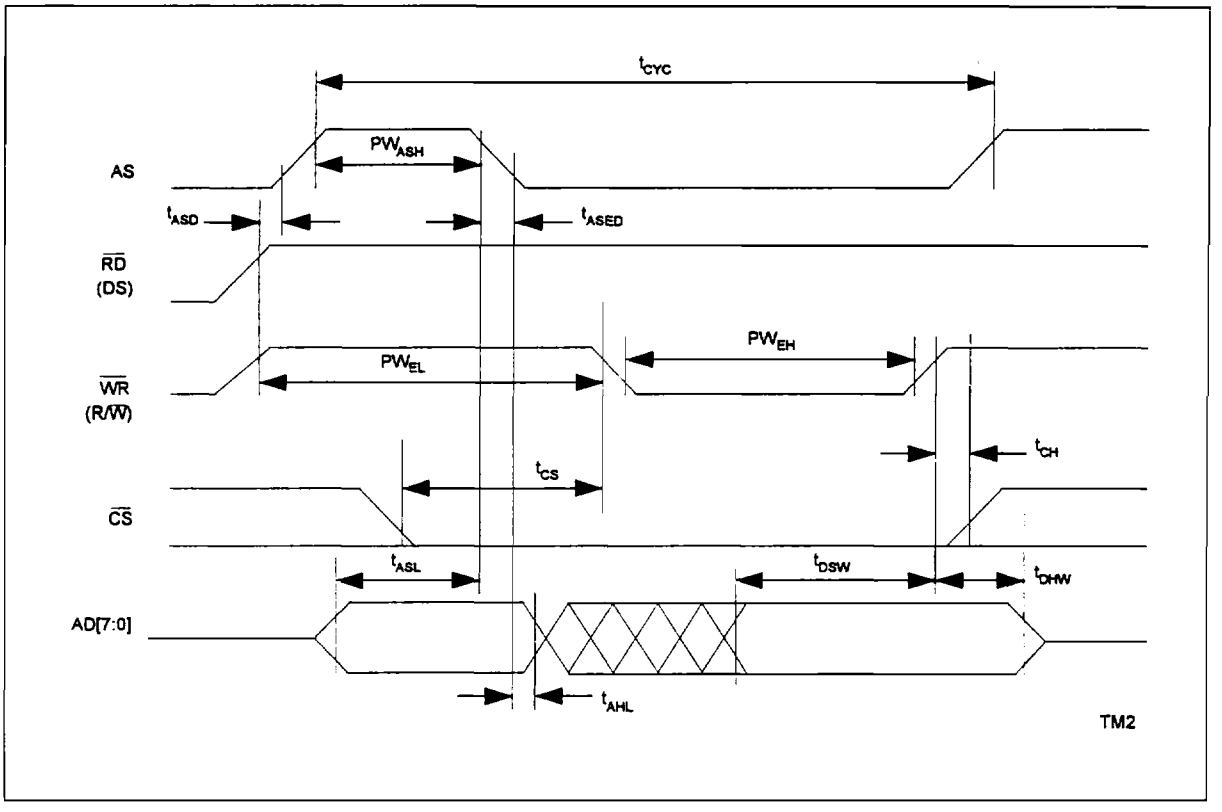
| CHARACTERISTICS | SYMBOLS | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| Cycle Time | $t_{CYC}$ | 200 | DC | nS |
| Pulse Width (DS Low or $\overline{RD}$ High) | $PW_{EL}$ | 150 | - | nS |
| Pulse Width (DS High or $\overline{WR}$ Low) | $PW_{EH}$ | 100 | - | nS |
| Input Rise, Fall Time | $t_R$,$t_F$ | - | 30 | nS |
| R/$\overline{W}$ Hold Time | $t_{RWH}$ | 10 | - | nS |
| R/$\overline{W}$ Setup Time Before DS | $t_{RWS}$ | 10 | - | nS |
| $\overline{CS}$ Active Setup Time Before AS Fall | $t_{CS}$ | 0 | 30 | nS |
| $\overline{CS}$ Active Hold Time | $t_{CH}$ | 0 | - | nS |
| Read Data Hold Time | $t_{DHR}$ | 10 | 1000 | nS |
| Write Data Hold Time | $t_{DHW}$ | 0 | - | nS |
| Muxed Address Valid Time to AS Fall | $t_{ASL}$ | 25 | - | nS |
| Muxed Address Hold Time | $t_{AHL}$ | 10 | - | nS |
| Dealy Time DS to AS Rise | $t_{ASD}$ | 50 | - | nS |
| Pulse Width, AS High | $PW_{ASH}$ | 50 | - | nS |
| Delay Time, AS to DS Rise | $t_{ASED}$ | 50 | - | nS |
| Output Data Delay Time from Read | $t_{DDR}$ | 15 | 30 | nS |
| Data Setup Time | $t_{DSW}$ | 50 | - | nS |

## TIMING WAVEFORMS

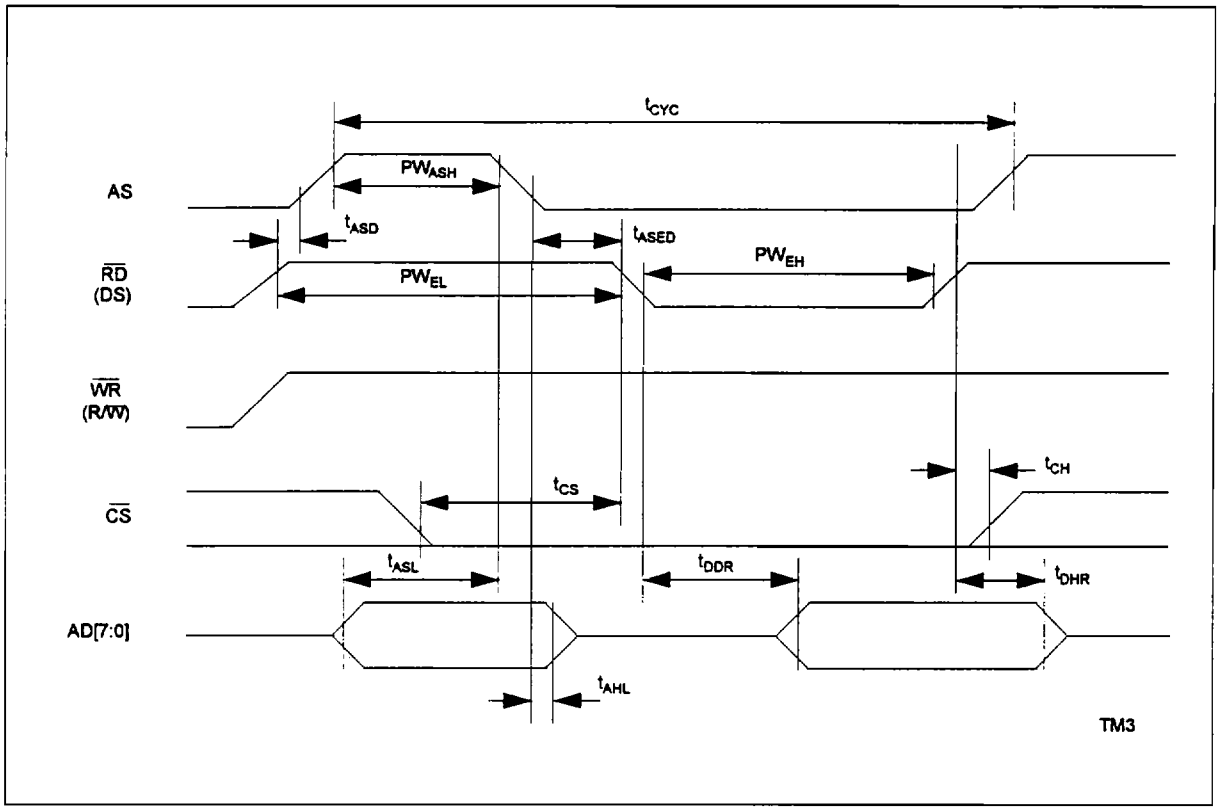
### BUS TIMING FOR MOTOROLA INTERFACE



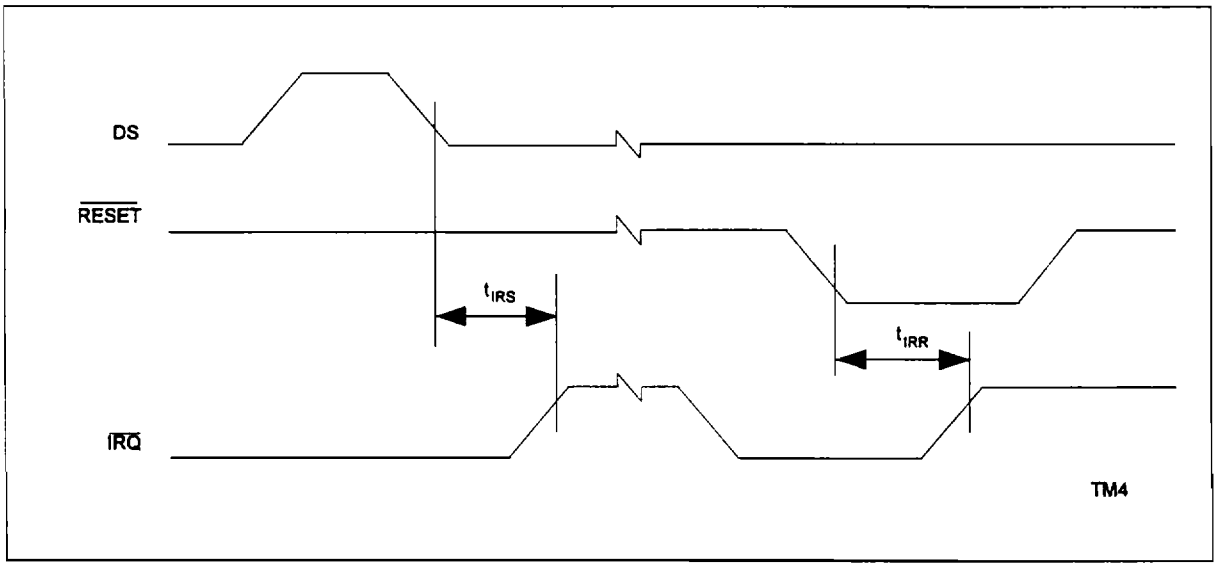
## WRITE BUS TIMING FOR INTEL INTERFACE



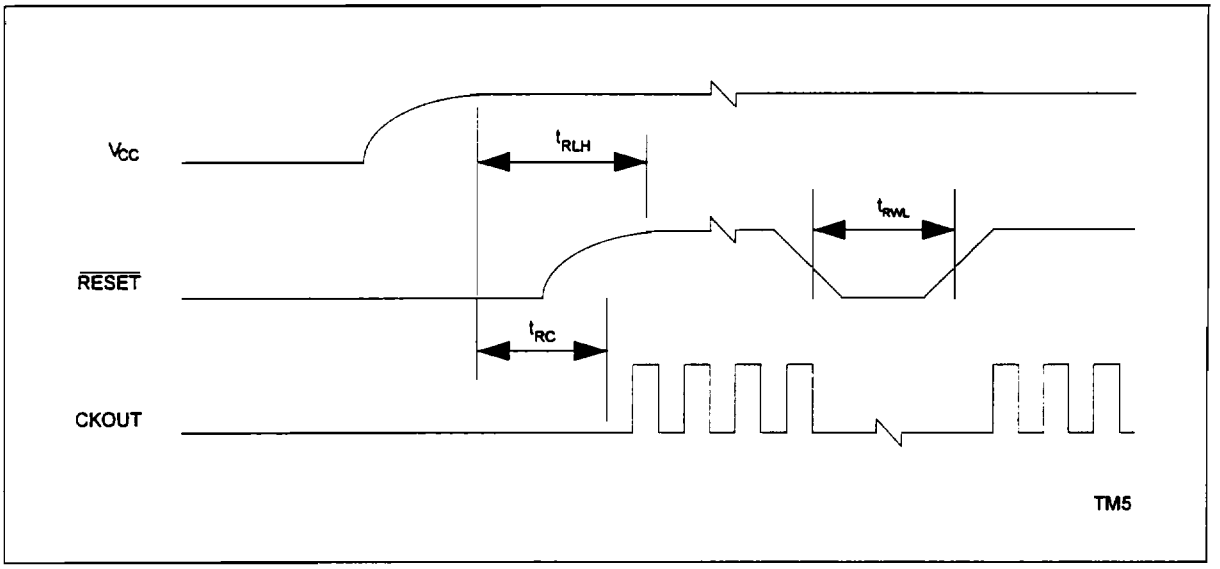
## READ BUS TIMING FOR INTEL INTERFACE



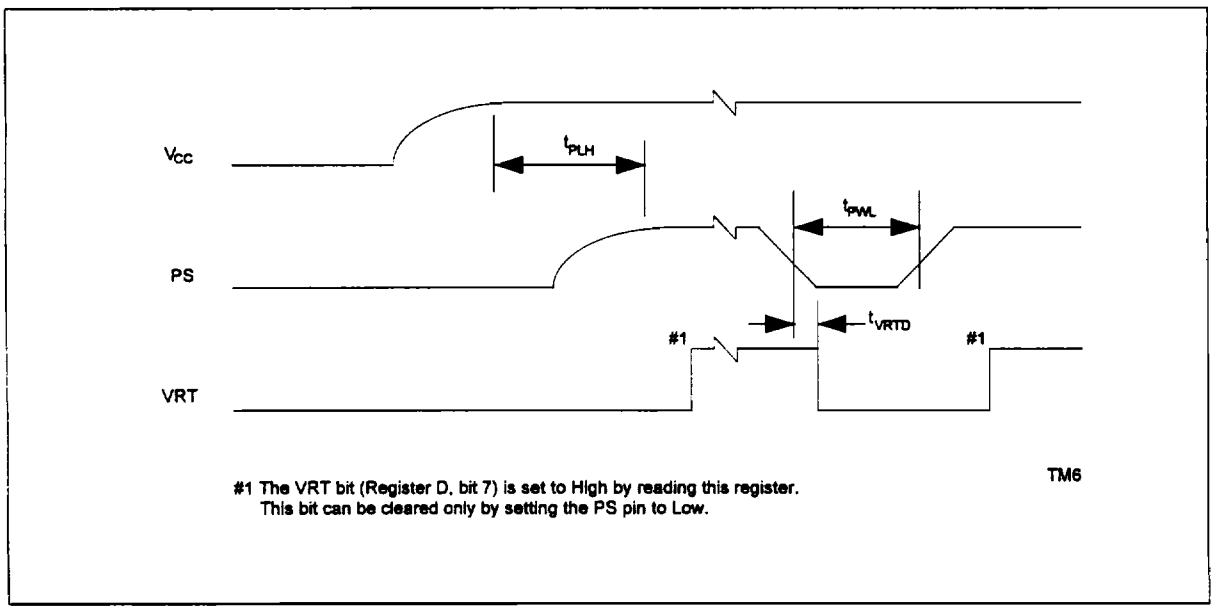

## IRQ RELEASE DELAY



## POWER UP

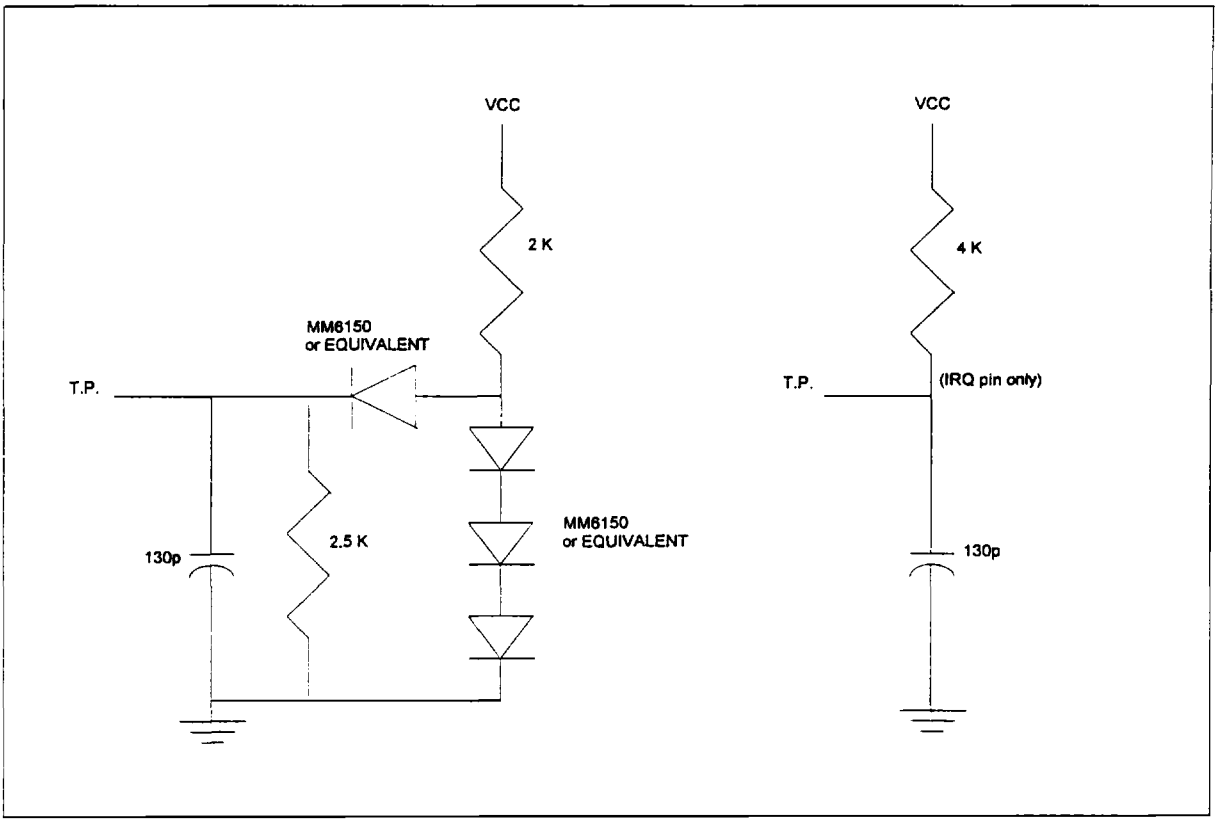



## VRT BIT CONDITION




#1 The VRT bit (Register D, bit 7) is set to High by reading this register. This bit can be cleared only by setting the PS pin to Low.

## OUTPUT LOAD


VCC
2 K
MM6150
or EQUIVALENT
T.P.
130p
2.5 K
MM6150
or EQUIVALENT
VCC
4 K
T.P.
(IRQ pin only)
130p