SOLID STATE OPTRONICS

SDN137

Digital High Speed Optocoupler
10MBd, Logic Output

Description

The SDN137 consists of a high efficient AlGaAs Light Emitting Diode and a high speed optical detector. This design provides excellent AC and DC isolation between the input and output sides of the Optocoupler.

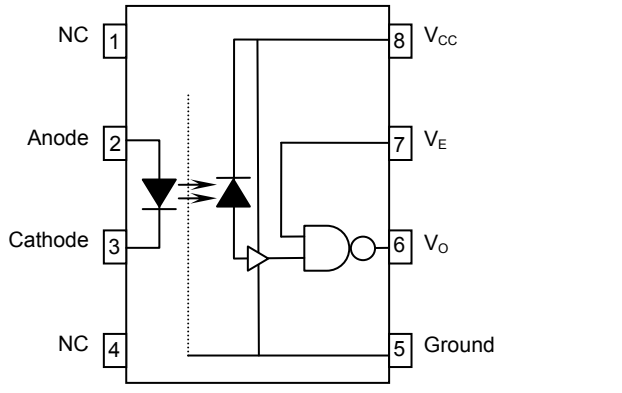
The output of the optical detector features an open collector Schottky clamped transistor. The enable function allows the optical detector to be strobed. The internal shield ensures high common mode transient immunity. A guaranteed common mode transient immunity is up to 15,000V/μS.

The SDN137 comes standard in an 8 pin DIP package.

Applications

- High Speed Logic Ground Isolation
- Replace Slower Speed Optocouplers
- Line Receivers
- Power Transistor Isolation
- Pulse Transformer Replacement
- Switch Mode Power Supplies
- Digital Fieldbus Isolation
- Ground Isolation – Analog Signals

Schematic Diagram



SCN137

Truth Table
(Positive Logic)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	L
OFF	NC	H

**** A 0.1μF bypass Capacitor must be connected between pins 5 & 8 (GND & V_{CC})**

Features

- TTL Compatible
- High Bit Rate: 10MBd
- High CMR Performance (15kV/μS)
- High Isolation Voltage (5000V_{RMS})
- High Common Mode Interference Immunity
- RoHS / Pb-Free / REACH Compliant

Agency Approvals

UL / C-UL:	File # E201932
VDE:	File # 40035191 (EN 60747-5-2)

Absolute Maximum Ratings

The values indicated are absolute stress ratings. Functional operation of the device is not implied at these or any conditions in excess of those defined in electrical characteristics section of this document. Exposure to absolute Maximum Ratings may cause permanent damage to the device and may adversely affect reliability.

Storage Temperature .....-55 to +125°C
Operating Temperature .....-40 to +85°C
Continuous Input Current.....40mA
Transient Input Current 400mA
Reverse Input Control Voltage 5V
Max Enable Input Voltage (V_E) 5V
Max Enable Input Current (I_E) 5mA
Input Power Dissipation 40mW
Max Supply Voltage (V_{CC}) 7V
Max Output Collector Current (I_O) 50mA
Max Output Collector Voltage (V_O) 7V
Output Power Dissipation 85mW

Ordering Information

Part Number	Description
SDN137	8 pin DIP, (50/Tube)
SDN137-H	0.40" (10.16mm) Lead Spacing (VDE0884)
SDN137-S	8 pin SMD, (50/Tube)
SDN137-STR	8 pin SMD, Tape and Reel (1000/Reel)

NOTE: Suffixes listed above are not included in marking on device for part number identification

Electrical Characteristics, T_A = 25°C (unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Specifications						
Input Forward Voltage	V_F	-	1.36	1.70	V	I_F = 10mA
Input Forward Voltage Temp Coefficient	$\Delta V_F/\Delta T$	-	-1.5	-	mV/°C	I_F = 10mA
Input Reverse Voltage	BV_R	5	-	-	V	I_R = 10µA
Input Threshold Current	I_{TH}	-	1.1	5	mA	V_E=2V, VCC=5.5V, I_{OL}(sinking)=13mA
Input Capacitance	C_{IN}	-	34	-	pF	f=1MHz, V_F=0V
Output Specifications, V_{CC} = 5V (unless otherwise specified)						
High Level Supply Current	I_{CCH}	-	7.4	10	mA	V_E=0.5V, V_{CC}=5.5V, I_F=0mA
Low Level Supply Current	I_{CCL}	-	10	13	mA	V_E=0.5V, V_{CC}=5.5V, I_F=10mA
High Level Enable Current	I_{EH}	-	-0.6	-1.6	mA	V_E=2V
Low Level Enable Current	I_{EL}	-	-0.9	-1.6	mA	V_E=0.5V
High Level Enable Voltage	V_{EH}	2	-	-	V	
Low Level Enable Voltage	V_{EL}	-	-	0.8		
High Level Output Current	I_{OH}	-	-	100	µA	V_E=2V, V_{CC}=5.5V, V_O=5.5V, I_F=250µA
Low Level Output Voltage	V_{OL}	-	0.28	0.60	V	V_E=2V, VCC=5.5V, I_F=5mA I_{OL}(sinking)=13mA
Switching Specifications, V_{CC} = 5V, I_F=7.5mA (unless otherwise specified)						
Propagation Delay Time to Low Output Level	t_{PHL}	25	35	100	nS	R_L=350Ω, C_L=15pF
Propagation Delay Time to High Output Level	t_{PLH}	25	45	100	nS	R_L=350Ω, C_L=15pF
Pulse Width Distortion	$\lvert t_{PLH} - t_{PHL} \rvert$	-	10	35	nS	R_L=350Ω, C_L=15pF
Propagation Delay Skew	t_{PSK}	-	8	40	nS	R_L=350Ω, C_L=15pF
Output Rise Time (10% - 90%)	t_r	-	20	-	nS	R_L=350Ω, C_L=15pF
Output Fall Time (90% - 10%)	t_f	-	8	-	nS	R_L=350Ω, C_L=15pF
Propagation Delay Time of enable from V_{EH} to V_{EL}	t_{ELH}	-	22	-	nS	R_L=350Ω, C_L=15pF, V_{EL}=0V, V_{EH}=3V
Propagation Delay Time of enable from V_{EL} to V_{EH}	t_{EHL}	-	12	-	nS	R_L=350Ω, C_L=15pF, V_{EL}=0V, V_{EH}=3V
Logic High Common Mode Transient Immunity	$\lvert CM_H \rvert$	5,000	-	-	V/µS	$\lvert V_{CM} \rvert$=20V, V_{CC}=5V, I_F=0mA, $V_{O\ (MIN)}$=2V, R_L=350Ω
Logic Low Common Mode Transient Immunity	$\lvert CM_L \rvert$	5,000	-	-	V/µS	$\lvert V_{CM} \rvert$=20V, V_{CC}=5V, I_F=7.5mA, $V_{O\ (MIN)}$=0V, R_L=350Ω

Electrical Characteristics, continued… T_A = 25°C (unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Isolation Specifications						
Input-Output Insulation Leakage Current	I_{I-O}	-	-	1.0	µA	45% RH, t=5s, V_{I-O}=3kV
Withstand Insulation Test Voltage	V_{ISO}	5000	-	-	V_{RMS}	RH ≤ 50%, t=1min
Input-Output Resistance	R_{I-O}	-	10^{12}	-	Ω	V_{I-O} = 500V_{DC}
Input-Output Capacitance	C_{I-O}	-	1.0	-	pF	f=1MHz

Notes

1. A 0.1µF or bigger bypass capacitor for V_{CC} is needed as shown in Figure 1
2. Peaking driving circuit may be used to speed up the LED. The peak drive current of LED may go up to 50mA and maximum pulse width 50ns, as long as average current doesn't exceed 20mA.
3. t_{PLH} (propagation delay) is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
4. t_{PHL} (propagation delay) is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
5. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the falling edge of the enable input pulse to the 1.5 V point on the rising edge of the output pulse.
6. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the rising edge of the enable input pulse to the 1.5 V point on the falling edge of the output pulse.
7. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_O > 2.0 V).
8. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_O < 0.8 V).
9. No external pull up is required for a high logic state on the enable input. If the enable pin is not used, tying it to V_{CC}.
10. Device is considered a two-terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
11. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage 3000 V_{RMS} for one second (leakage current less than 5 µA). This test is performed before the 100% production test for partial discharge
12. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage 6000 V_{RMS} for one second (leakage current less than 5 µA). This test is performed before the 100% production test for partial discharge

Recommended Operating Conditions, T_A = 25°C (unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Operating Temperature	°C	-40	-	85	°C	
Supply Voltage	V_{CC}	4.5	-	5.5	V	
Low Level Input Current	I_{FL}	0	-	250	µA	
High Level Input Current	I_{FH}	5	-	15	mA	
Low Level Enable Voltage	V_{EL}	0	-	0.8	V	
High Level Enable Voltage	V_{EH}	2	-	V_{CC}	V	
Output Pull Up Resistor	R_L	330	-	4k	Ω	
Fan Out	N	-	-	5	-	R_L = 1kΩ

SDN137 Electrical Test Circuits

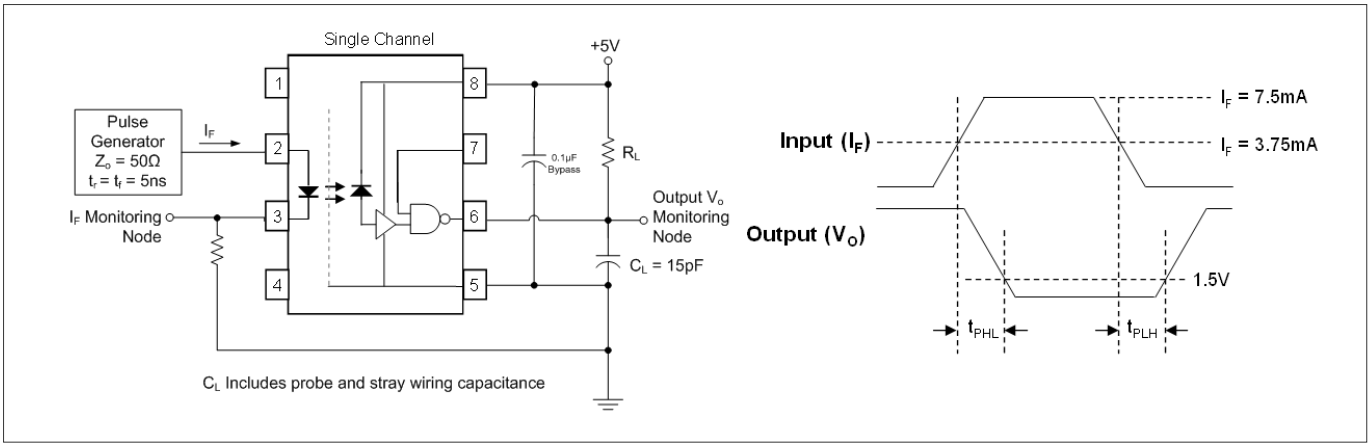


Figure 1: *Single Channel Test Circuit for t_{PHL} and t_{PLH}*

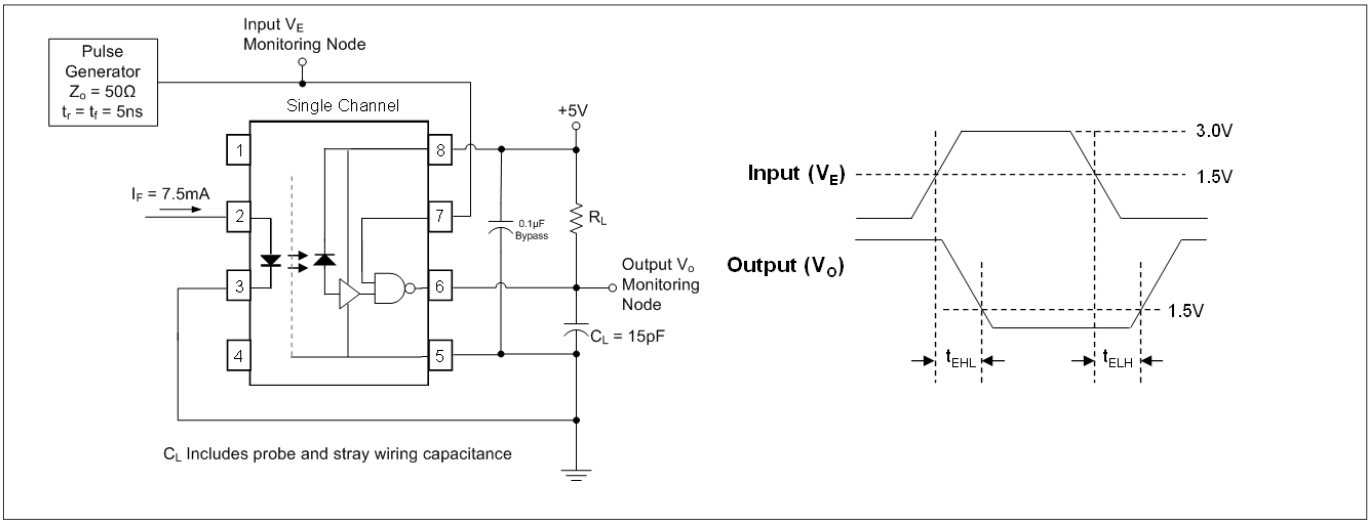


Figure 2: *Single Channel Test Circuit for t_{EHL} and t_{ELH}*

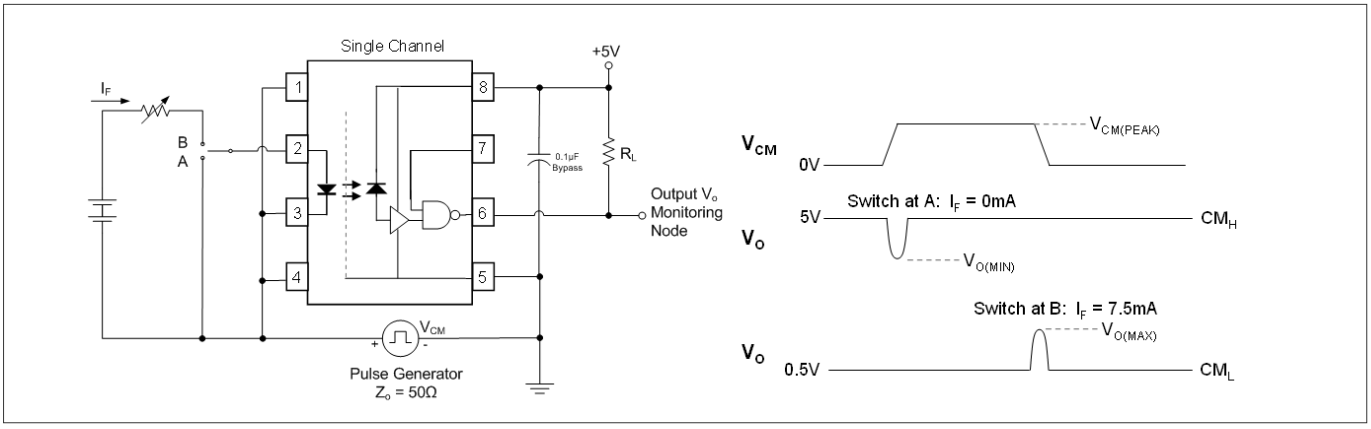


Figure 3: *Single Channel Test Circuit for Common Mode Transient Immunity*

SDN137 Performance & Characteristics Plots, T_A = 25°C (unless otherwise specified)

Figure 4: *Input Diode Forward Characteristics*

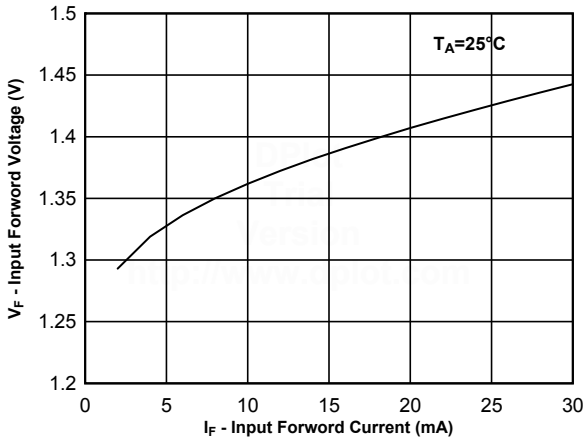


Figure 5: *Input Diode Forward Voltage vs. Temperature*

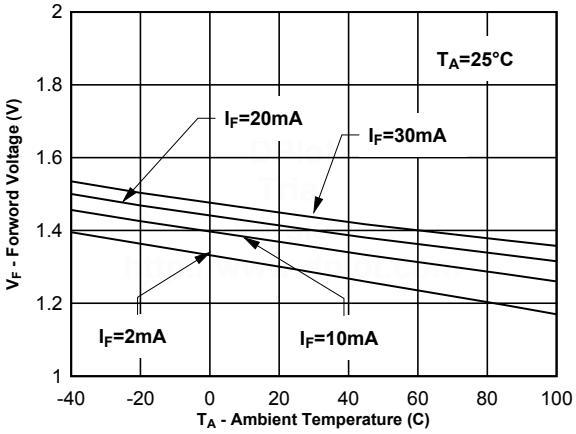


Figure 6: *Input Diode Threshold Current vs. Temperature*

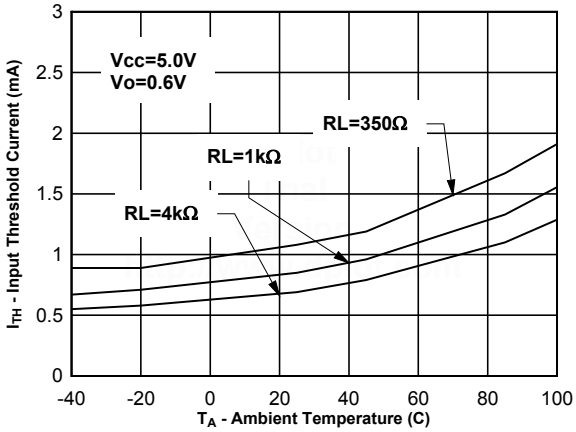


Figure 7: *Output Voltage vs. Input Forward Current*

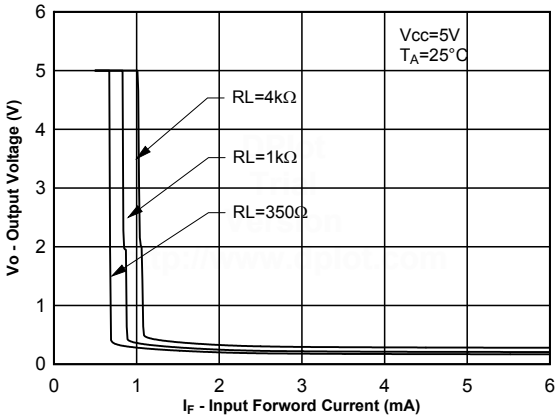


Figure 8: *Low Level Output Voltage vs. Temperature*

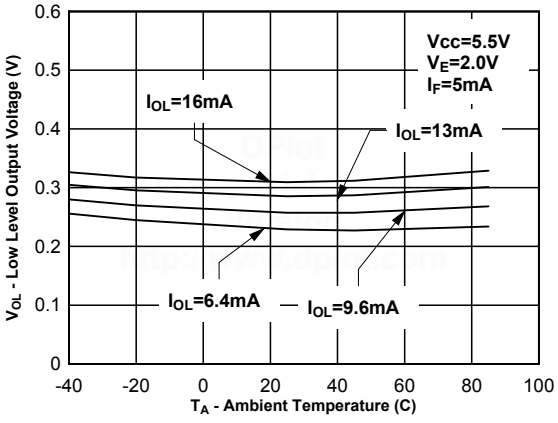
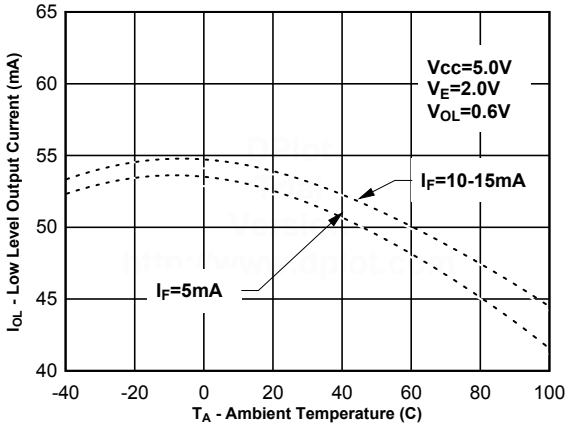


Figure 9: *Low Level Output Current vs. Temperature*



SDN137 Performance & Characteristics Plots, T_A = 25°C (unless otherwise specified)

Figure 10: *Enable Propagation Delay vs. Temperature*

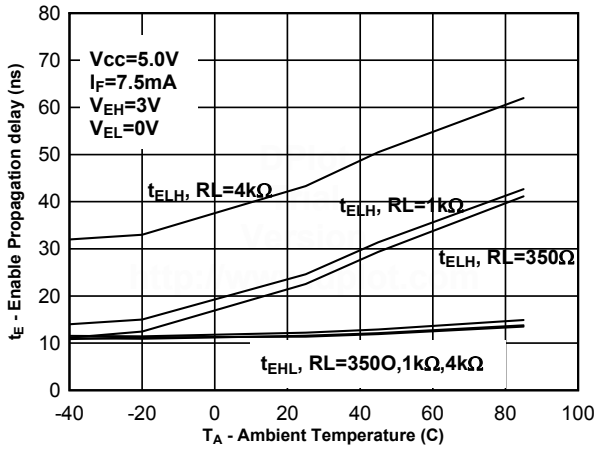


Figure 11: *Rise and Fall Time vs. Temperature*

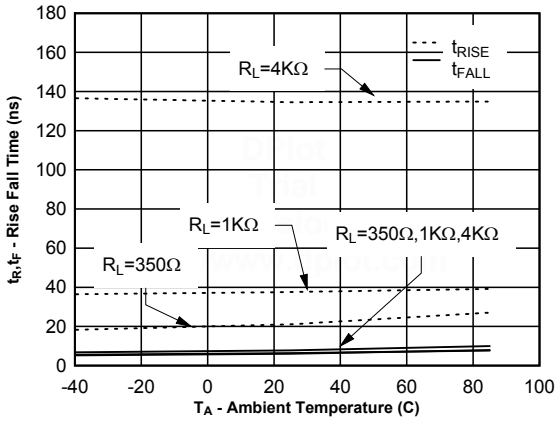


Figure 12: *Propagation Delay Time vs. Temperature*

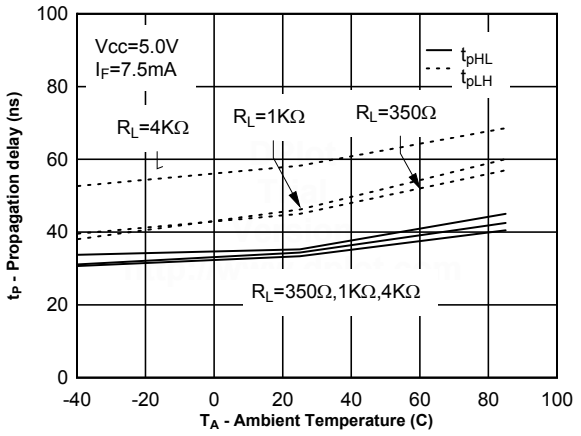


Figure 13: *Propagation Delay vs. Input Forward Current*

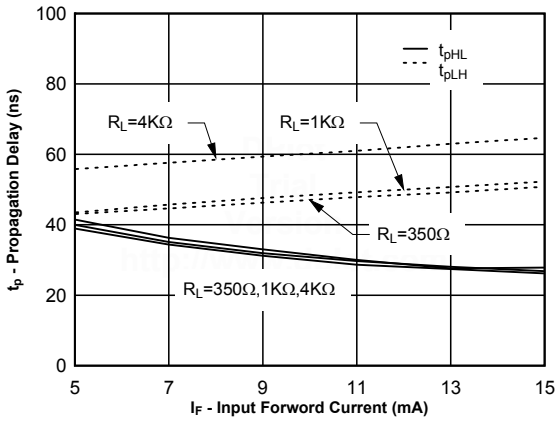


Figure 14: *Pulse Width Distortion vs. Input Forward Current*

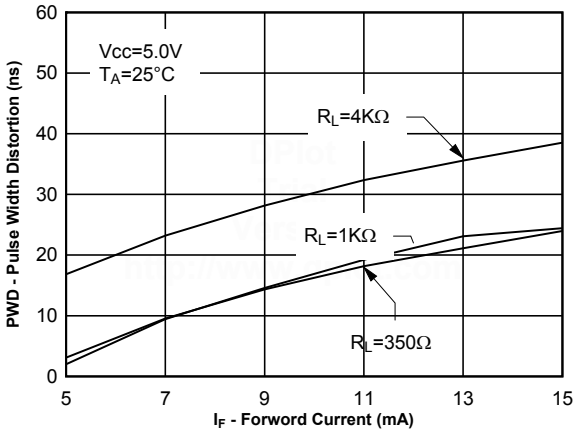
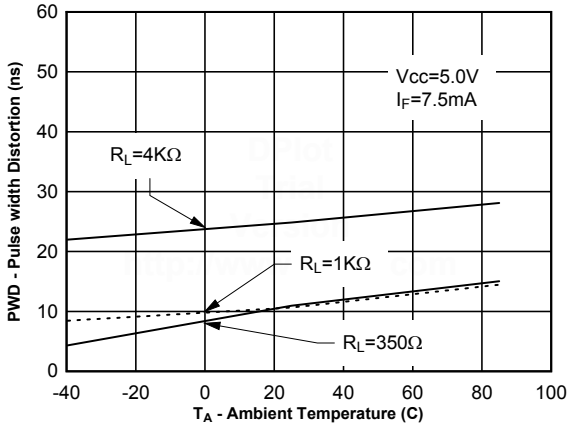


Figure 15: *Pulse Width Distortion vs. Temperature*



SDN137 Solder Reflow Temperature Profile Recommendations

(1) *Infrared Reflow:*

Refer to the following figure as an example of an optimal temperature profile for single occurrence infrared reflow. Soldering process should not exceed temperature or time limits expressed herein. Surface temperature of device package should not exceed 250ºC:

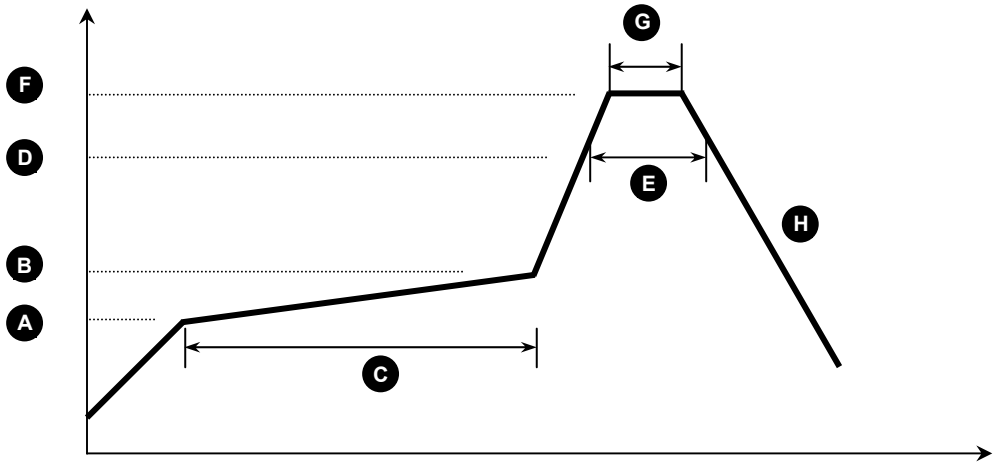


Figure 16

Process Step	Description	Parameter
A	Preheat Start Temperature (ºC)	150ºC
B	Preheat Finish Temperature (ºC)	180ºC
C	Preheat Time (s)	90 - 120s
D	Melting Temperature (ºC)	230ºC
E	Time above Melting Temperature (s)	30s
F	Peak Temperature, at Terminal (ºC)	260ºC
G	Dwell Time at Peak Temperature (s)	10s
H	Cool-down (ºC/s)	<6ºC/s

(2) *Wave Solder:*

Maximum Temperature:	260ºC (at terminal)
Maximum Time:	10s
Pre-heating:	100 - 150ºC (30 - 90s)
Single Occurrence	

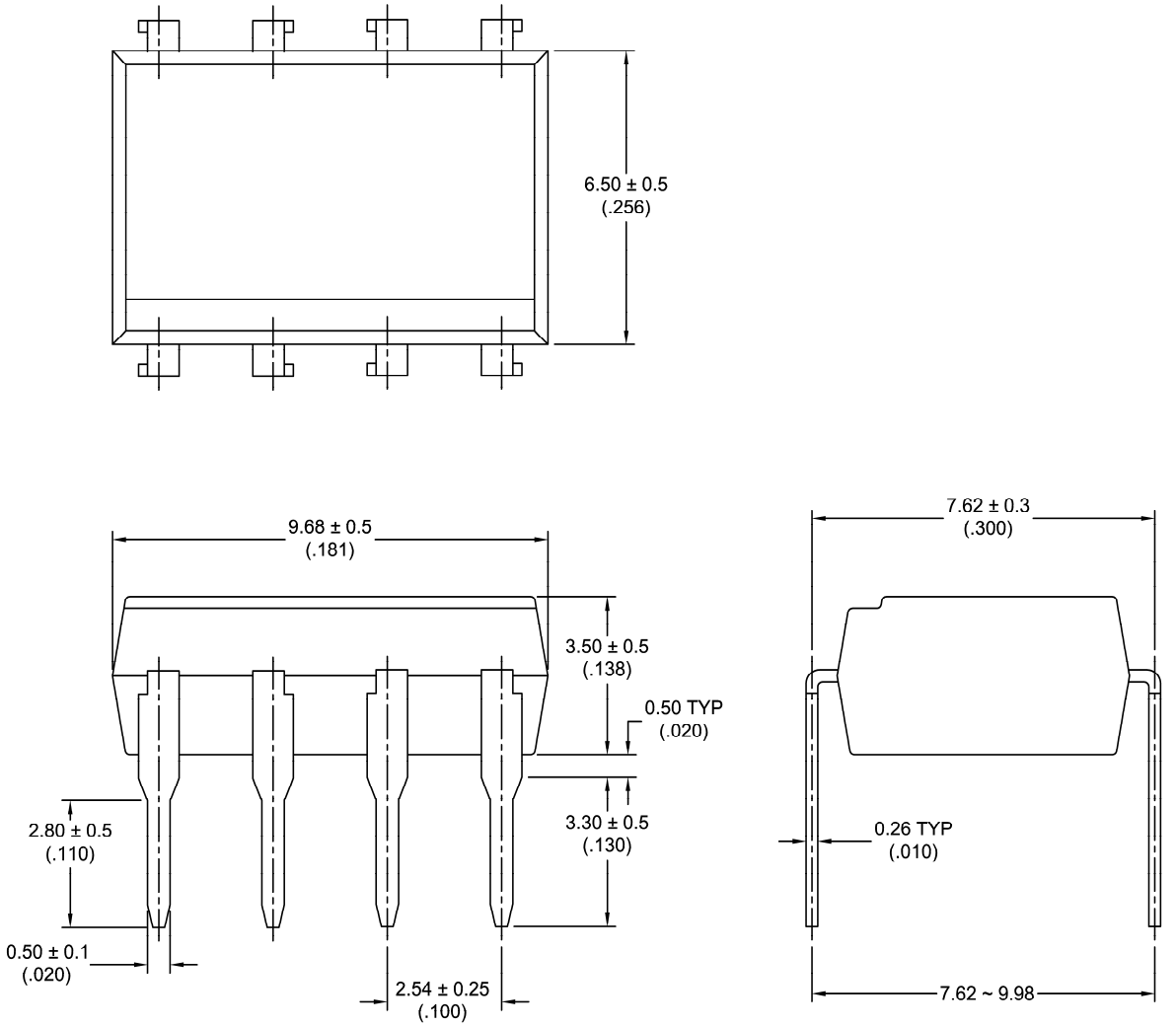
(3) *Hand Solder:*

Maximum Temperature:	350ºC (at tip of soldering iron)
Maximum Time:	3s
Single Occurrence	

SDN137 Package Dimensions

8 PIN DIP Package

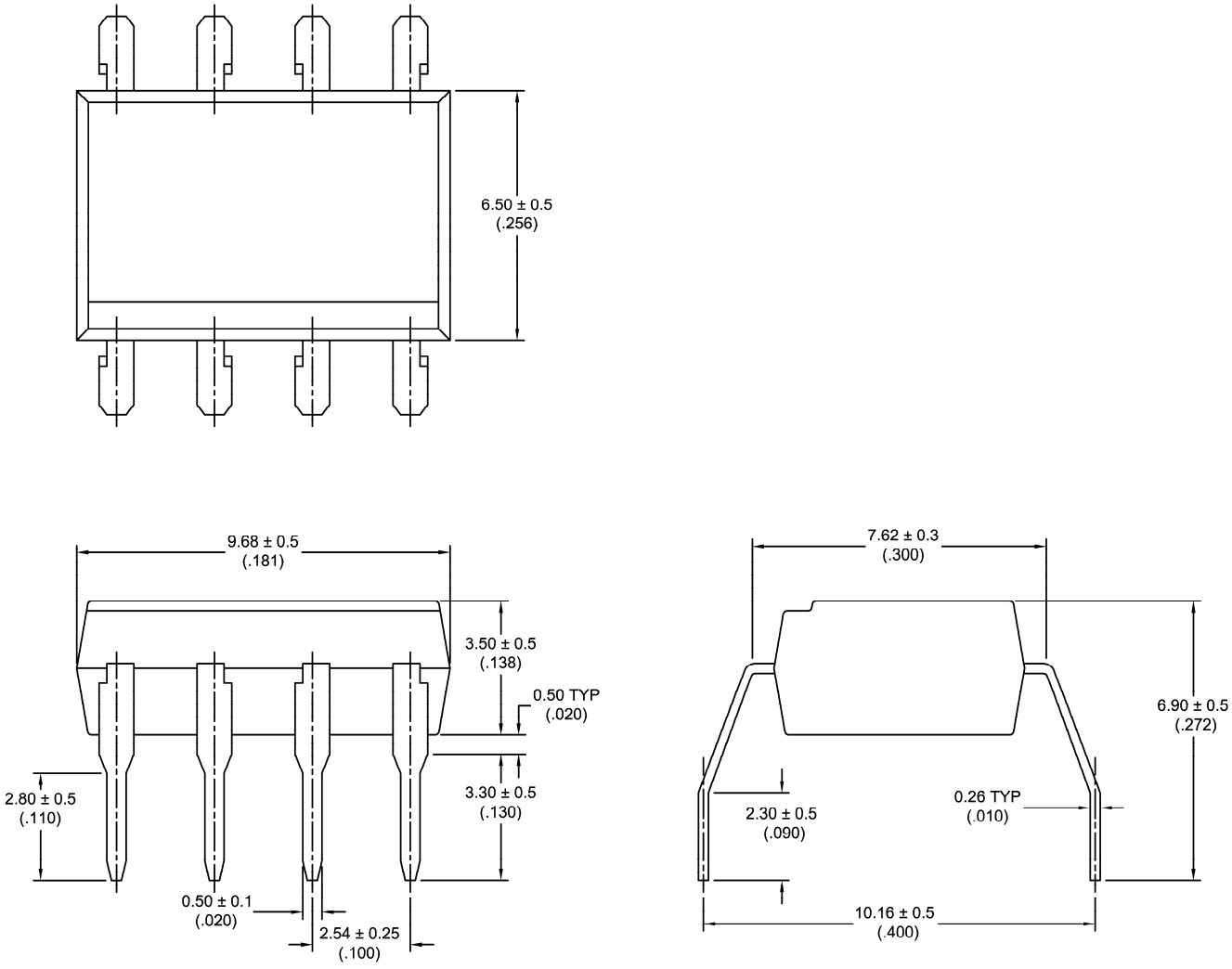
Note: *All dimensions in millimeters [mm] with inches in parenthesis ()*



SDN137 Package Dimensions

8 PIN WIDE Lead Space Package (-H)

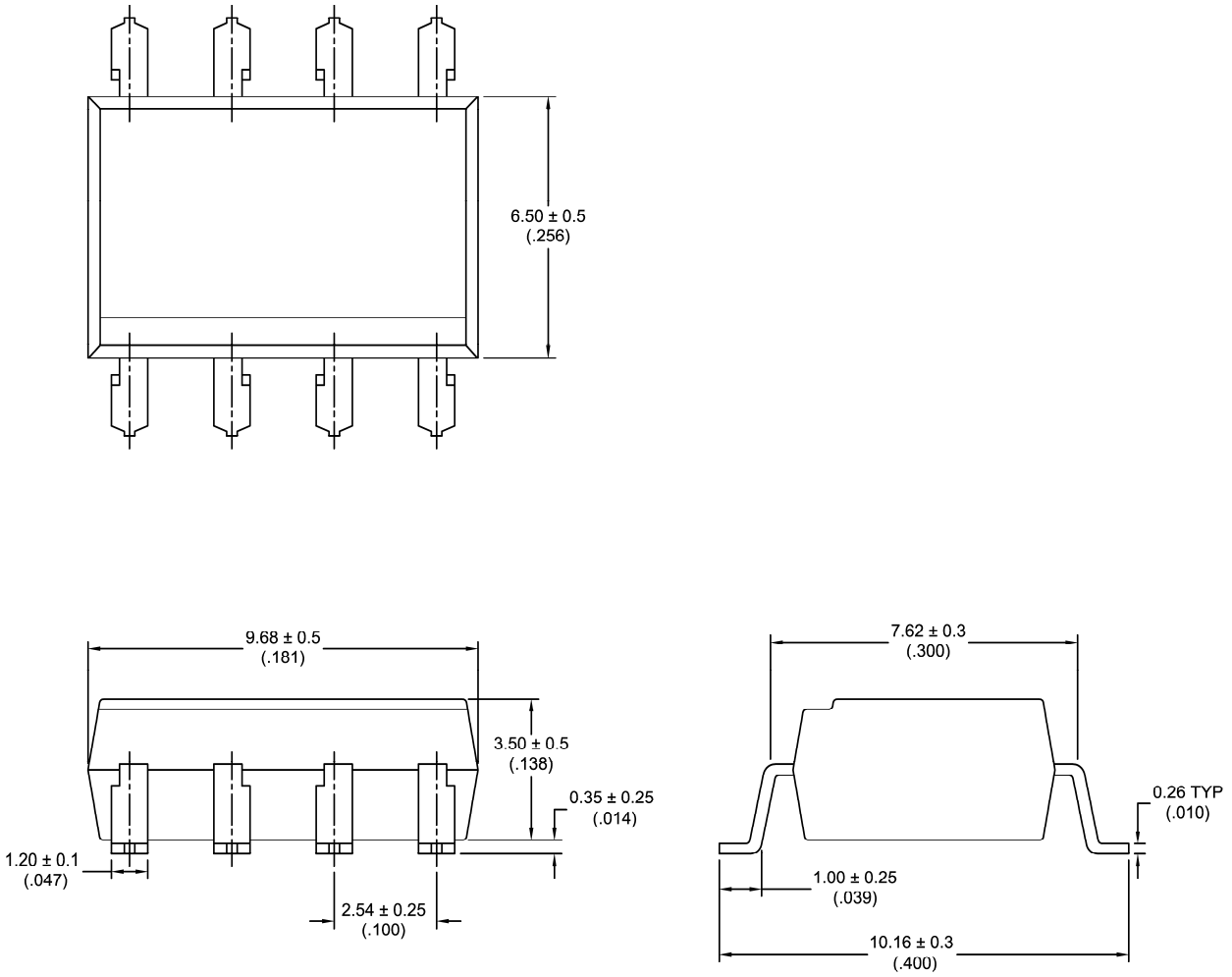
Note: *All dimensions in millimeters [mm] with inches in parenthesis ()*



SDN137 Package Dimensions

8 PIN SMD Surface Mount Package (-S)

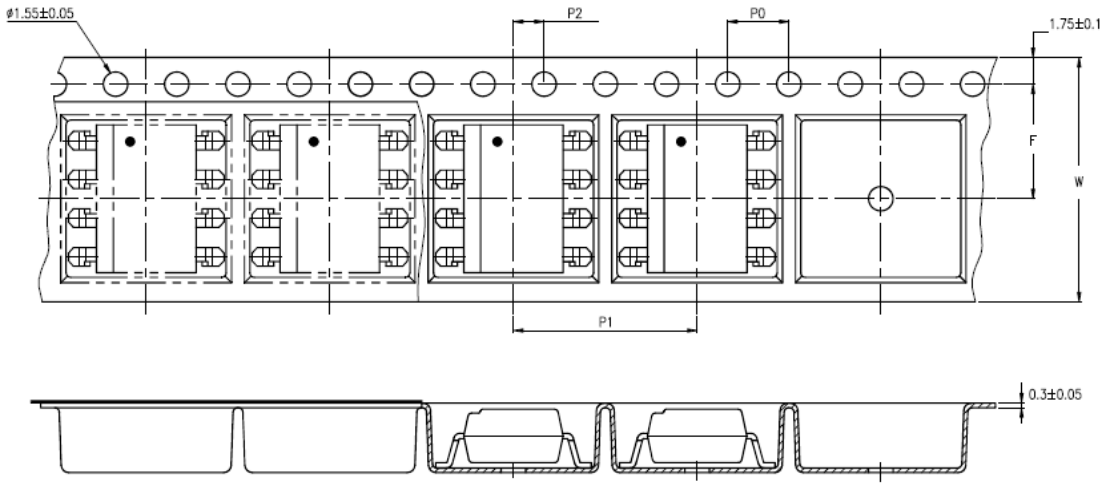
Note: *All dimensions in millimeters [mm] with inches in parenthesis ()*



SDN137 Packaging Specifications

Tape & Reel Specifications (T&R)

Note: *All dimensions in millimeters [mm] with inches in parenthesis ()*



Specification	Symbol	Dimensions, mm (inches)
Tape Width	W	16 ± 0.3 (0.63)
Sprocket Hole Pitch	P0	4 ± 0.1 (0.15)
Compartment Location	F P2	7.5 ± 0.1 (0.295) 2 ± 0.1 (0.079)
Compartment Pitch	P1	12 ± 0.1 (0.472)

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