

MN102L25G , MN102LF25Z , MN102L25Z , MN102L25D , MN102L25A , MN102L2503 , MN102L62G

Type		MN102L25G , MN102LF25Z , MN102L25Z , MN102L25D , MN102L25A , MN102L2503 , MN102L62G				
ROM (×8-Bit / ×16-Bit)		128 K / 128 K (Flash) / 128 K / 64 K / 32 K / External / 128 K				
RAM (×8-Bit / ×16-Bit)		5 K / 3 K / 3 K / 3 K / 3 K / 3 K / 5 K				
Minimum Instruction Execution Time		All models : 100 ns (at 4.5 V to 5.5 V, 20 MHz) All models except MN102LF25Z and MN102L62G: 200 ns (at 2.7 V to 3.6 V, 10 MHz) MN102L62G : 148 ns (at 3.0 V to 3.6 V, 13.5MHz)				
Interrupts		<ul style="list-style-type: none"> • RESET • Watchdog • Timer Counter 0 to 5 • Timer Counter 6 to 7 • Timer Counter 6 to 7 Compare Capture A • Timer Counter 6 to 7 Compare Capture B • ATC Transfer finish • External 0 to 4 • Serial ch 0, 1 Transmission • Serial ch 0, 1 Reception • NMI Pin • A/D Conversion finish 				
Timer Counter		<p>Timer Counter 0 : 8-Bit × 1 (Timer Output, Event Count) Clock Source : 1/1, 1/128 of System Clock, 1/4 of Low Speed Clock, External Clock Interrupt Source : Underflow of Timer Counter 0</p> <p>Timer Counter 1 : 8-Bit × 1 (Timer Output, Event Count, A/D Conversion Start up) Clock Source : System Clock, 1/4 of Low Speed Clock, External Clock, Timer Counter 0 Output Interrupt Source : Underflow of Timer Counter 1</p> <p>Timer Counter 2 to 3 : 8-Bit × 1 (Timer Output, Event Count, UART Baud Rate Generator) Clock Source : System Clock, External Clock, Timer Counter 0 Output, Timer Counter 1, 2 Output Interrupt Source : Underflow of Timer Counter 2, 3</p> <p>Timer Counter 4, 5 : 8-Bit × 1 (Timer Output, Event Count) Clock Source : 1/4 of Low Speed Clock, External Clock, Timer Counter 0 Output, Timer Counter 3, 4 Output Interrupt Source : Underflow of Timer Counter 4, 5</p> <p>Timer Counter 6, 7 : 16-Bit × 1 (Timer Output, Event Count, Input Capture, Output Compare, PWM Output, 2-Phase Encoder Input) Clock Source : System Clock, External Clock, Timer Counter 4, 5 Output Interrupt Source : Coincidence with Compare Capture A or at Capture, Coincidence with Compare Capture B or at Capture, Underflow of Timer Counter 6, 7</p> <p style="text-align: center;"> Connectable Timer Counter 0 to 5 </p>				
Serial Interface		<p>Serial 0 : 7, 8-Bit × 1 (Common use with UART, Transfer direction of MSB/LSB selectable) Clock Source : 1/16 of Timer Counter 2, 1/16 of Timer Counter 3, External Clock, 1/2 of Timer Counter 2</p> <p>Serial 1 : 7, 8-Bit × 1 (Common use with UART, Transfer direction of MSB/LSB selectable) Clock Source : 1/16 of Timer Counter 2, 1/16 of Timer Counter 3, External Clock, 1/2 of Timer Counter 3</p> <p>UART × 2 (Common use with Serial 0, 1)</p> <p>I²C × 2 (Single master)</p>				
I/O Pins	I/O	<table border="0"> <tr> <td style="border: 1px solid black; padding: 2px;">80</td> <td style="padding: 2px;">• Common use 16 (by 8-Bit), 8 (by 4-Bit), 56 (by-bit) (all models except MN102L2503)</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">48</td> <td style="padding: 2px;">• Common use 8 (by 4-Bit), 40 (by-bit) (MN102L2503)</td> </tr> </table>	80	• Common use 16 (by 8-Bit), 8 (by 4-Bit), 56 (by-bit) (all models except MN102L2503)	48	• Common use 8 (by 4-Bit), 40 (by-bit) (MN102L2503)
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48	• Common use 8 (by 4-Bit), 40 (by-bit) (MN102L2503)					
A/D Inputs		8-Bit × 8ch (with S/H)				
PWM		16-Bit × 2ch				

MN102L25G , MN102LF25Z , MN102L25Z , MN102L25D □
 MN102L25A , MN102L2503, MN102L62G

Notes Burst ROM interface support, ATC (between serial 0ch and internal RAM) support

Package LQFP100-P-1414

Electrical Characteristics

A/D Characteristics (at VDD = 5 V)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
A/D Conversion Relative Error		VDD = 5 V, VSS = 0 V			±3	LSB
					+4	
A/D Conversion Time			4	8		µs
Analog Input Voltage	VIA		VSS		VDD	V

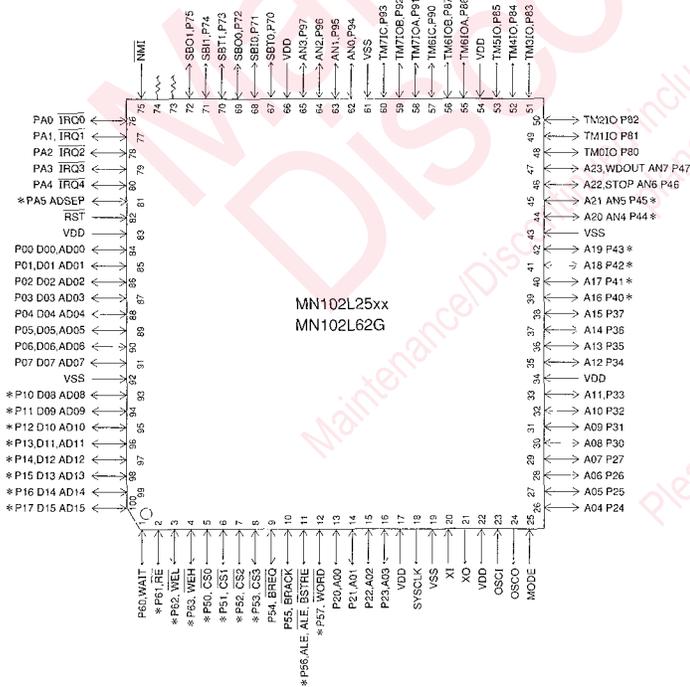
(Ta = 25 °C, VDD = 5.0 V, VSS = 0 V)

A/D Characteristics (at VDD=3V)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
A/D Conversion Relative Error		VDD = 3 V, VSS = 0 V			±3	LSB
					+4	
A/D Conversion Time			9	6		µs
Analog Input Voltage	VIA		VSS		VDD	V

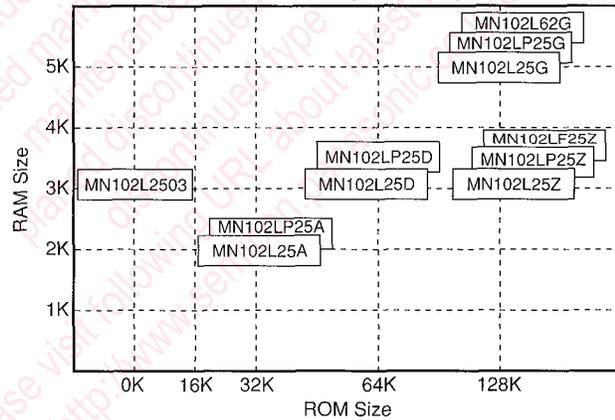
(Ta = 25 °C, VDD = 3.0 V, VSS = 0 V)

Pin Assignment



LQFP100-P-1414

MN102L25xx (100-pin version) series



* Use of these ports are disabled for MN102L2503

* The MN102LF25Z is manufactured and sold under license agreement with BULL CP8 Inc. Note that MN102LF25Z cannot be used as the IC card

See the next page for support tool.

Support Tool

In-Circuit Emulator	PX-ICE102L00 + PX-PRB102L25	
EPROM built-in Type	Type	MN102LP25G , MN102LP25Z , MN102LP25A [ES (Engineering Sample) available]
	ROM (× 8-Bit / × 16-Bit)	128 K / 128 K / 32 K
	RAM (× 8-Bit / × 16-Bit)	5 K / 3 K / 3 K
	Minimum Instruction Execution Time	100 μs (at 4.5 V to 5.5 V, 20 MHz) 200 μs (at 2.7 V to 3.6 V, 10 MHz)
	Package	LQFP100-P-1414

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maintenance type
planned discontinued type
discontinued type
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