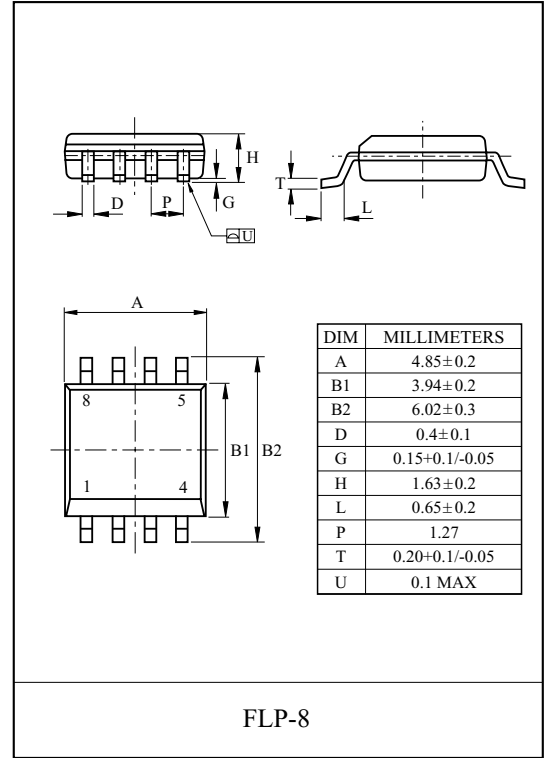


### General Description

Switching regulator and DC-DC Converter applications.  
It s mainly suitable for Back-light Inverter.

### FEATURES

- N-Channel
  - :  $V_{DSS}=30V$ ,  $I_D=7A$ .
  - :  $R_{DS(ON)}=23.5m$  (Max.) @  $V_{GS}=10V$
  - :  $R_{DS(ON)}=39m$  (Max.) @  $V_{GS}=4.5V$
- P-Channel
  - :  $V_{DSS}=-30V$ ,  $I_D=-5A$ .
  - :  $R_{DS(ON)}=45.5m$  (Max.) @  $V_{GS}=-10V$
  - :  $R_{DS(ON)}=80m$  (Max.) @  $V_{GS}=-4.5V$
- Super High Dense Cell Design.
- Reliable and rugged.

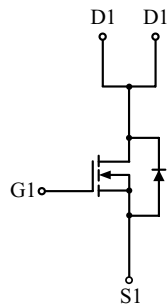
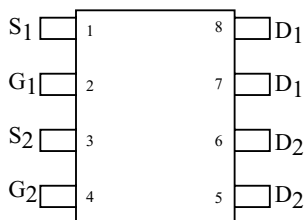


### MAXIMUM RATING (Ta=25 °C)

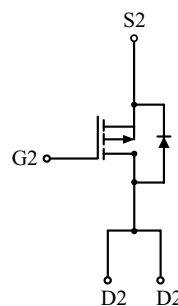
CHARACTERISTIC		SYMBOL	N-Ch	P-Ch	UNIT
Drain-Source Voltage		$V_{DSS}$	30	-30	V
Gate-Source Voltage		$V_{GSS}$	± 20	± 20	V
Drain Current	DC	$I_D^*$	7	-5	A
	Pulsed (note1)	$I_{DP}$	29	-20	
Source-Drain Diode Current		$I_S$	1.7	-1.7	A
Drain Power Dissipation		$P_D^*$	2		W
Maximum Junction Temperature		$T_j$	150		
Storage Temperature Range		$T_{stg}$	-55 150		
Thermal Resistance, Junction to Ambient		$R_{thJA}^*$	62.5		/W

Note : \*Surface Mounted on FR4 Board

### PIN CONNECTION (TOP VIEW)



N-Channel MOSFET



P-Channel MOSFET

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## ELECTRICAL CHARACTERISTICS (Ta=25 °C)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250 μA, V <sub>GS</sub> =0V,	N-Ch	30	-	-	V
		I <sub>D</sub> =-250 μA, V <sub>GS</sub> =0V,	P-Ch	-30	-	-	
Drain Cut-off Current	I <sub>DSS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =24V	N-Ch	-	-	1	μA
		V <sub>GS</sub> =0V, V <sub>DS</sub> =-24V	P-Ch	-	-	-1	
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20V, V <sub>DS</sub> =0V	N-Ch	-	-	± 100	nA
			P-Ch	-	-	± 100	
Gate Threshold Voltage	V <sub>th</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	N-Ch	1.0	-	3	V
		V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250 μA	P-Ch	-1.0	-	-3	
Drain-Source ON Resistance	R <sub>DS(ON)</sub> *	V <sub>GS</sub> =10V, I <sub>D</sub> =7A	N-Ch	-	18	23.5	m
		V <sub>GS</sub> =-10V, I <sub>D</sub> =-5A	P-Ch	-	35	45.5	
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =6A	N-Ch	-	30	39	
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A	P-Ch	-	62	80	
ON State Drain Current	I <sub>D(ON)</sub> *	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =5V	N-Ch	20	-	-	A
		V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V	P-Ch	-20	-	-	
Forward Transconductance	g <sub>fs</sub> *	V <sub>DS</sub> =5V, I <sub>D</sub> =6.6A	N-Ch	-	10	-	S
		V <sub>DS</sub> =-5V, I <sub>D</sub> =-5A	P-Ch	-	9	-	
Source-Drain Diode Forward Voltage	V <sub>SD</sub> *	I <sub>S</sub> =1.7A, V <sub>GS</sub> =0V	N-Ch	-	0.7	1.2	V
		I <sub>S</sub> =-1.7A, V <sub>GS</sub> =0V	P-Ch	-	-0.8	-1.2	

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## ELECTRICAL CHARACTERISTICS (Ta=25 °C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
<b>Dynamic</b>								
Total Gate Charge	Q <sub>g</sub>	<b>N-Ch</b> : V <sub>DS</sub> =15V, I <sub>D</sub> =6.6A, V <sub>GS</sub> =10V (Fig.1)	N-Ch	-	16.4	20.5	nC	
			P-Ch	-	13	16		
		<b>P-Ch</b> : V <sub>DS</sub> =-15V, I <sub>D</sub> =-5A, V <sub>GS</sub> =-10V (Fig.3)	N-Ch	-	7.2	9		
			P-Ch	-	6.25	7.8		
Gate-Source Charge	Q <sub>gs</sub>	<b>N-Ch</b> : V <sub>DS</sub> =15V, I <sub>D</sub> =6.6A, V <sub>GS</sub> =10V (Fig.1)	N-Ch	-	4	-		
Gate-Drain Charge	Q <sub>gd</sub>		<b>P-Ch</b> : V <sub>DS</sub> =-15V, I <sub>D</sub> =-5A, V <sub>GS</sub> =-10V (Fig.3)	P-Ch	-	2.6		-
		N-Ch		-	2.6	-		
P-Ch	-	2.9	-					
Turn-on Delay time	t <sub>d(on)</sub>	<b>N-Ch</b> : V <sub>DD</sub> =15V, I <sub>D</sub> =6.6A, V <sub>GS</sub> =10V, R <sub>G</sub> =3 (Fig.2)	N-Ch	-	7.4	-	ns	
Turn-on Rise time	t <sub>r</sub>		P-Ch	-	4.7	-		
			N-Ch	-	27.7	-		
Turn-off Delay time	t <sub>d(off)</sub>		<b>P-Ch</b> : V <sub>DD</sub> =-15V, V <sub>GS</sub> =-10V, R <sub>G</sub> =3, R <sub>L</sub> =2.7 (Fig.4)	P-Ch	-	7.8		-
				N-Ch	-	12.2		-
Turn-off Fall time	t <sub>f</sub>		P-Ch	-	47.2	-		
			N-Ch	-	7.6	-		
P-Ch	-		22.6	-				
Input Capacitance	C <sub>iss</sub>	<b>N-Ch</b> : V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1.0MHz	N-Ch	-	742	-	pF	
Output Capacitance	C <sub>oss</sub>		P-Ch	-	820	-		
			N-Ch	-	126	-		
Reverse transfer Capacitance	C <sub>rss</sub>		<b>P-Ch</b> : V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1.0MHz	P-Ch	-	137		-
				N-Ch	-	76		-
P-Ch	-		89	-				

Note 1>\* Pulse test : Pulse width 300μs, Duty Cycle 2%.

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## N-Channel

Fig1.  $I_D - V_{DS}$

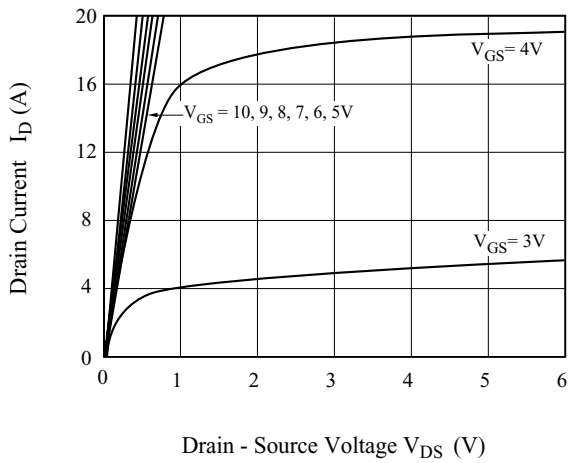


Fig2.  $I_D - V_{GS}$

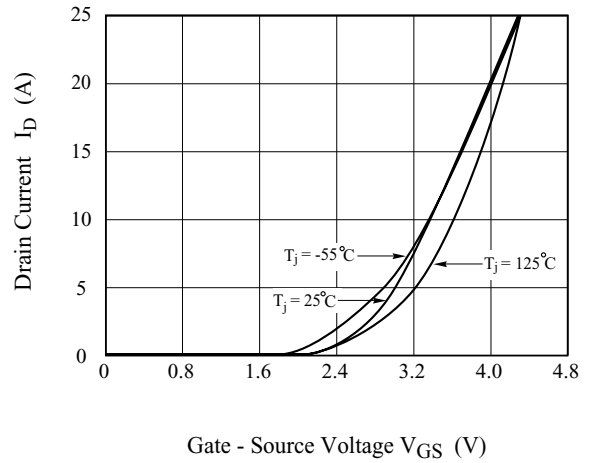


Fig3.  $V_{th} - T_j$

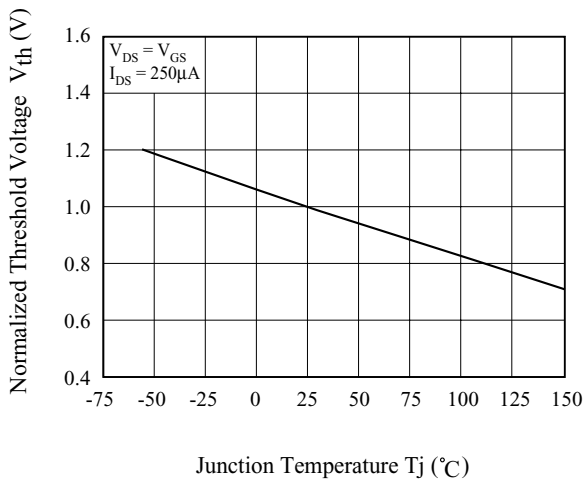


Fig4.  $I_{DR} - V_{SD}$

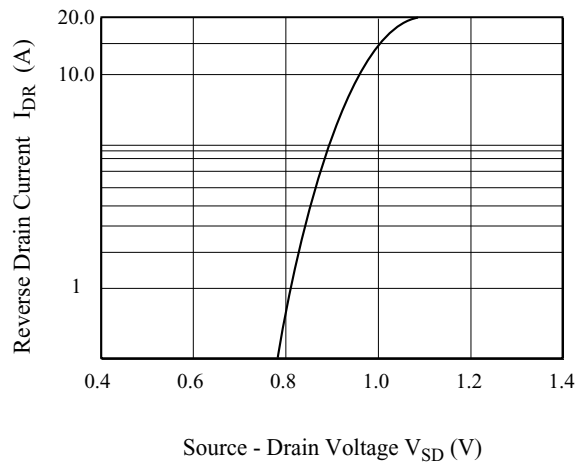


Fig5.  $R_{DS(ON)} - T_j$

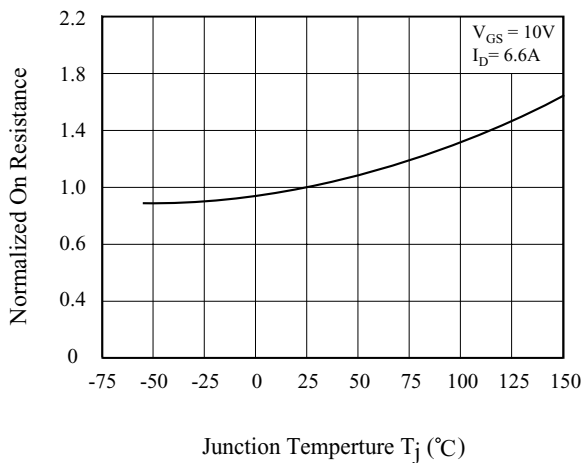
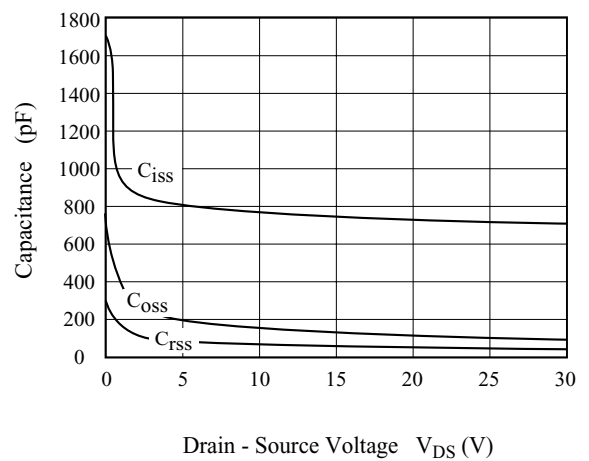


Fig6.  $C - V_{DS}$



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Fig7.  $Q_g - V_{GS}$

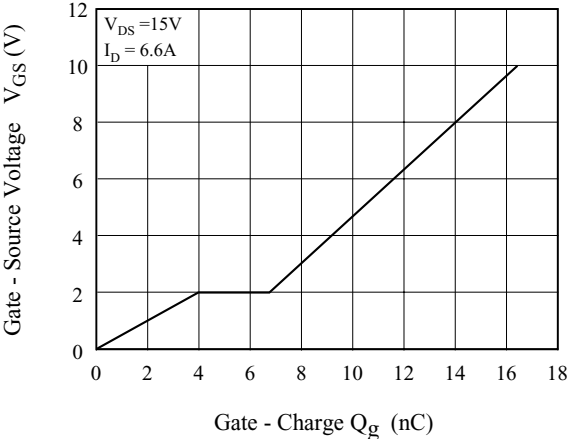


Fig8. Safe Operation Area

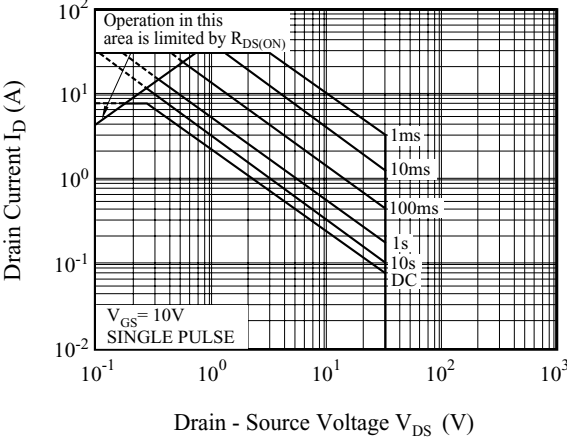
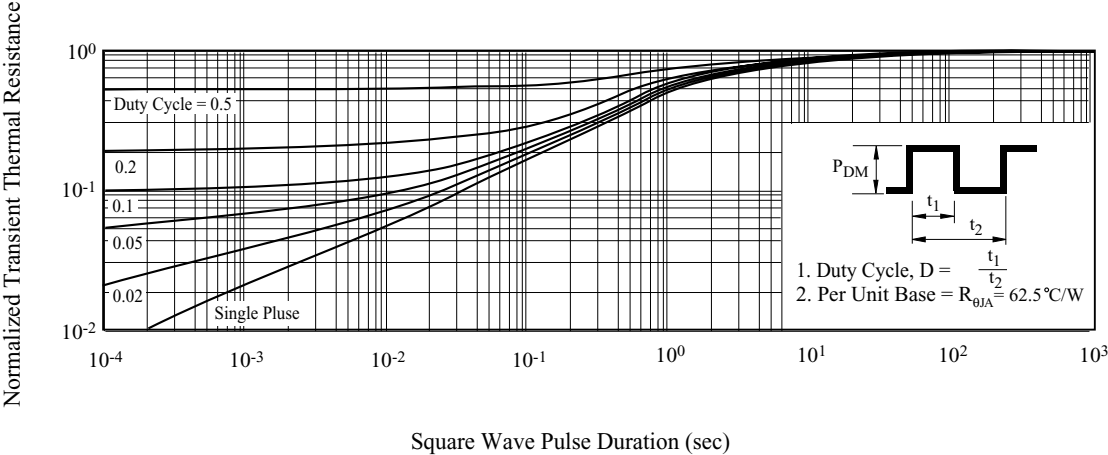


Fig9. Transient Thermal Response Curve



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## P-Channel

Fig1.  $I_D - V_{DS}$

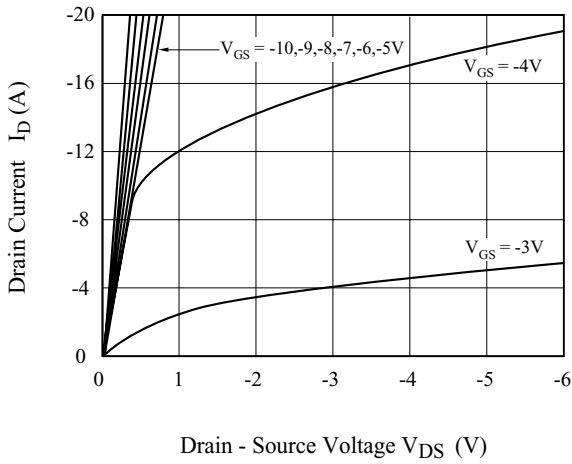


Fig2.  $I_D - V_{GS}$

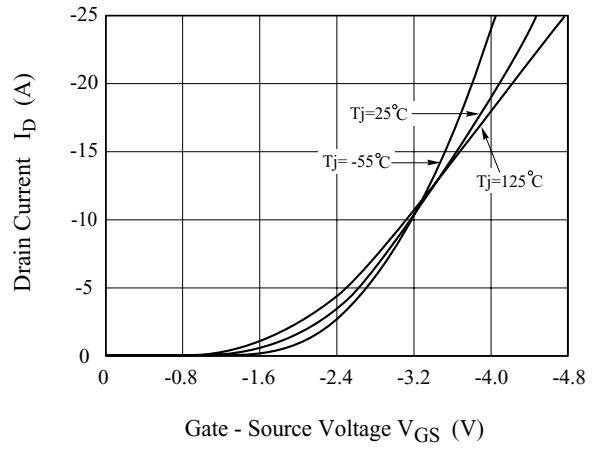


Fig3.  $V_{th} - T_j$

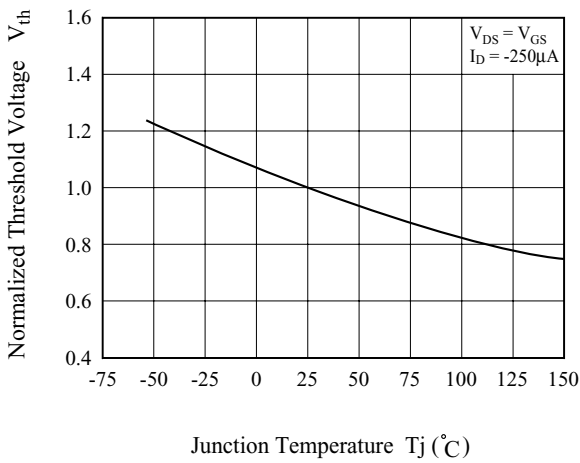


Fig4.  $I_{DR} - V_{SD}$

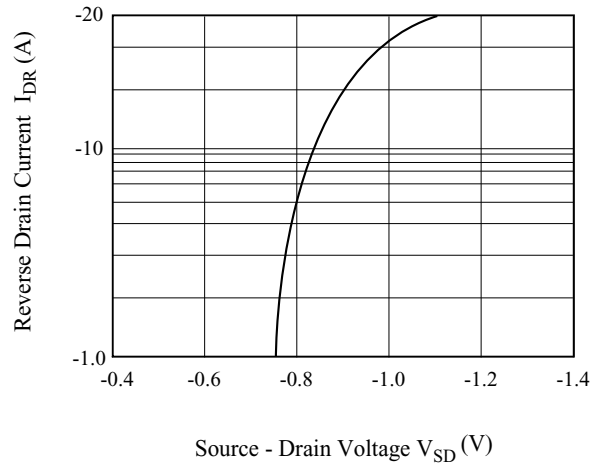


Fig5.  $R_{DS(ON)} - T_j$

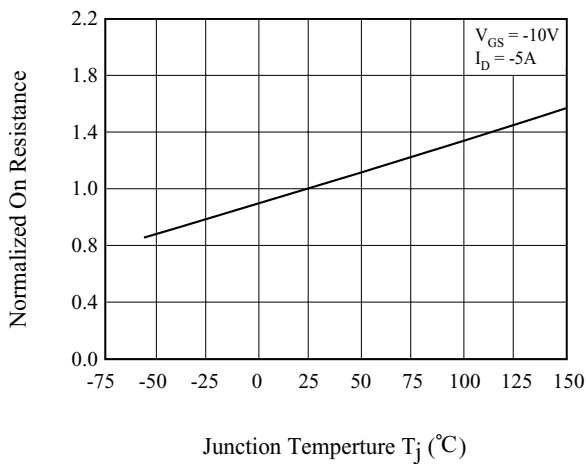
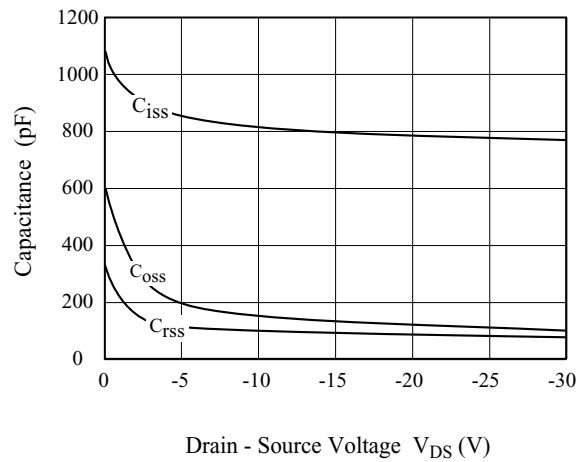


Fig6.  $C - V_{DS}$



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Fig7.  $Q_g - V_{GS}$

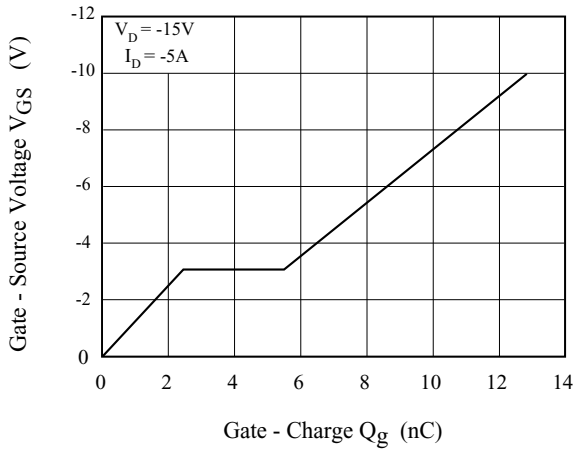


Fig8. Safe Operation Area

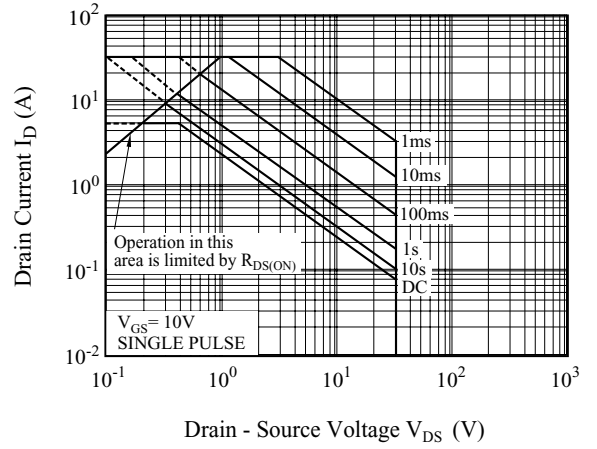
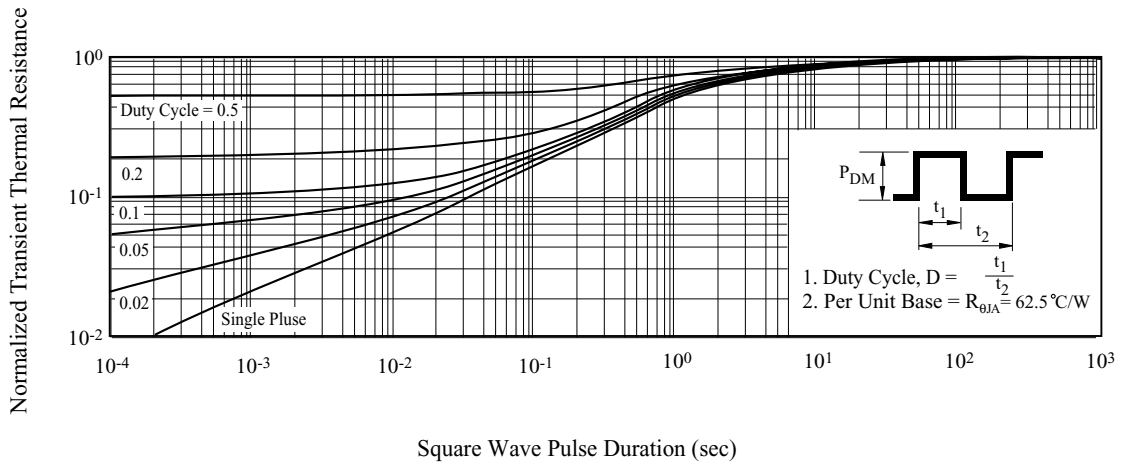


Fig9. Transient Thermal Response Curve



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## N-Channel

Fig. 1 Gate Charge

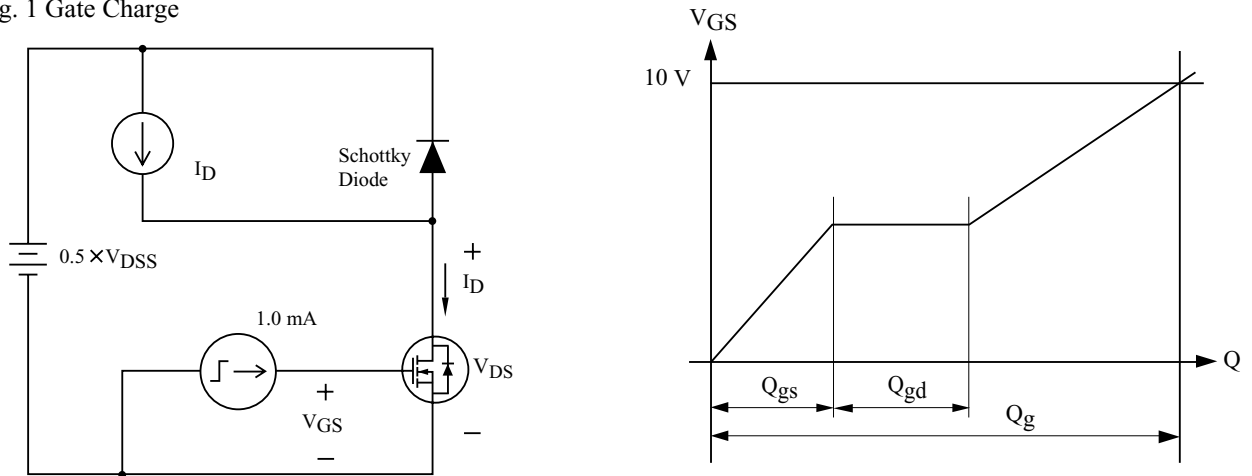
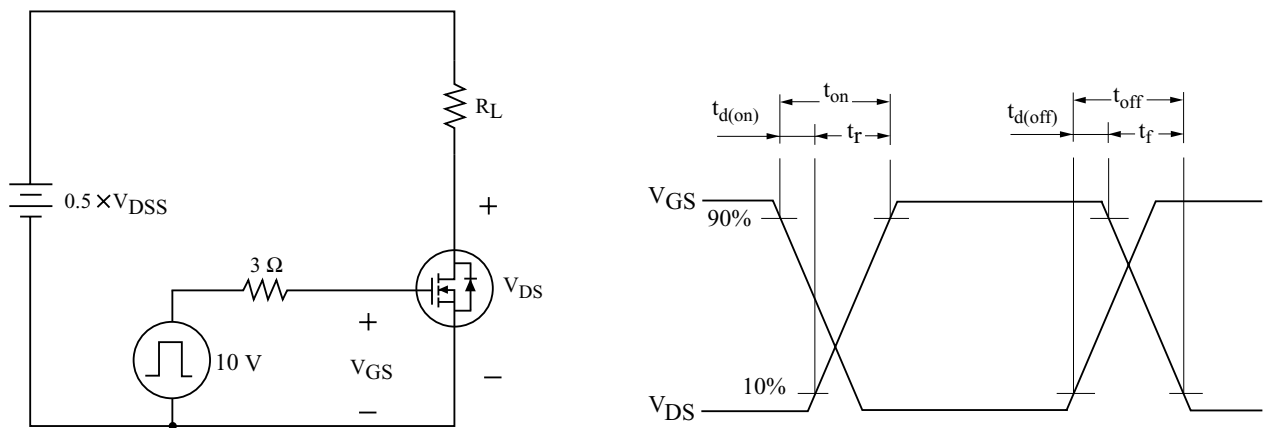


Fig. 2 Resistive Load Switching





## P-Channel

Fig. 1 Gate Charge

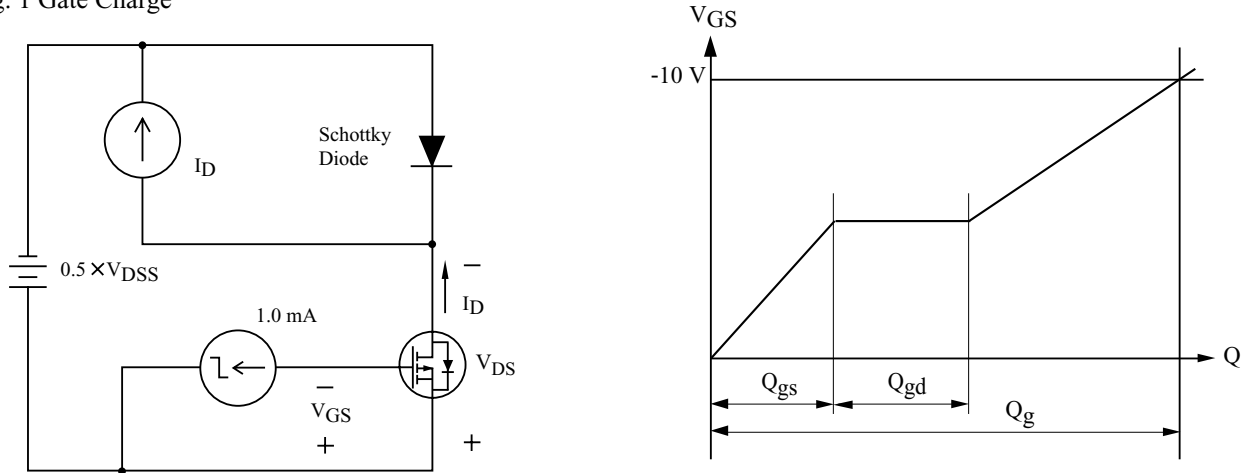


Fig. 2 Resistive Load Switching

