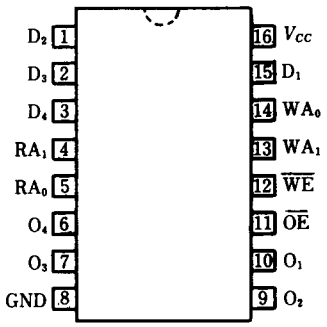
HD74AC670/HD74ACT670 • 4×4 Register File with with 3-State Output

Description

The HD74AC670/HD74ACT670 contains 16 high speed, low power, transparent D-type latches arranged as four words of four bits each, to function as a 4 x 4 register file. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

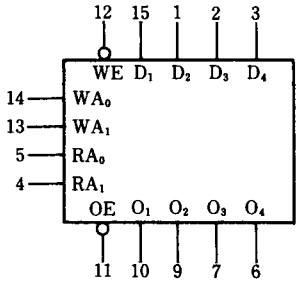
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA
- HD74ACT670 have TTL-Compatible Inputs

Pin Assignment



(Top View)

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Pin Names

D_1-D_4	Data Inputs
WA_0, WA_1	Write Address Inputs
$\overline{WE}$	Write Enable Input (Active Low)
RA_0, RA_1	Read Address Inputs
$\overline{OE}$	3-State Output Enable Input (Active Low)
O_1-O_4	Data Outputs

Write Function Table

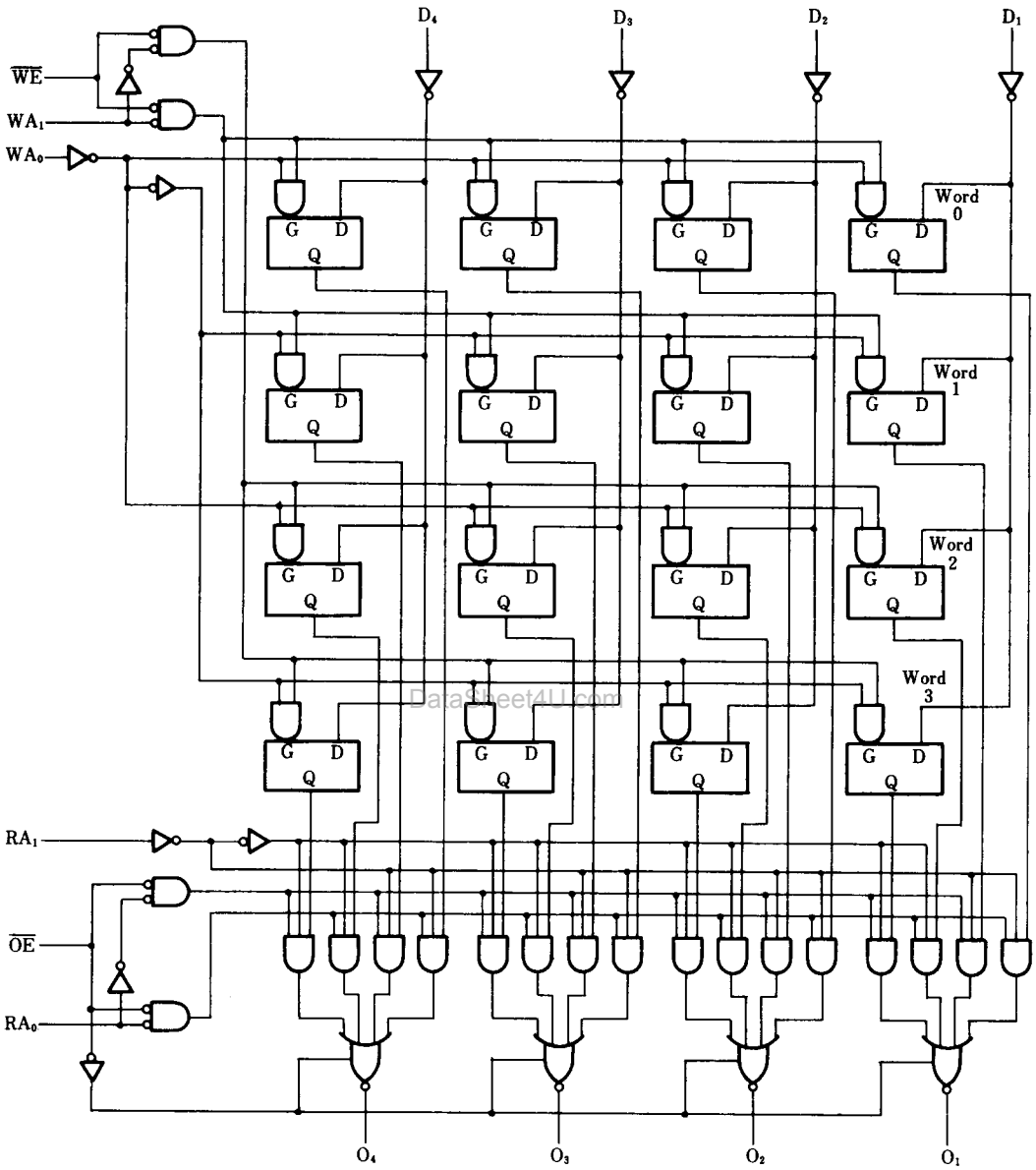
Write Inputs			D Inputs to
$\overline{WE}$	WA_1	WA_0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (hold)

Read Function Table

Read Inputs			Outputs from
$\overline{OE}$	RA_1	RA_0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (HIGH Z)

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

Logic Diagram



DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN}=V_{CC}$ or Ground, $V_{CC}=5.5V$, Ta=Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN}=V_{CC}$ or Ground, $V_{CC}=5.5V$, Ta=25°C
I_{CCT}	Maximum I_{CC}/Input (HD74ACT670)	1.5	mA	$V_{IN}=V_{CC}-2.1V$ $V_{CC}=5.5V$, Ta=Worst Case

AC Characteristics : HD74AC670

Symbol	Parameter	V_{CC}* (V)	Ta=+25°C C_L=50pF			Ta=−40°C to +85°C C_L=50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Dalay $\overline{W_E}$ to O_n	3.3	1.0	14.0	17.5	1.0	19.0	ns
		5.0	1.0	11.5	13.5	1.0	15.0	
t_{PHL}	Propagation Dalay $\overline{W_E}$ to O_n	3.3	1.0	13.5	17.0	1.0	18.5	ns
		5.0	1.0	11.0	13.0	1.0	14.5	
t_{PLH}	Propagation Dalay R_{A1} or R_{A0} to O_n	3.3	1.0	12.5	15.5	1.0	17.0	ns
		5.0	1.0	10.0	12.0	1.0	13.0	
t_{PHL}	Propagation Dalay R_{A1} or R_{A0} to O_n	3.3	1.0	12.5	15.5	1.0	17.0	ns
		5.0	1.0	10.0	12.0	1.0	13.0	
t_{PLH}	Propagation Delay Data to O_n	3.3	1.0	12.0	15.0	1.0	16.5	ns
		5.0	1.0	9.5	11.5	1.0	12.5	
t_{PHL}	Propagation Delay Data to O_n	3.3	1.0	11.5	14.5	1.0	16.0	ns
		5.0	1.0	9.0	11.0	1.0	12.0	
t_{PZH}	Enable Time $\overline{OE}$ to O_n	3.3	1.0	8.0	11.0	1.0	12.0	ns
		5.0	1.0	6.0	8.5	1.0	9.5	
t_{PZL}	Enable Time $\overline{OE}$ to O_n	3.3	1.0	10.0	12.0	1.0	13.0	ns
		5.0	1.0	7.5	9.5	1.0	10.5	
t_{PHZ}	Disable Time $\overline{OE}$ to O_n	3.3	1.0	8.0	11.0	1.0	12.0	ns
		5.0	1.0	6.0	8.5	1.0	9.5	
t_{PLZ}	Disable Time $\overline{OE}$ to O_n	3.3	1.0	9.0	11.5	1.0	12.5	ns
		5.0	1.0	7.0	9.0	1.0	10.0	

* Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements : HD74AC670

Symbol	Parameter	V_{CC}* (V)	Ta=+25°C C_L=50pF	Ta=−40°C to +85°C C_L=50pF		Unit
			Typ	Guaranteed Minimum		
t_{su}	Setup Time Data to $\overline{W_E}$	3.3	3.0	5.5	6.0	ns
		5.0	2.0	4.0	4.5	
	Setup Time W_{A1} or W_{A0} to $\overline{W_E}$	3.3	3.0	5.5	6.0	ns
		5.0	2.0	4.5	4.5	
t_h	Hold Time $\overline{W_E}$ to Data	3.3	3.0	4.0	4.0	ns
		5.0	2.5	4.0	4.0	
	Hold Time $\overline{W_E}$ to W_{A1} or W_{A2}	3.3	3.0	4.0	4.0	ns
		5.0	2.5	4.0	4.0	
t_w	Pulse Width $\overline{W_E}$	3.3	3.5	5.5	7.0	ns
		5.0	2.5	4.5	5.0	
t_{latch}	Latch Width $\overline{W_E}$ to 1	3.3	0.5	10.0	10.0	ns
		5.0	0.5	10.0	10.0	

* Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Characteristics : HD74ACT670 Preliminary

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C C_L = 50pF			Ta = −40°C to +85°C C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Dalay $\overline{W_E}$ to O	5.0	1.0	13.0	15.5	1.0	16.5	ns
t_{PHL}	Propagation Dalay $\overline{W_E}$ to O	5.0	1.0	13.0	15.5	1.0	16.5	ns
t_{PLH}	Propagation Dalay R_{A1} or R_{A0} to O	5.0	1.0	13.0	15.5	1.0	16.5	ns
t_{PHL}	Propagation Dalay R_{A1} or R_{A0} to O	5.0	1.0	11.0	13.5	1.0	14.5	ns
t_{PLH}	Propagation Delay Data to O	5.0	1.0	10.5	12.5	1.0	13.5	ns
t_{PHL}	Propagation Delay Data to O	5.0	1.0	11.0	13.0	1.0	14.0	ns
t_{PZH}	Enable Time $\overline{OE}$ to O	5.0	1.0	8.0	10.5	1.0	11.5	ns
t_{PZL}	Enable Time $\overline{OE}$ to O	5.0	1.0	9.5	11.5	1.0	12.5	ns
t_{PHZ}	Disable Time $\overline{OE}$ to O	5.0	1.0	7.0	9.5	1.0	10.5	ns
t_{PLZ}	Disable Time $\overline{OE}$ to O	5.0	1.0	7.5	10.0	1.0	11.0	ns

* Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements : HD74ACT670 Preliminary

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C C_L = 50pF	Ta = −40°C to +85°C C_L = 50pF	Unit
			Typ	Guaranteed Minimum	
t_{su}	Setup Time Data to $\overline{W_E}$	5.0	2.5	7.0	8.0	ns
	Setup Time W_{A1} or W_{A0} to $\overline{W_E}$	5.0	2.5	7.0	8.0	ns
t_h	Hold Time $\overline{W_E}$ to Data	5.0	2.5	4.0	4.0	ns
	Hold Time $\overline{W_E}$ to W_{A1} or W_{A2}	5.0	2.5	4.0	4.0	ns
t_w	Pulse Width $\overline{W_E}$	5.0	4.5	7.0	8.0	ns
t_{latch}	Latch Time $\overline{W_E}$ to R_B	5.0	0.5	10.0	10.0	ns

* Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capacitance	60	pF	V_{CC} = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

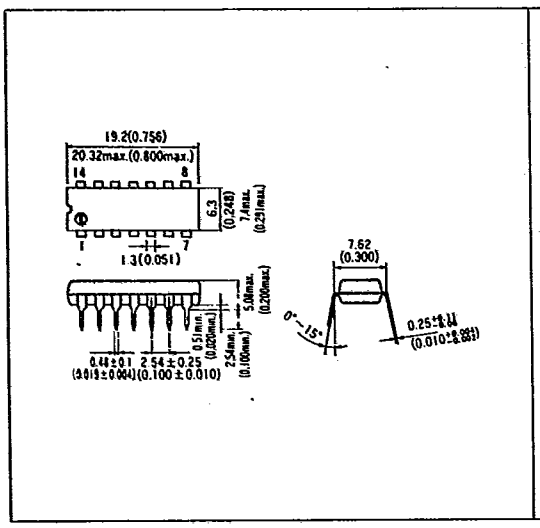
• Package code of Advanced CMOS Logic

HD74AC XXXX P

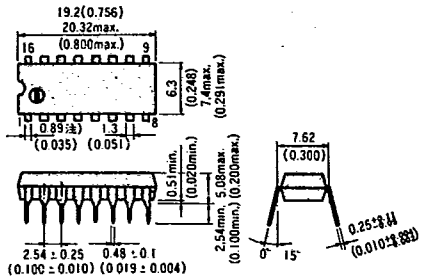
- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
  - 74AC: Commercial FACT
  - 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

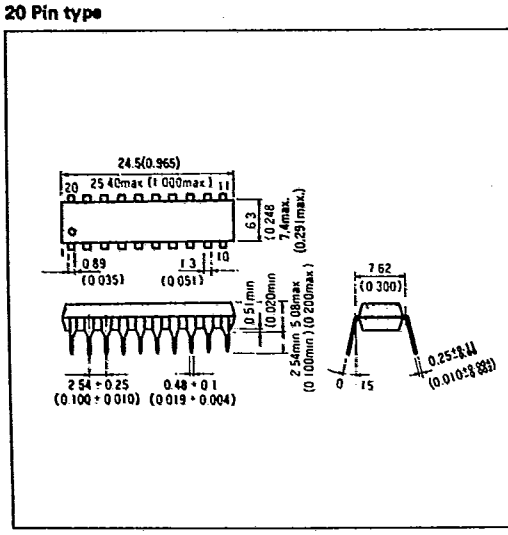
14 Pin type



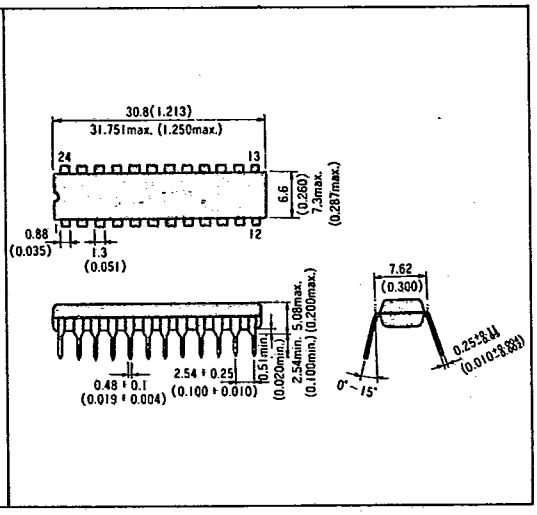
16 Pin type



20 Pin type



24 Pin type



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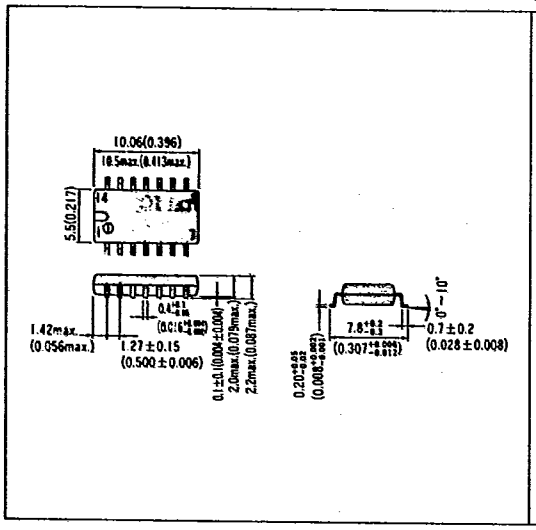
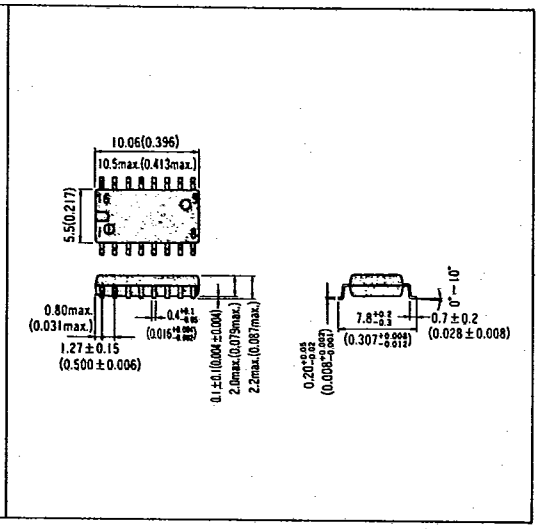
Package Information

Small Outline Package [Unit: mm (inch)]

14 Pin type



16 Pin type



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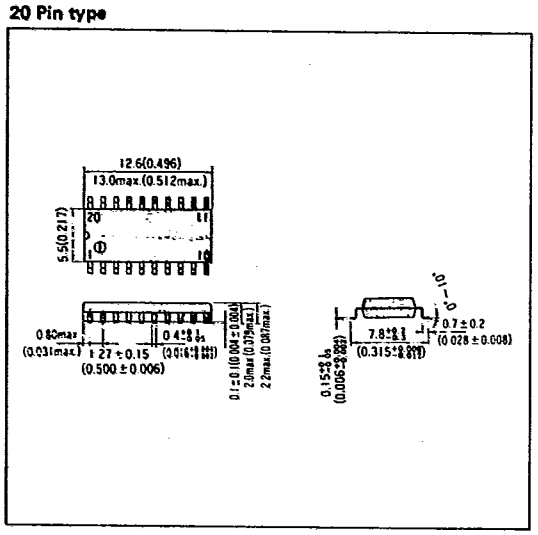

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