

**LVDS UHF VCXO
SD-X3DBXXX-X Series**

Rev. J

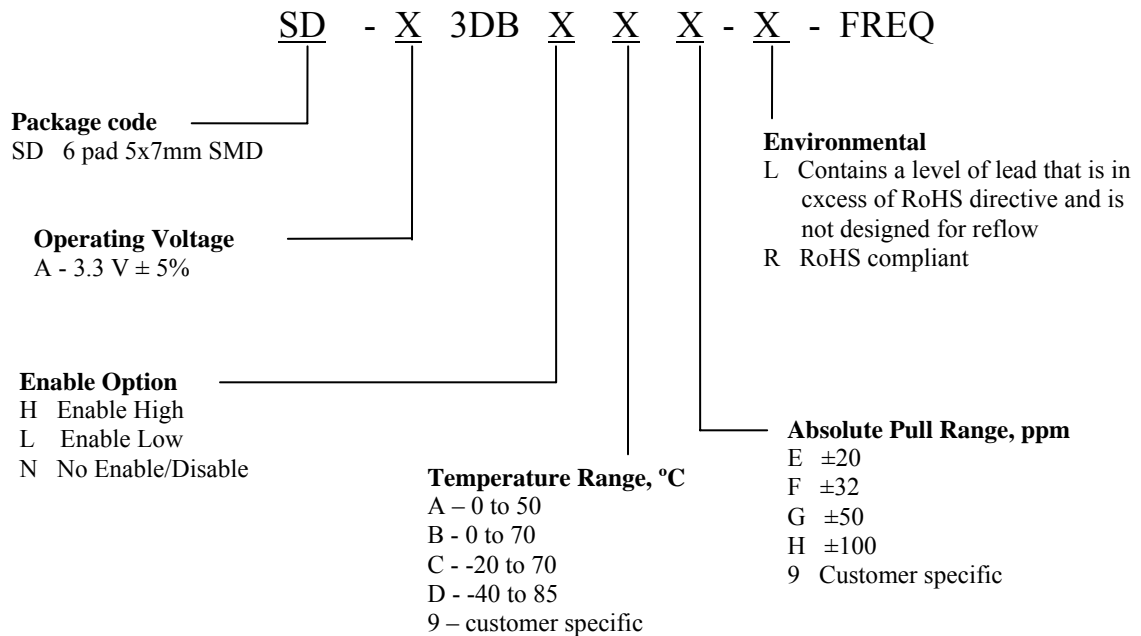
Description

The **SD-X3DBXXX Series** of voltage controlled crystal oscillators (VCXO) provides ultra high frequency with LVDS complementary output. The outputs can be Tri-stated for test automation or combining multiple clocks. The device is based on low noise analog harmonic multiplication for higher frequencies, and packaged in a miniature, low profile leadless ceramic SMD package with 6 gold plated pads.

Applications and Features

- Wide frequency range – 60.0MHz to 312.500MHz
- Fiber Channel; 10 GbE; Infiniband; Network Processors; SOHO Routing
- High Reliability – NEL HALT/HASS qualified for crystal oscillator start-up conditions
- Low Phase Noise and Jitter
- High Shock Resistance, to 1000g
- Ultra High Frequency
- Absolute Pull Range (APR) to ± 100 ppm
- Grounded lid and internal by-pass capacitor reduce EMI
- COTS/Dual use

Creating a Part Number



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Operating Temperature Range	To	-40 to +85	°C
Storage Temperature Range	Tst	-50 to +90	°C
Supply Voltage	Vcc	-0.5 to 4.5	V
Enable/Disable Voltage	Ven/dis	0 to Vcc	V

Electrical Parameters (2)

Parameter	Symb	Conditions, Note	MIN	TYP	MAX	Unit
Nominal Frequency	Fo		60		312.500	MHz
Supply Voltage	Vcc	Code A	3.135	3.3	3.465	V
Supply current	Icc			60	70	mA
Output Logic Type				LVDS		
Load		At receiving end between the outputs	90	100	110	Ohm
Output Levels	Vod	Differential amplitude	247	330	454	mV
		Amplitude error			50	mV
	Vof	Offset Voltage	1.125	1.25	1.375	V
		Offset Voltage error			50	mV
Duty Cycle (Symmetry)		At outputs crossing, room temperature	45/55	50/50	55/45	%
Rise/Fall Time	Tr/Tf	20 to 80, 80 to 20 %		0.5	0.7	ns
Jitter	Integrated	J	Integrated from Phase Noise, 12 KHz to 20 MHz, RMS		0.3	ps
		Wavecrest characterized	Random period,		2.5	ps
		Accumul., pk-to-pk		35	ps	
		Deterministic		6	ps	
Sub-Harmonics				-50		dBc
Phase Noise ⁽¹⁾	£ (Δf)	212.5 MHz	@ 10 Hz @ 100 Hz @ 1 KHz @ 10KHz @ 100KHz @ >1MHz	-65 -95 -122 -138 -142 -148		dBc/Hz
Frequency Stability	ΔF/F	Overall, including temperature, aging 10 years, shock and vibration @ Vc=Vcc/2; If -40 to 85°C is selected		30 50		ppm
Control Voltage Range	Vc		0V		Vcc	V
Setability	Vcs	Vc to set F at Fo; T, Vcc, load - nominal, as shipped	0.4 Vcc	0.5 Vcc	0.6 Vcc	V
Absolute Pull Range	APR	Over all conditions, see part # creation	20,32, 50,100			ppm
Input Impedance	Zin	@ Fmod < 100 KHz	10			KOhm
Modulation Bandwidth		At Vc = Vcc/2, -3dB	10			KHz
Enable High Option						
Pin 2 Enabled		CMOS logic 1 or N/C	0.7 Vcc		Vcc	V
Pin 2 Disabled		CMOS logic 0	0		0.3 Vcc	V
Enable Low Option						
Pin 2 Disabled		CMOS logic 1 or N/C	0.7 Vcc		Vcc	V
Pin 2 Enabled		CMOS logic 0	0		0.3 Vcc	V

Footnote: 1) If phase noise data at a particular frequency is needed, contact factory.

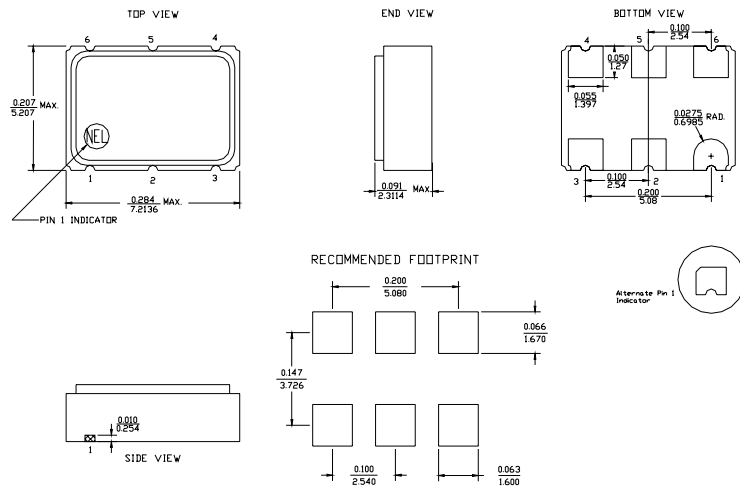
2) All parameters, unless otherwise specified, are at nominal conditions, ie: T=25°C, Nominal Vcc & Nominal Load.

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Electrical Connection

Pin	Connection
1	V _{CO}
2	Enable
3	V _{EE}
4	Output
5	Output Complement
6	V _{CC}



ALL DIMENSIONS: $\frac{IN}{mm}$
All tolerances are ± 0.005 inches (± 0.127 mm) unless otherwise specified.

Environmental and Mechanical Characteristics

Operating temp. range	see part # table
Mechanical Shock	Per MIL-STD-202, Method 213, Cond. A
Thermal Shock	Per MIL-STD-883, Method 1011, Cond. A
Vibration	Per MIL-STD-883, Method 2007, Cond. A
Hermetic Seal	Leak rate less than 1×10^{-8} atm.cc/s of helium
Soldering conditions	See MAX reflow profile below

MAX Reflow Profile

