ROHM SEMICONDUCTOR

Datasheet

Operational Amplifiers

Low Power Ground Sense Operational Amplifiers

LMR821G

●General Description

Ground Sense Low Voltage Op-Amp integrates single Op-Amp on a single chip. Especially, these series are operable with low voltage and low supply current.

●Features

- Low operating supply voltage
- Input Ground Sense, Output Full Swing
- High large signal voltage gain
- High Slew Rate
- Low supply current
- Low input offset voltage

●Applications

- Customer electronics
- Buffer
- Active filter
- Mobile equipment

●Key Specifications

- Low Operating Supply Voltage (single supply): +2.5V to +5.0V
- High voltage gain (RL=600Ω): 105dB (Typ.)
- Wide Temperature Range: -40°C to +85°C
- High Slew Rate: 2.0V/µs (Typ.)
- Low Input Offset Voltage: 3.5mV (Max.)
- Low Input Bias Current: 30nA (Typ.)

●Package

Package	W(Typ.) xD(Typ.) xH(Max.)
SSOP5	2.90mm x 2.80mm x 1.25mm

●Simplified Schematic

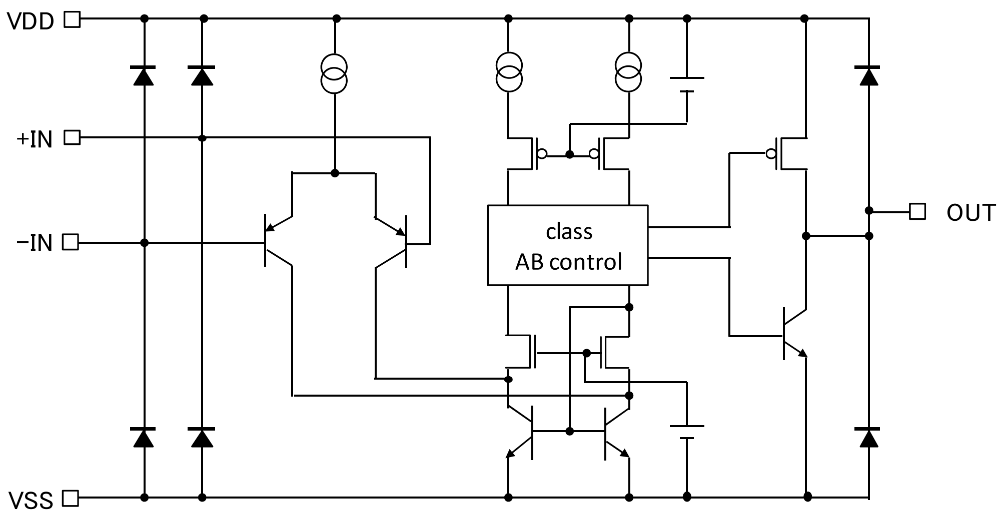
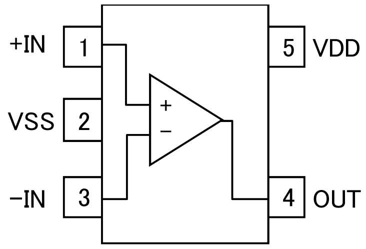


Figure 1. Simplified Schematic (1 channel only)

○Product structure：Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

●Pin Configuration
LMR821G (SSOP5)



Pin No.	Pin Name
1	+IN
2	VSS
3	-IN
4	OUT
5	VDD

Package
SSOP5
LMR821G

●Ordering Information

L M R 8 2 1 G - T R

Part Number
LMR821

Package
G:SSOP5

Packaging and forming specification
TR: Embossed tape and reel
(SSOP5)

●Line-up

Topr	**Package**		**Operable Part Number**
-40°C to +85°C	SSOP5	Reel of 3000	LMR821G-TR

●Absolute Maximum Ratings(Ta=25°C)

Parameter	Symbol		Ratings	Unit
Supply Voltage	VDD-VSS		+7	V
Power dissipation	Pd	SSOP5	675[*1*2]	mW
Differential Input Voltage[*3]	Vid		VDD to VSS	V
Input Common-mode Voltage Range	Vicm		(VSS - 0.3) to (VDD + 0.3)	V
Operable with low voltage	Vopr		+2.5 to +5.0	V
Operating Temperature	Topr		- 40 to +85	°C
Storage Temperature	Tstg		- 55 to +150	°C
Maximum Junction Temperature	Tjmax		+150	°C

Note: Absolute maximum rating item indicates the condition which must not be exceeded.
Application of voltage in excess of absolute maximum rating or use out absolute maximum rated temperature environment may cause deterioration of characteristics.

*1 To use at temperature above Ta＝25°C reduce 5.4mW/°C.

*2 Mounted on a FR4 glass epoxy PCB(70mm×70mm×1.6mm).

*3 The voltage difference between inverting input and non-inverting input is the differential input voltage.
Then input terminal voltage is set to more than VSS.

●**Electrical Characteristics**:

○LMR821G (Unless otherwise specified VDD=+2.7V, VSS=0V)

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage *4*5	Vio	25°C	-	1	3.5	mV	VDD=2.5V to 5.0V
		Full Range	-	-	4		
Input Offset Voltage Drift	ΔVio/ΔT	25°C	-	1	-	μV/°C	-
Input Offset Current*4	Iio	25°C	-	0.5	30	nA	-
Input Bias Current *4	Ib	25°C	-	30	90	nA	-
Supply Current*5	IDD	25°C	-	220	300	μA	Av=0dB, VIN=1.35V
		Full range	-	-	500		
Maximum Output Voltage(High)	VOH	25°C	2.50	2.58	-	V	RL=600Ω to VDD/2
			2.60	2.66	-		RL=2kΩ to VDD/2
Maximum Output Voltage(Low)	VOL	25°C	-	130	200	mV	RL=600Ω to VDD/2
			-	80	120		RL=2kΩ to VDD/2
Large Signal Voltage Gain	Av	25°C	-	100	-	dB	RL=600Ω to VDD/2
			95	100	-		RL=2kΩ to VDD/2
Input Common-mode Voltage Range	Vicm	25°C	VSS	-	VDD-0.9	V	VSS to VDD
Common-mode Rejection Ratio	CMRR	25°C	70	85	-	dB	VCM=0.5V
Power supply reject-ratio	PSRR	25°C	75	85	-	dB	VDD=2.7V to 5.0V VCM=1V
Output Source Current *6	Isource	25°C	12	16	-	mA	OUT=0V, short current
Output Sink Current *6	Isink	25°C	12	26	-	mA	OUT=2.7V, short current
Slew Rate	SR	25°C	-	1.5	-	V/μs	CL=25pF
Gain Bandwidth	GBW	25°C	-	4.5	-	MHz	CL=25pF, Av=40dB f=1MHz
Phase Margin	θ	25°C	-	45	-	Deg	CL=25pF, Av=40dB
Gain Margin	GM	25°C	-	4.5	-	dB	CL=25pF, Av=40dB
Input Referred Noise Voltage	Vn	25°C	-	45	-	$nV/\sqrt{Hz}$	f=1kHz
Total Harmonic Distortion + Noise	THD+N	25°C	-	0.01	-	%	OUT=2.2V_{P-P}, f=1kHz RL=10kΩ Av=0dB, DIN-AUDIO

*4 Absolute value.
*5 Full range: Ta=-40°C to +85°C
*6 Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

○LMR821G (Unless otherwise specified VDD=+2.5V, VSS=0V)

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage *7	Vio	25°C	-	1	3.5	mV	VDD=2.5V to 5.0V
		Full Range	-	-	4		
Maximum Output Voltage(High)	VOH	25°C	2.30	2.37	-	V	RL=600Ω to VDD/2
			2.40	2.46	-		RL=2kΩ to VDD/2
Maximum Output Voltage(Low)	VOL	25°C	-	130	200	mV	RL=600Ω to VDD/2
			-	80	120		RL=2kΩ to VDD/2

*7 Absolute value.

○LMR821G (Unless otherwise specified VDD=+5.0V, VSS=0V)

Parameter	Symbol	Temperature Range	Limits Min.	Limits Typ.	Limits Max.	Unit	Condition
Input Offset Voltage *8*9	Vio	25°C	-	1	3.5	mV	VDD=2.5V to 5.0V
		Full Range	-	-	4		
Input Offset Voltage Drift	ΔVio/ΔT	25°C	-	1	-	μV/°C	-
Input Offset Current*8	Iio	25°C	-	0.5	30	nA	-
Input Bias Current *8	Ib	25°C	-	40	100	nA	-
Supply Current*9	IDD	25°C	-	300	400	μA	Av=0dB, VIN=2.5V
		Full range	-	-	600		
Maximum Output Voltage(High)	VOH	25°C	4.75	4.84	-	V	RL=600Ω to VDD/2
			4.85	4.90	-		RL=2kΩ to VDD/2
Maximum Output Voltage(Low)	VOL	25°C	-	170	250	mV	RL=600Ω to VDD/2
			-	100	150		RL=2kΩ to VDD/2
Large Signal Voltage Gain	Av	25°C	-	105	-	dB	RL=600Ω to VDD/2
			95	105	-		RL=2kΩ to VDD/2
Input Common-mode Voltage Range	Vicm	25°C	VSS	-	VDD-0.9	V	VSS to VDD
Common-mode Rejection Ratio	CMRR	25°C	72	90	-	dB	VCM=0.5V
Power supply reject-ratio	PSRR	25°C	75	85	-	dB	VDD=2.7V to 5.0V VCM=1V
Output Source Current *10	Isource	25°C	20	45	-	mA	OUT=0V, short current
Output Sink Current *10	Isink	25°C	20	40	-	mA	OUT=5V, short current
Slew Rate	SR	25°C	-	2.0	-	V/μs	CL=25pF
Gain Bandwidth	GBW	25°C	-	5	-	MHz	CL=25pF, Av=40dB f=1MHz
Phase Margin	θ	25°C	-	45	-	Deg	CL=25pF, Av=40dB
Gain Margin	GM	25°C	-	4.5	-	dB	CL=25pF, Av=40dB
Input Referred Noise Voltage	Vn	25°C	-	42	-	$nV/\sqrt{Hz}$	f=1kHz
Total Harmonic Distortion + Noise	THD+N	25°C	-	0.01	-	%	OUT=4.1V_{P-P}, f=1kHz RL=10kΩ Av=0dB, DIN-AUDIO

*8 Absolute value
*9 Full range: Ta=-40°C to +85°C
*10 Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

Description of electrical characteristics

Described here are the terms of electric characteristics used in this datasheet. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacture's document or general document.

1. Absolute maximum ratings

Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

1.1 Power supply voltage (VDD/VSS)

Indicates the maximum voltage that can be applied between the positive power supply terminal and negative power supply terminal without deterioration or destruction of characteristics of internal circuit.

1.2 Differential input voltage (Vid)

Indicates the maximum voltage that can be applied between non-inverting terminal and inverting terminal without deterioration and destruction of characteristics of IC.

1.3 Input common-mode voltage range (Vicm)

Indicates the maximum voltage that can be applied to non-inverting terminal and inverting terminal without deterioration or destruction of characteristics. Input common-mode voltage range of the maximum ratings not assures normal operation of IC. When normal Operation of IC is desired, the input common-mode voltage of characteristics item must be followed.

1.4 Power dissipation (Pd)

Indicates the power that can be consumed by specified mounted board at the ambient temperature 25℃(normal temperature). As for package product, Pd is determined by the temperature that can be permitted by IC chip in the package (maximum junction temperature) and thermal resistance of the package.

2.Electrical characteristics item

2.1 Input offset voltage (Vio)

Indicates the voltage difference between non-inverting terminal and inverting terminal. It can be translated into the input voltage difference required for setting the output voltage at 0 V.

2.2 Input offset voltage drift (△Vio/△T)

Denotes the ratio of the input offset voltage fluctuation to the ambient temperature fluctuation.

2.3 Input offset current (Iio)

Indicates the difference of input bias current between non-inverting terminal and inverting terminal.

2.4 Input bias current (Ib)

Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias current at non-inverting terminal and input bias current at inverting terminal.

2.5 Circuit current (IDD)

Indicates the IC current that flows under specified conditions and no-load steady status.

2.6 Maximum Output Voltage(High) / Maximum Output Voltage(Low) (VOH/VOL)

Indicates the voltage range that can be output by the IC under specified load condition. It is typically divided into maximum output voltage High and low. Maximum output voltage high indicates the upper limit of output voltage. Maximum output voltage low indicates the lower limit.

2.7 Output source current/ output sink current (Isource/Isink)

The maximum current that can be output under specific output conditions, it is divided into output source current and output sink current. The output source current indicates the current flowing out of the IC, and the output sink current the current flowing into the IC.

2.8 Large signal voltage gain (Av)

Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.

Av = (Output voltage fluctuation) / (Input offset fluctuation)

2.9 Input common-mode voltage range (Vicm)

Indicates the input voltage range where IC operates normally.

2.10 Common-mode rejection ratio (CMRR)

Indicates the ratio of fluctuation of input offset voltage when in-phase input voltage is changed. It is normally the fluctuation of DC.

CMRR = (Change of Input common-mode voltage)/(Input offset fluctuation)

2.11 Power supply rejection ratio (PSRR)

Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC. PSRR= (Change of power supply voltage)/(Input offset fluctuation)

2.12 Slew rate (SR)

Indicates the time fluctuation ratio of voltage output when step input signal is applied.

2.13 Gain Band Width (GBW)

Indicates to multiply by the frequency and the gain where the voltage gain decreases 6dB/octave.

2.14 Phase Margin (θ)

Indicates the margin of phase from 180 degree phase lag at unity gain frequency.

2.15 Gain Margin (GM)

Indicates the difference between 0dB and the gain where operational amplifier has 180 degree phase delay.

2.16 Total harmonic distortion + Noise (THD+N)

Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

2.17 Input referred noise voltage (Vn)

Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input terminal.

●**Typical Performance Curves**
○**LMR821G**

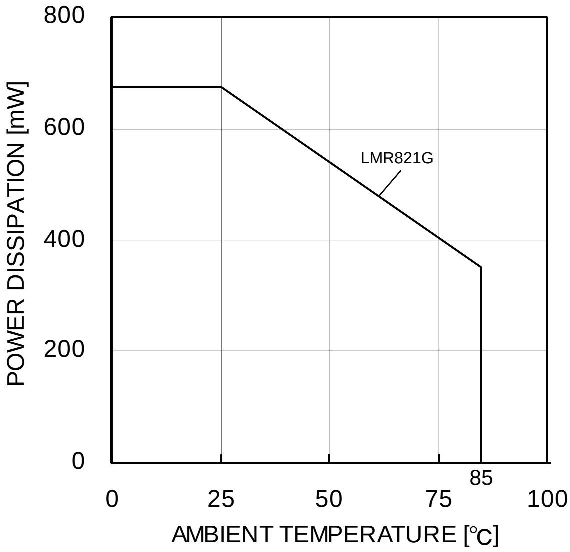


Figure 2.
Derating curve

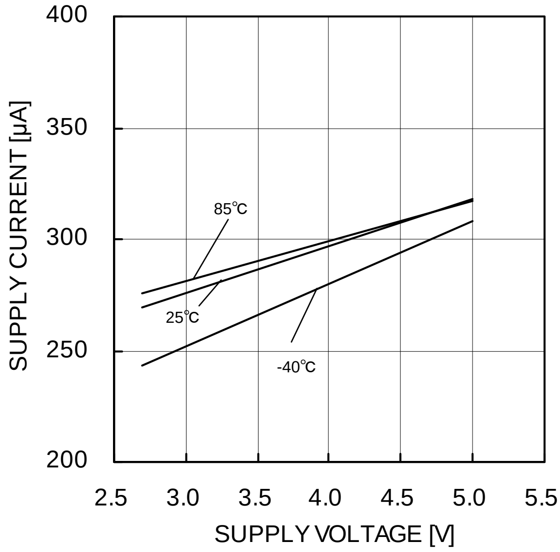


Figure 3.
Supply Current – Supply Voltage

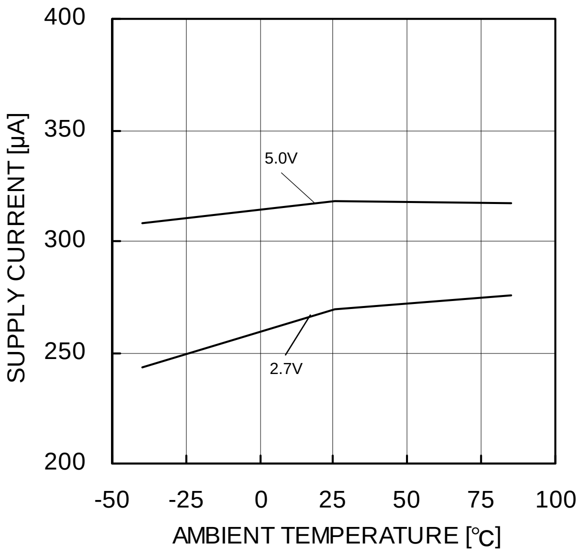


Figure 4.
Supply Current – Ambient Temperature

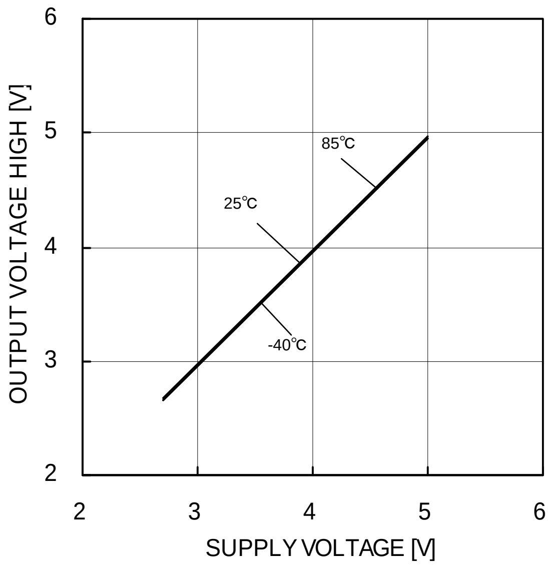


Figure 5.
Output Voltage High – Supply Voltage
(RL=2kΩ)

(*)The data above is measurement value of typical sample, it is not guaranteed.

●Typical Performance Curves (Reference data) – Continued

○**LMR821G**

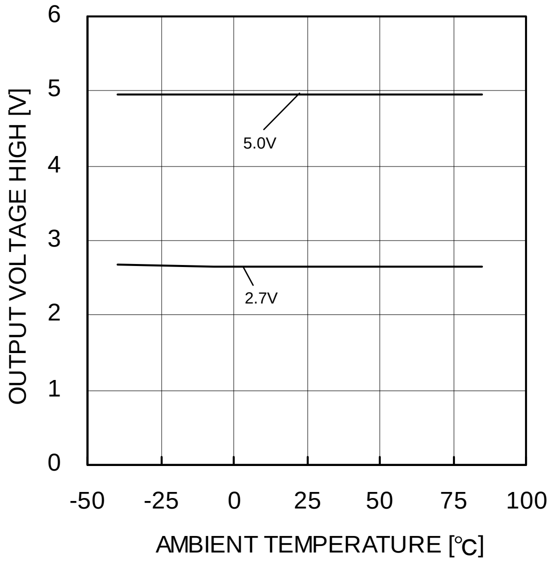


Figure 6.
Output Voltage High – Ambient Temperature
(RL=2kΩ)

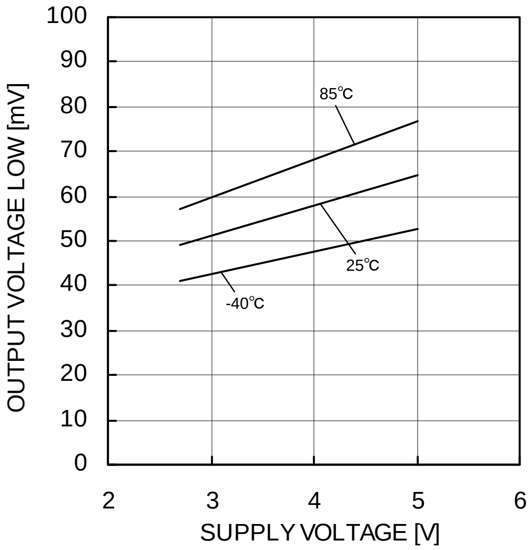


Figure 7.
Output Voltage Low – Supply Voltage
(RL=2kΩ)

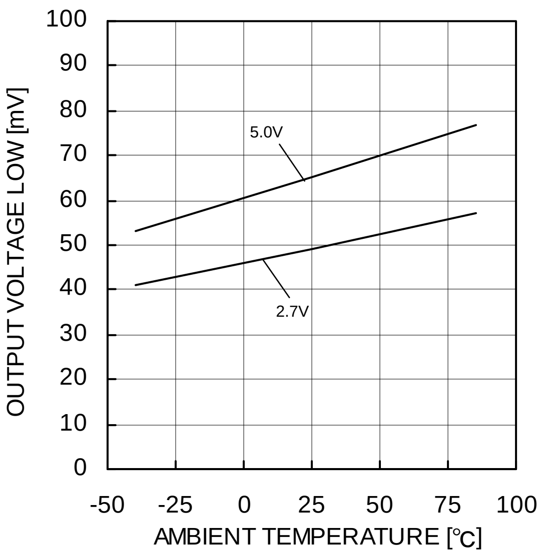


Figure 8.
Output Voltage Low –Ambient Temperature
(RL=2kΩ)

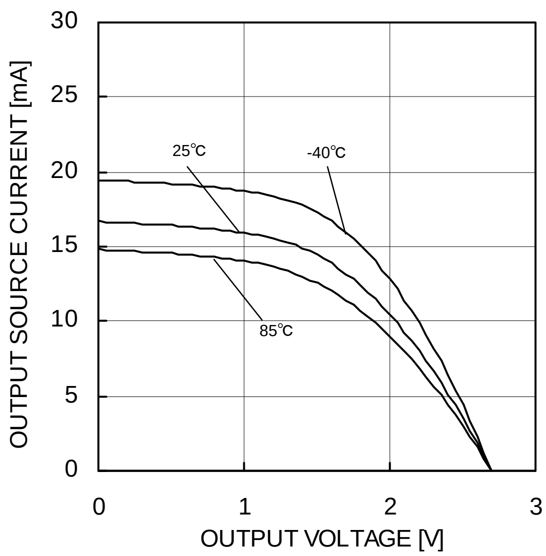


Figure 9.
Output Source Current – Output Voltage
(VDD=2.7V)

(*)The data above is measurement value of typical sample, it is not guaranteed.

● Typical Performance Curves (Reference data) – Continued

○ **LMR821G**

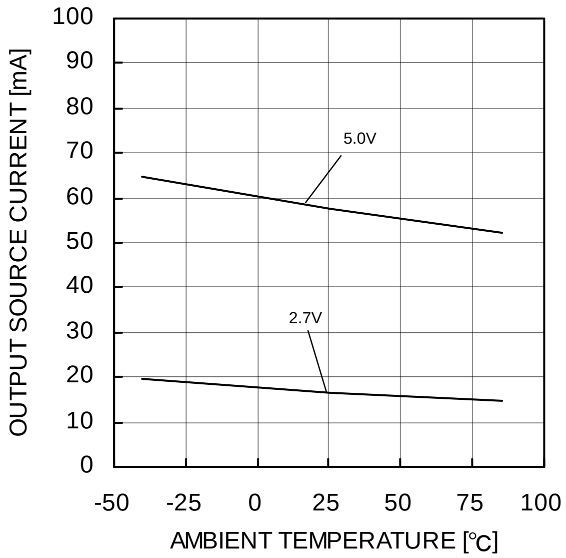


Figure 10.
Output Source Current –Ambient Temperature

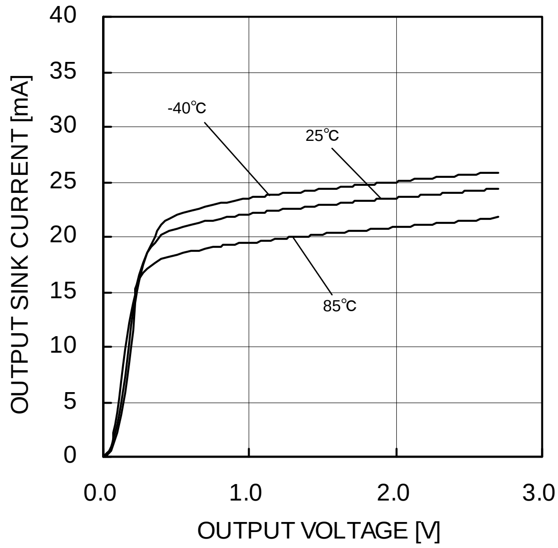


Figure 11.
Output Sink Current – Output Voltage
(VDD=2.7V)

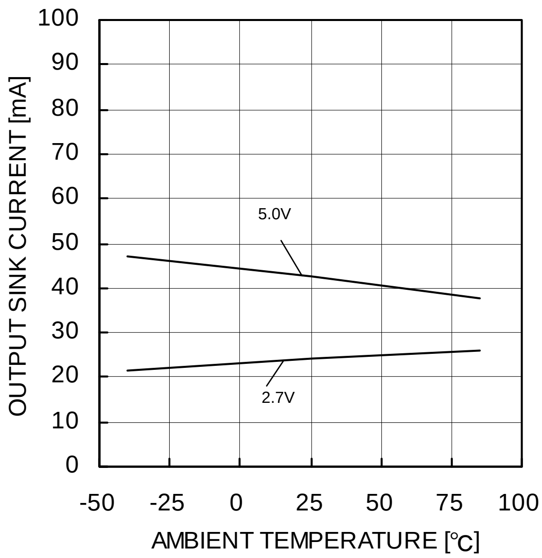


Figure 12.
Output Sink Current – Ambient Temperature

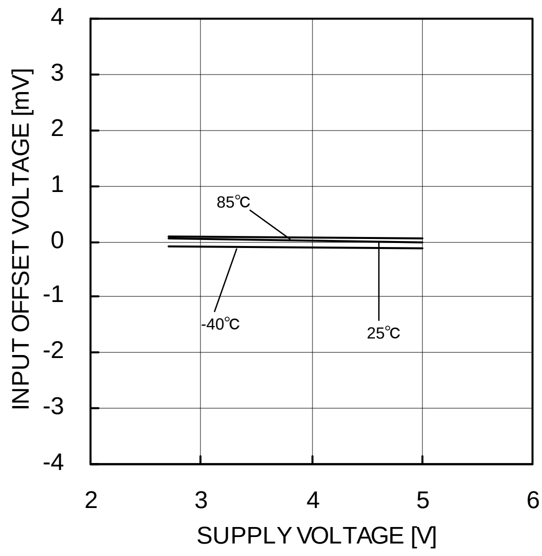


Figure 13.
Input Offset Voltage – Supply Voltage

(*)The data above is measurement value of typical sample, it is not guaranteed.

●Typical Performance Curves (Reference data) - Continued

○**LMR821G**

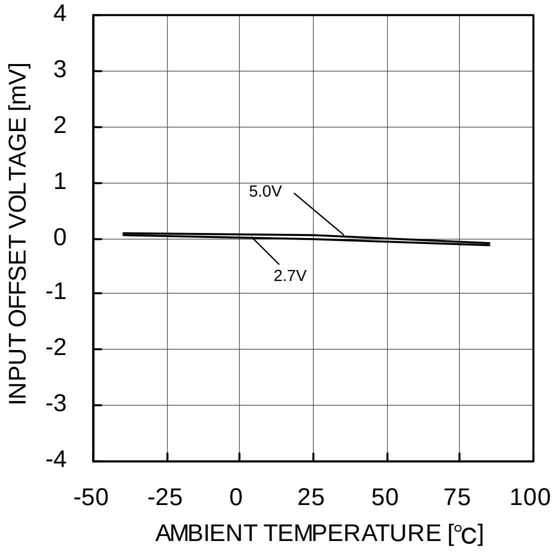


Figure 14.
Input Offset Voltage – Ambient Temperature

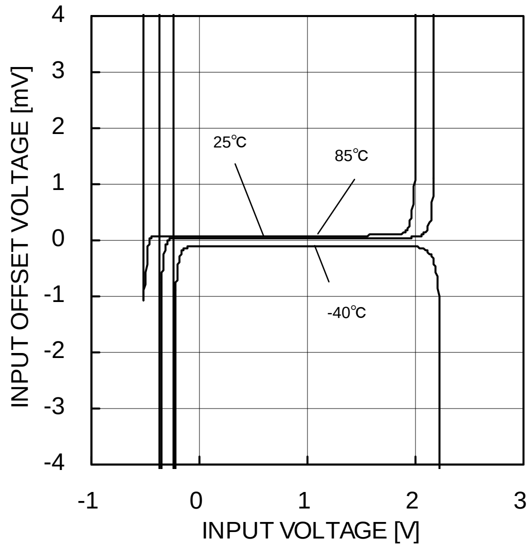


Figure 15.
Input Offset Voltage – Input Voltage
(VDD=2.7V)

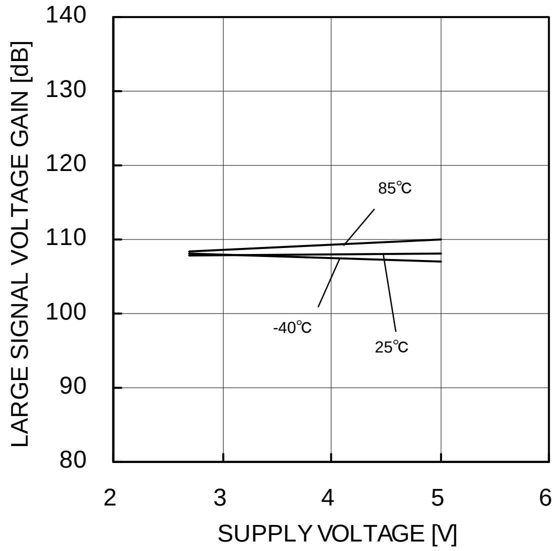


Figure 16.
Large Signal Voltage Gain – Supply Voltage

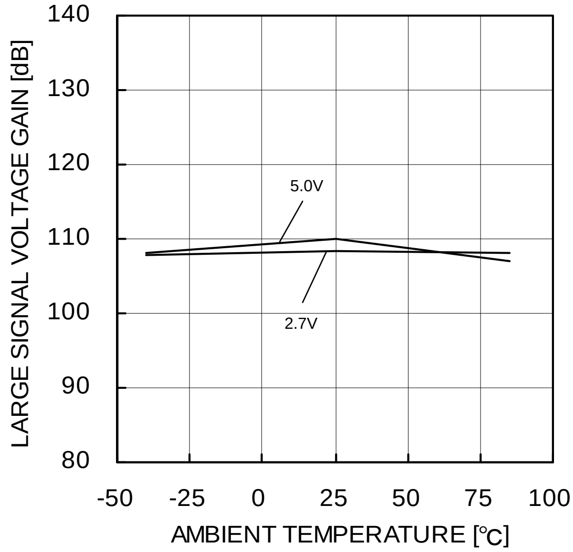


Figure 17.
Large Signal Voltage Gain – Ambient Temperature

(*)The data above is measurement value of typical sample, it is not guaranteed.

●Typical Performance Curves (Reference data) – Continued

○**LMR821G**

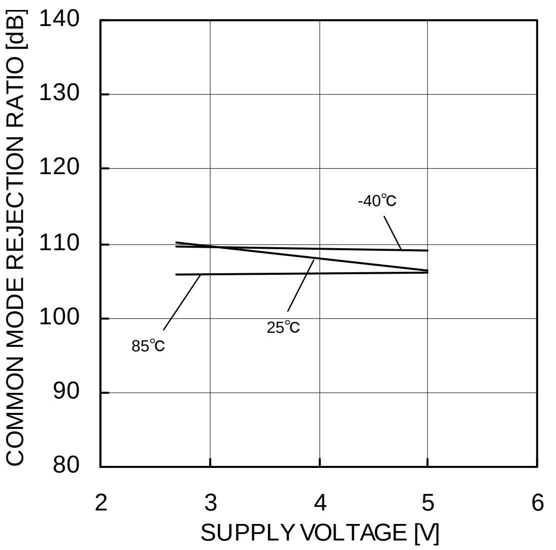


Figure 18.
Common Mode Rejection Ratio – Supply Voltage
(VDD=2.7V)

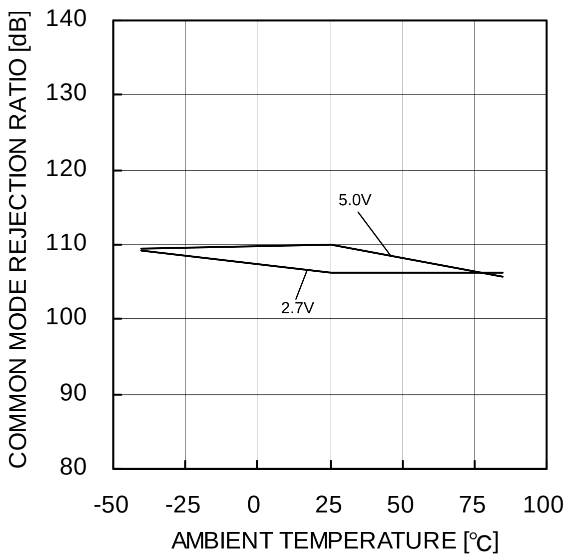


Figure 19.
Common Mode Rejection Ratio – Ambient Temperature

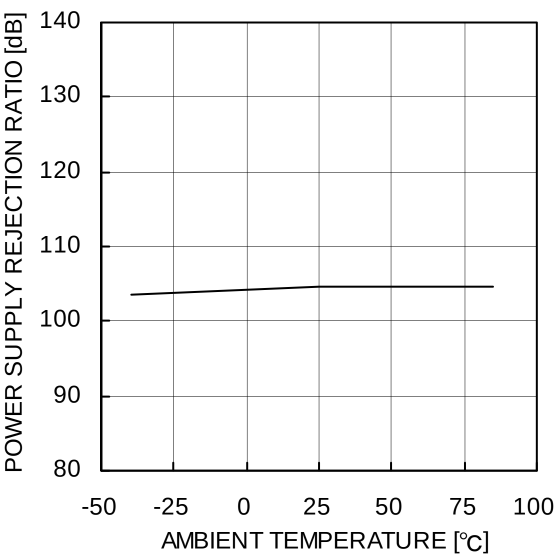


Figure 20.
Power Supply Rejection Ratio – Ambient Temperature
(VDD=2.7V~5.0V)

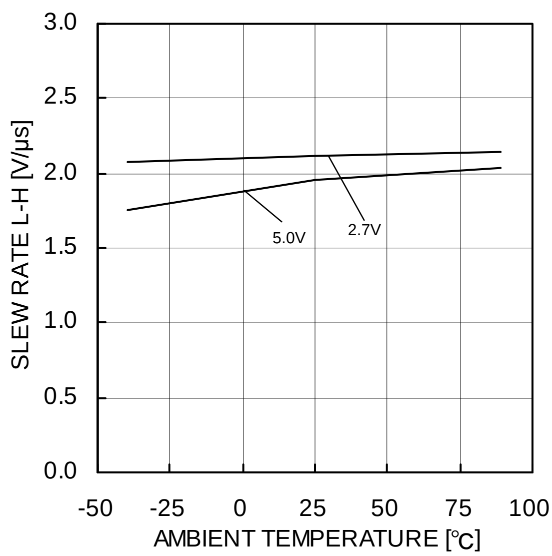


Figure 21.
Slew Rate L-H – Ambient Temperature

(*)The data above is measurement value of typical sample, it is not guaranteed.

●Typical Performance Curves (Reference data) - Continued

○**LMR821G**

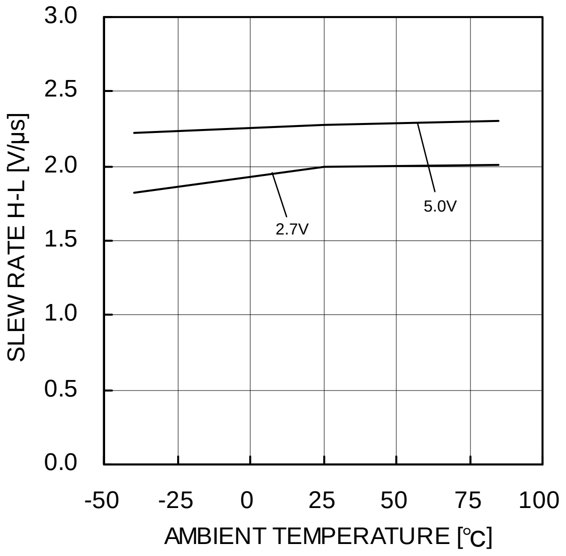


Figure 22.
Slew Rate H-L – Ambient Temperature

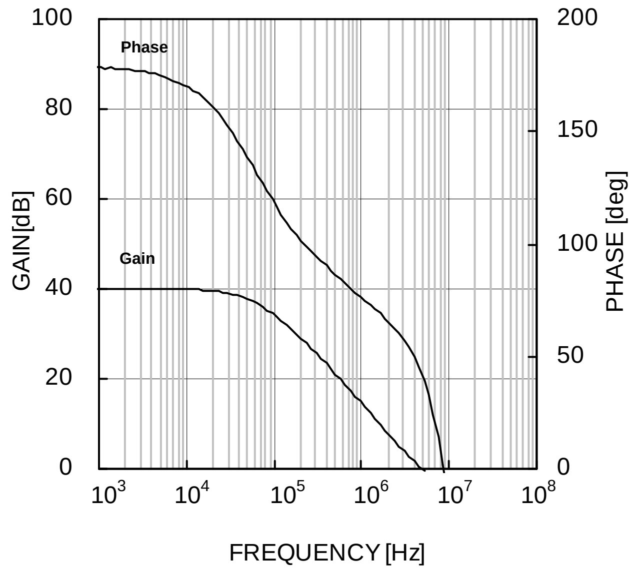


Figure 23.
Voltage Gain, Phase – Frequency

(*)The data above is measurement value of typical sample, it is not guaranteed.

●Application Information

NULL method condition for Test Circuit 1

VDD, VSS, EK, Vicm Unit:V

Parameter	VF	S1	S2	S3	VDD	VSS	EK	Vicm	Calculation
Input Offset Voltage	VF1	ON	ON	OFF	3	0	-1.5	3	1
Large Signal Voltage Gain	VF2	ON	ON	ON	3	0	-0.5	1.5	2
	VF3						-2.5		
Common-mode Rejection Ratio (Input Common-mode Voltage Range)	VF4	ON	ON	OFF	3	0	-1.5	0	3
	VF5							3	
Power Supply Rejection Ratio	VF6	ON	ON	OFF	2.5	0	-1.2	0	4
	VF7				5.0				

－ Calculation－

1. Input Offset Voltage (Vio)

$$Vio = \frac{|VF1|}{1+RF/RS} \; [V]$$

2. Large Signal Voltage Gain(Av)

$$Av = 20Log \frac{2 \times (1+RF/RS)}{|VF2-VF3|} \; [dB]$$

3. Common-mode Rejection Ratio (CMRR)

$$CMRR = 20Log \frac{3 \times (1+RF/RS)}{|VF4 - VF5|} \; [dB]$$

4. Power Supply Rejection Ratio (PSRR)

$$PSRR = 20Log \frac{3.2 \times (1+ RF/RS)}{|VF6 - VF7|} \; [dB]$$

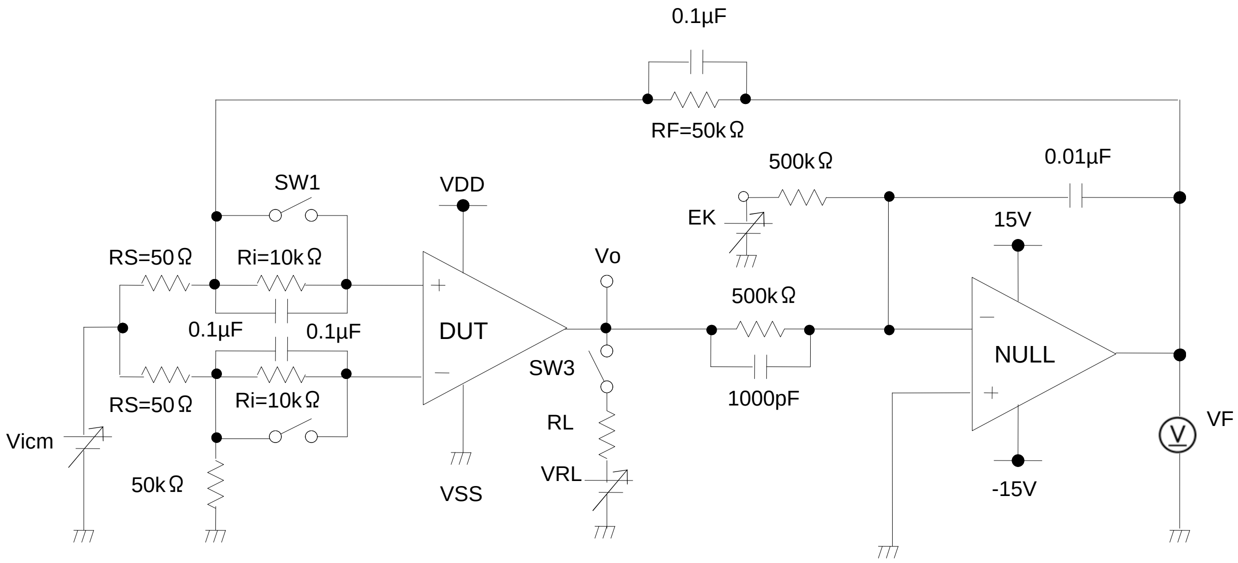


Figure 24. Test circuit1

●**Switch Condition for Test Circuit 2**

SW No.	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12
Supply Current	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage RL=10kΩ	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
Output Current	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Slew Rate	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
Unity gain Frequency	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON

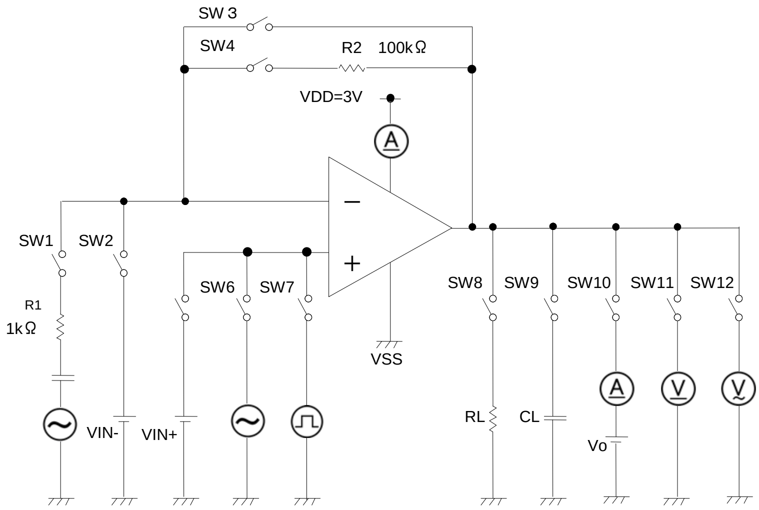


Figure 25. Test circuit2

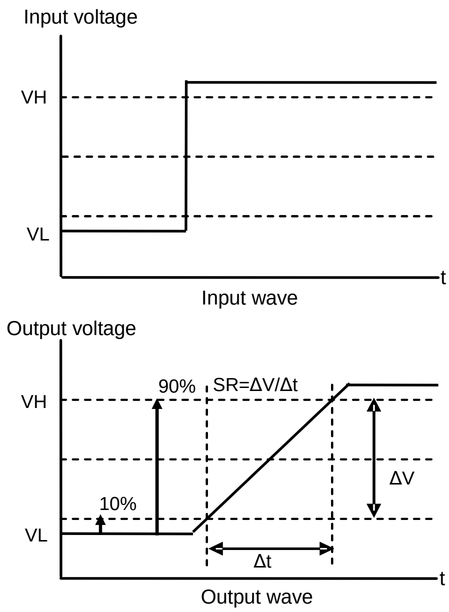


Figure 26. Slew rate input output wave

● Examples of circuit

○ Voltage follower

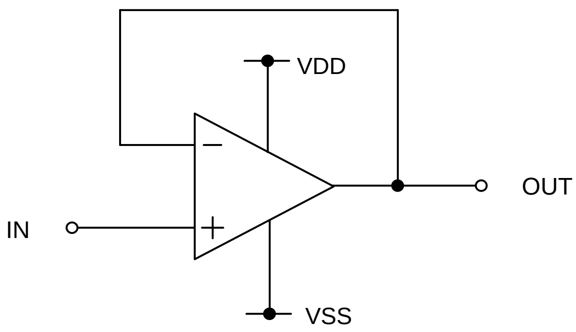


Figure 27. Voltage follower

Voltage gain is 0dB.
This circuit controls output voltage (OUT) equal input voltage (IN), and keeps OUT with stable because of high input impedance and low output impedance.
OUT is shown next expression.
OUT=IN

○ Inverting amplifier

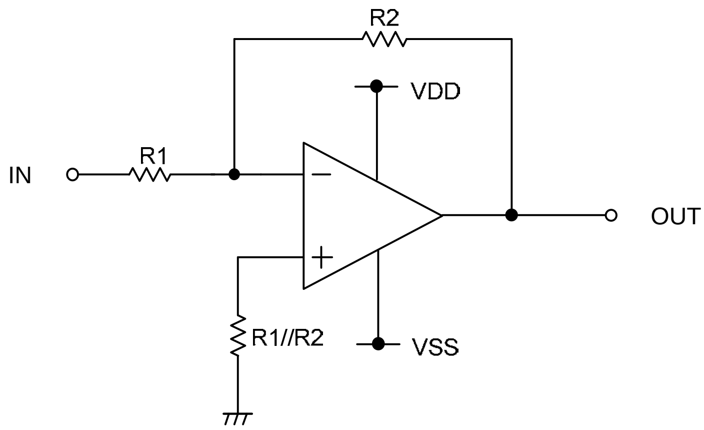


Figure 28. Inverting amplifier circuit

For inverting amplifier, Vi(b) Derating curve voltage gain decided R1 and R2, and phase reversed voltage is output.
OUT is shown next expression.
OUT=-(R2/R1)・IN
Input impedance is R1.

○ Non-inverting amplifier

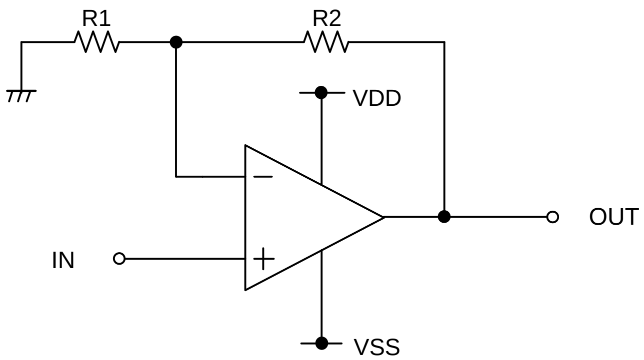


Figure 29. Non-inverting amplifier circuit

For non-inverting amplifier, IN is amplified by voltage gain decided R1 and R2, and phase is same with IN.
OUT is shown next expression.
OUT=(1 + R2/R1)・IN
This circuit performes high input impedance because Input impedance is operational amplifier’s input Impedance.

●**Power Dissipation**

Power dissipation (total loss) indicates the power that can be consumed by IC at Ta=25℃(normal temperature).IC is heated when it consumed power, and the temperature of IC ship becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance, represented by the symbol θja℃/W. The temperature of IC inside the package can be estimated by this thermal resistance.

Figure 30. (a) shows the model of thermal resistance of the package. Thermal resistance θja, ambient temperature Ta, maximum junction temperature Tjmax, and power dissipation Pd can be calculated by the equation below:

$$\theta ja = (Tjmax - Ta) / Pd \quad ℃/W \quad \cdot\cdot\cdot\cdot\cdot \quad (I)$$

Derating curve in Figure 30. (b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θja. Thermal resistance θja depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 31. show a derating curve for an example of LMR821

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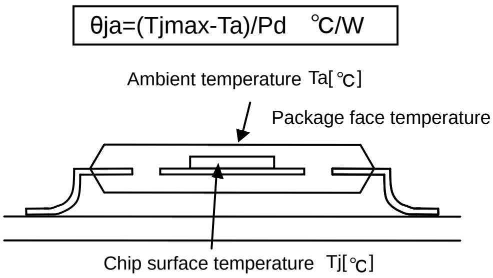
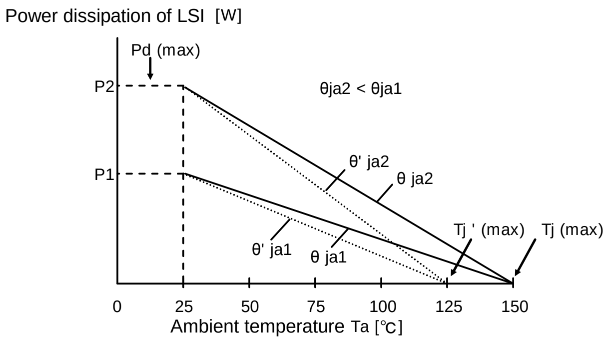
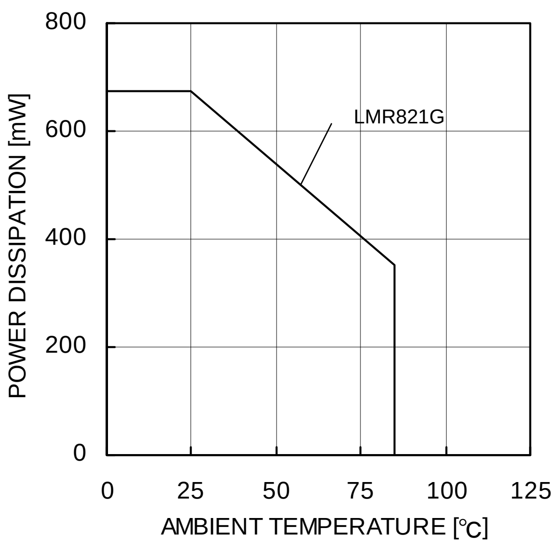


(a) Thermal resistance



(b) Derating curve

Figure 30. Thermal resistance and derating



5.4	mW/℃

When using the unit above Ta=25℃, subtract the value above per degree℃. Permissible dissipation is the value when FR4 glass epoxy board 70mm×70mm×1.6mm (cooper foil area below 3%) is mounted

Figure 31. Derating Curve

●**Operational Notes**

1) Unused circuits
When there are unused circuits it is recommended that they are connected as in Figure 32., setting the non-inverting input terminal to a potential within input common-mode voltage range (Vicm).

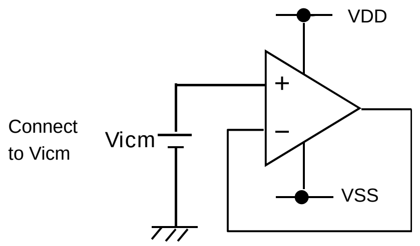


Figure 32. The example of application circuit for unused op-amp

2) Applied voltage to the input terminal
For normal circuit operation of voltage comparator, please input voltage for its input terminal within input common mode voltage VDD + 0.3V. Then, regardless of power supply voltage, VSS-0.3V can be applied to input terminals without deterioration or destruction of its characteristics.

3) Power supply (single / dual)
The op-amp operates when the specified voltage supplied is between VDD and VSS. Therefore, the single supply op-amp can be used as dual supply op-amp as well.

4) Power dissipation Pd
Using the unit in excess of the rated power dissipation may cause deterioration in electrical characteristics due to a rise in chip temperature, including reduced current capability. Therefore, please take into consideration the power dissipation (Pd) under actual operating conditions and apply a sufficient margin in thermal design. Refer to the thermal derating curves for more information.

5) Short-circuit between pins and erroneous mounting
Incorrect mounting may damage the IC. In addition, the presence of foreign particles between the outputs, the output and the power supply, or the output and GND may result in IC destruction.

6) Operation in a strong electromagnetic field
Operation in a strong electromagnetic field may cause malfunctions.

7) IC handling
Applying mechanical stress to the IC by deflecting or bending the board may cause fluctuations in the electrical characteristics due to piezo resistance effects.

8) Board inspection
Connecting a capacitor to a pin with low impedance may stress the IC. Therefore, discharging the capacitor after every process is recommended. In addition, when attaching and detaching the jig during the inspection phase, ensure that the power is turned OFF before inspection and removal. Furthermore, please take measures against ESD in the assembly process as well as during transportation and storage.

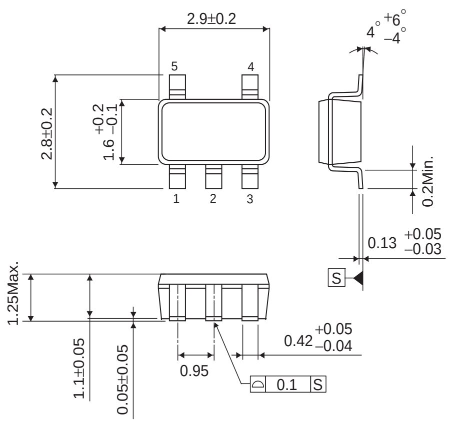
9) The IC destruction caused by capacitive load
The transistors in circuits may be damaged when VDD terminal and VSS terminal is shorted with the charged output terminal capacitor.When IC is used as a operational amplifier or as an application circuit, where oscillation is not activated by an output capacitor, the output capacitor must be kept below 0.1μF in order to prevent the damage mentioned above.

10) Latch up
Be careful of input voltage that exceed the VDD and VSS. When CMOS device have sometimes occur latch up operation. And protect the IC from abnormaly noise

11) Decupling capacitor
Insert the decupling capacitance between VDD and VSS, for stable operation of operational amplifier.

●Physical Dimensions Tape and Reel Information

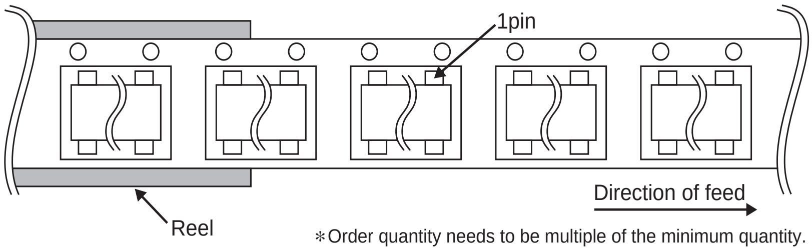
SSOP5



(Unit : mm)

<Tape and Reel information>

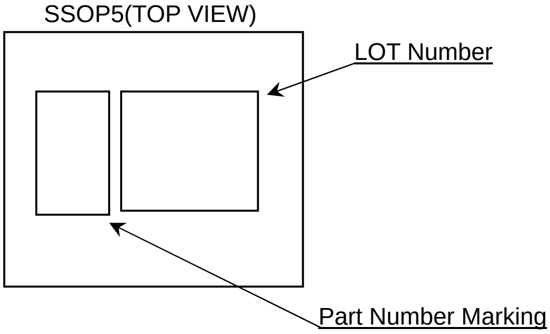
Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram

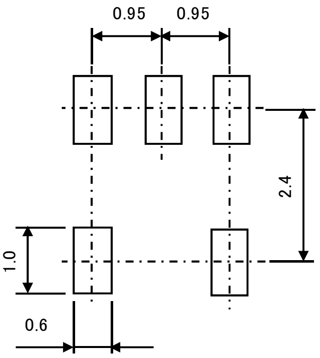
SSOP5(TOP VIEW)



Product Name		Package Type	Marking
LMR821	G	SSOP5	L3

●Land Pattern

SSOP5



Unit：mm

PKG	Land Pitch e	Land Space MIE	Land Length ≧ℓ 2	Land Width b2
SSOP5	0.95	2.4	1.0	0.6

●Revision History

Date	Revision	Changes
2013.1.18	001	New Release

Notice

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4) The Products are not subject to radiation-proof design.

5) Please verify and confirm characteristics of the final or mounted products in using the Products.

6) In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse) is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7) De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8) Confirm that operation temperature is within the specified range described in the product specification.

9) ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

●Precaution for Mounting / Circuit board design

1) When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2) In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

●Precautions Regarding Application Examples and External Circuits

1) If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2) You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

●Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

●Precaution for Storage / Transportation

1) Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2) Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3) Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4) Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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