

# Bias Resistor Transistors

## PNP Silicon Surface Mount Transistors With Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SOT-723 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- The SOT-723 Package can be Soldered using Wave or Reflow.
- Available in 4 mm, 8000 Unit Tape & Reel
- We declare that the material of product compliance with RoHS requirements.

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

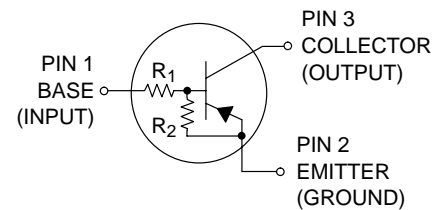
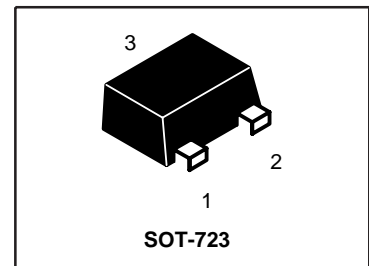
Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{CB0}$	50	Vdc
Collector-Emitter Voltage	$V_{CEO}$	50	Vdc
Collector Current	$I_C$	100	mAdc

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	260 (Note 1) 600 (Note 2) 2.0 (Note 1) 4.8 (Note 2)	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	480 (Note 1) 205 (Note 2)	$^\circ\text{C/W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad
2. FR-4 @ 1.0 x 1.0 inch Pad

## LDTA114EM3T5G Series



### MARKING DIAGRAM



- xx = Specific Device Code
- M = Date Code

**LDTA114EM3T5G\_Series****ORDERING INFORMATION, DEVICE MARKING AND RESISTOR VALUES**

Device	Marking	R1 (K)	R2 (K)	Package	Shipping
LDTA114EM3T5G	6A	10	10	SOT-723	8000/Tape & Reel
LDTA124EM3T5G	6B	22	22		
LDTA144EM3T5G	6C	47	47		
LDTA114YM3T5G	6D	10	47		
LDTA114TM3T5G	6E	10	∞		
LDTA143TM3T5G	6F	4.7	∞		
LDTA123EM3T5G	6H	2.2	2.2		
LDTA143EM3T5G	6J	4.7	4.7		
LDTA143ZM3T5G	6K	4.7	47		
LDTA124XM3T5G	6L	22	47		
LDTA123JM3T5G	6M	2.2	47		
LDTA115EM3T5G	6N	100	100		
LDTA144WM3T5G	6P	47	22		

**LDTA114EM3T5G\_Series**

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Base Cutoff Current ( $V_{CB} = 50\text{ V}, I_E = 0$ )	$I_{CBO}$	–	–	100	nAdc
Collector–Emitter Cutoff Current ( $V_{CE} = 50\text{ V}, I_B = 0$ )	$I_{CEO}$	–	–	500	nAdc
Emitter–Base Cutoff Current ( $V_{EB} = 6.0\text{ V}, I_C = 0$ )	$I_{EBO}$	–	–	0.5	mAdc
LDTA114EM3T5G		–	–	0.2	
LDTA124EM3T5G		–	–	0.1	
LDTA144EM3T5G		–	–	0.2	
LDTA114YM3T5G		–	–	0.9	
LDTA114TM3T5G		–	–	1.9	
LDTA143TM3T5G		–	–	2.3	
LDTA123EM3T5G		–	–	1.5	
LDTA143EM3T5G		–	–	0.18	
LDTA143ZM3T5G		–	–	0.13	
LDTA124XM3T5G		–	–	0.2	
LDTA123JM3T5G		–	–	0.05	
LDTA115EM3T5G		–	–	0.13	
LDTA144WM3T5G		–	–		
Collector–Base Breakdown Voltage ( $I_C = 10\ \mu\text{A}, I_E = 0$ )	$V_{(BR)CBO}$	50	–	–	Vdc
Collector–Emitter Breakdown Voltage (Note 3.) ( $I_C = 2.0\text{ mA}, I_B = 0$ )	$V_{(BR)CEO}$	50	–	–	Vdc

**ON CHARACTERISTICS** (Note 3.)

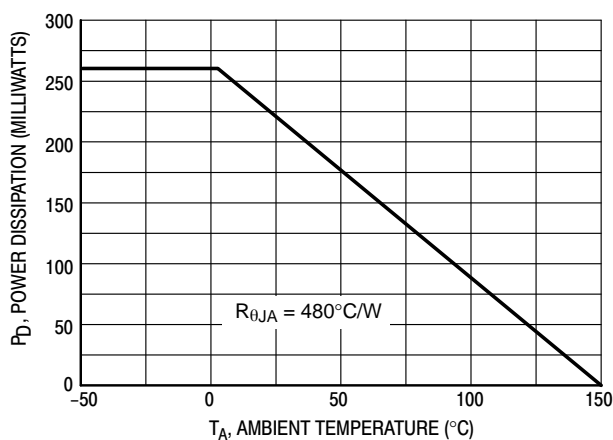
DC Current Gain ( $V_{CE} = 10\text{ V}, I_C = 5.0\text{ mA}$ )	$h_{FE}$	35	60	–	
LDTA114EM3T5G		60	100	–	
LDTA124EM3T5G		80	140	–	
LDTA144EM3T5G		80	140	–	
LDTA114YM3T5G		160	250	–	
LDTA114TM3T5G		160	250	–	
LDTA143TM3T5G		8.0	15	–	
LDTA123EM3T5G		15	27	–	
LDTA143EM3T5G		80	140	–	
LDTA143ZM3T5G		80	130	–	
LDTA124XM3T5G		80	140	–	
LDTA123JM3T5G		80	150	–	
LDTA115EM3T5G		80	140	–	
LDTA144WM3T5G		80	140	–	
Collector–Emitter Saturation Voltage ( $I_C = 10\text{ mA}, I_E = 0.3\text{ mA}$ ) ( $I_C = 10\text{ mA}, I_B = 5\text{ mA}$ ) LDTA123EM3T5G ( $I_C = 10\text{ mA}, I_B = 1\text{ mA}$ ) LDTA114TM3T5G/LDTA143TM3T5G/ LDTA143ZM3T5G/LDTA124XM3T5G/LDTA143EM3T5G	$V_{CE(sat)}$	–	–	0.25	Vdc
Output Voltage (on) ( $V_{CC} = 5.0\text{ V}, V_B = 2.5\text{ V}, R_L = 1.0\text{ k}\Omega$ )	$V_{OL}$	–	–	0.2	Vdc
LDTA114EM3T5G		–	–	0.2	
LDTA124EM3T5G		–	–	0.2	
LDTA114YM3T5G		–	–	0.2	
LDTA114TM3T5G		–	–	0.2	
LDTA143TM3T5G		–	–	0.2	
LDTA123EM3T5G		–	–	0.2	
LDTA143EM3T5G		–	–	0.2	
LDTA143ZM3T5G		–	–	0.2	
LDTA124XM3T5G		–	–	0.2	
LDTA123JM3T5G		–	–	0.2	
( $V_{CC} = 5.0\text{ V}, V_B = 3.5\text{ V}, R_L = 1.0\text{ k}\Omega$ ) LDTA144EM3T5G		–	–	0.2	
( $V_{CC} = 5.0\text{ V}, V_B = 5.5\text{ V}, R_L = 1.0\text{ k}\Omega$ ) LDTA115EM3T5G		–	–	0.2	
( $V_{CC} = 5.0\text{ V}, V_B = 4.0\text{ V}, R_L = 1.0\text{ k}\Omega$ ) LDTA144WM3T5G		–	–	0.2	
Output Voltage (off) ( $V_{CC} = 5.0\text{ V}, V_B = 0.5\text{ V}, R_L = 1.0\text{ k}\Omega$ ) ( $V_{CC} = 5.0\text{ V}, V_B = 0.25\text{ V}, R_L = 1.0\text{ k}\Omega$ )	$V_{OH}$	4.9	–	–	Vdc
LDTA114TM3T5G					
LDTA143TM3T5G					
LDTA123EM3T5G					
LDTA143EM3T5G					

3. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%

**LDTA114EM3T5G\_Series**

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit	
Input Resistor	R1	LDTA114EM3T5G	7.0	10	13	k $\Omega$
		LDTA124EM3T5G	15.4	22	28.6	
		LDTA144EM3T5G	32.9	47	61.1	
		LDTA114YM3T5G	7.0	10	13	
		LDTA114TM3T5G	7.0	10	13	
		LDTA143TM3T5G	3.3	4.7	6.1	
		LDTA123EM3T5G	1.5	2.2	2.9	
		LDTA143EM3T5G	3.3	4.7	6.1	
		LDTA143ZM3T5G	3.3	4.7	6.1	
		LDTA124XM3T5G	15.4	22	28.6	
		LDTA123JM3T5G	1.54	2.2	2.86	
		LDTA115EM3T5G	70	100	130	
		LDTA144WM3T5G	32.9	47	61.1	
		Resistor Ratio /	R <sub>1</sub> /R <sub>2</sub>			
LDTA114EM3T5G/LDTA124EM3T5G/LDTA144EM3T5G		0.8	1.0	1.2		
LDTA115EM3T5G		0.17	0.21	0.25		
LDTA114YM3T5G		-	-	-		
LDTA114TM3T5G/LDTA143TM3T5G		0.8	1.0	1.2		
LDTA123EM3T5G/LDTA143EM3T5G		0.055	0.1	0.185		
LDTA143ZM3T5G		0.38	0.47	0.56		
LDTA124XM3T5G		0.038	0.047	0.056		
LDTA123JM3T5G		1.7	2.1	2.6		
LDTA144WM3T5G						



**Figure 1. Derating Curve**

LDTA114EM3T5G\_Series

TYPICAL ELECTRICAL CHARACTERISTICS – LDTA114EM3T5G

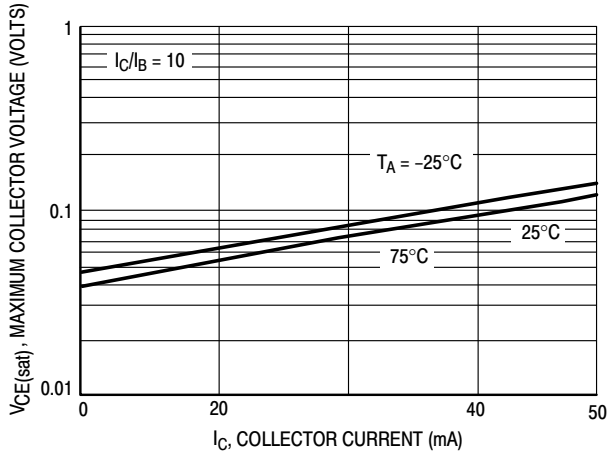


Figure 2.  $V_{CE(sat)}$  versus  $I_C$

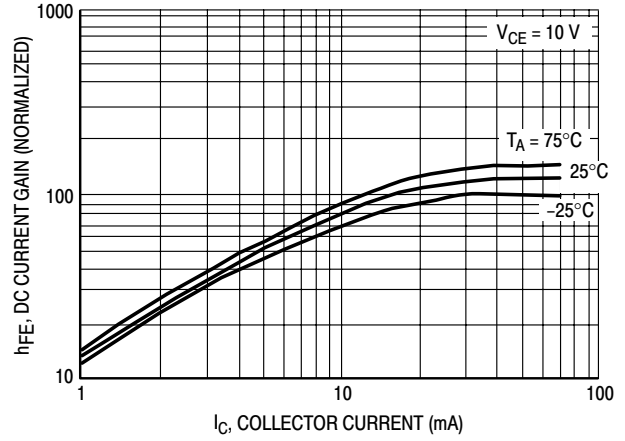


Figure 3. DC Current Gain

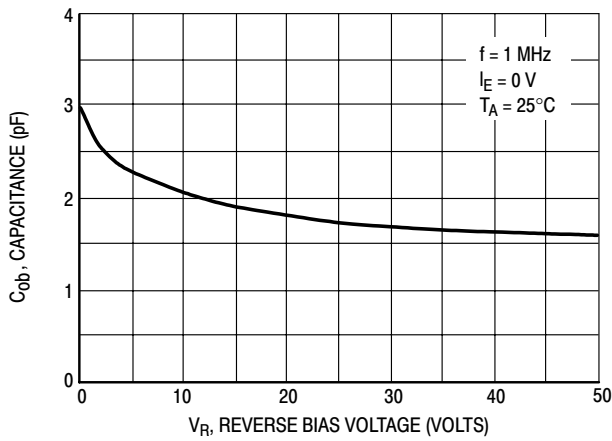


Figure 4. Output Capacitance

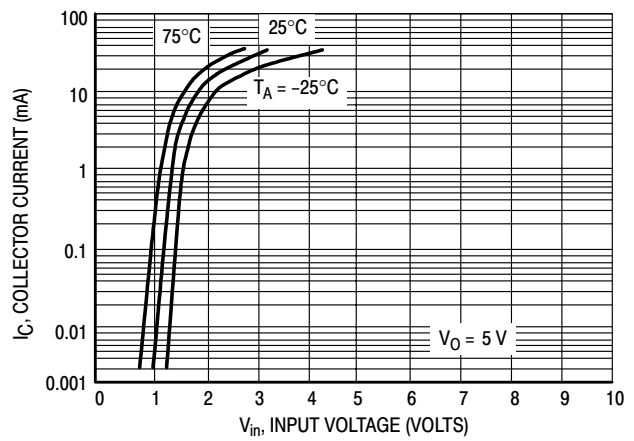


Figure 5. Output Current versus Input Voltage

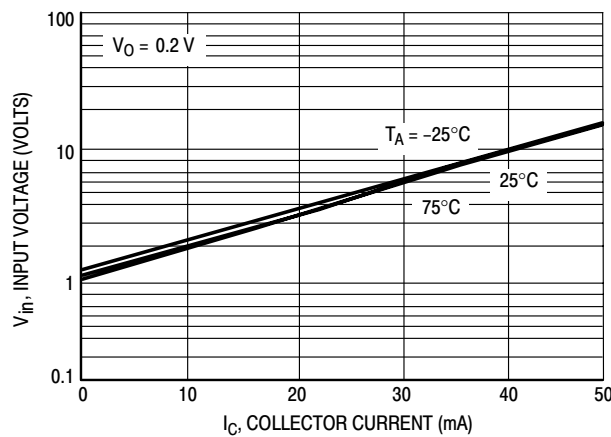


Figure 6. Input Voltage versus Output Current

LDTA114EM3T5G\_Series

TYPICAL ELECTRICAL CHARACTERISTICS – LDTA124EM3T5G

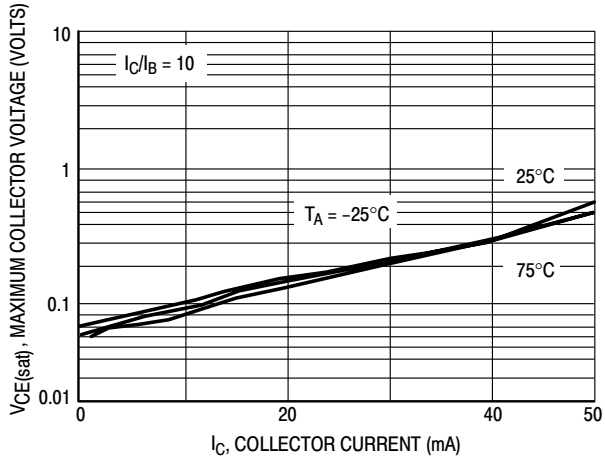


Figure 7.  $V_{CE(sat)}$  versus  $I_C$

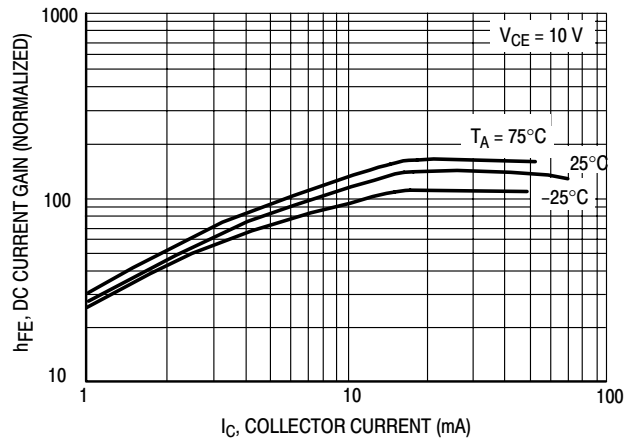


Figure 8. DC Current Gain

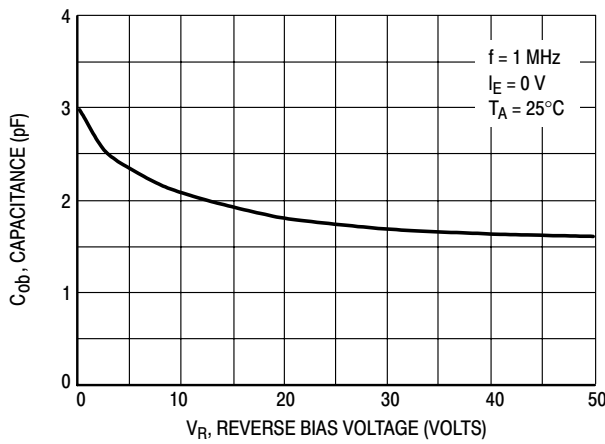


Figure 9. Output Capacitance

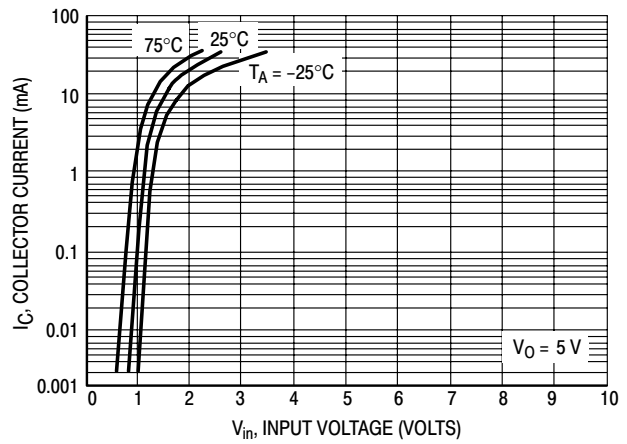


Figure 10. Output Current versus Input Voltage

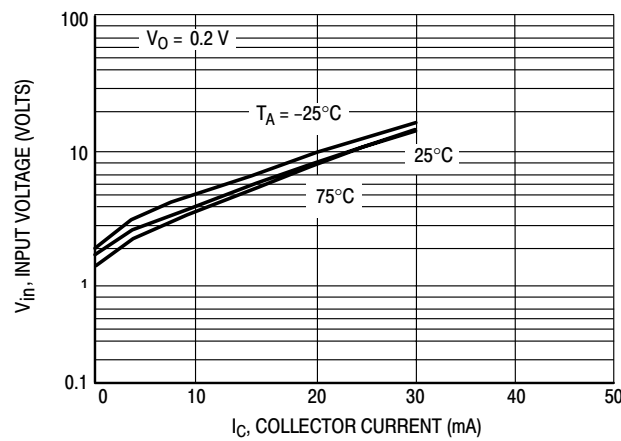


Figure 11. Input Voltage versus Output Current

LDTA114EM3T5G\_Series

TYPICAL ELECTRICAL CHARACTERISTICS – LDTA144EM3T5G

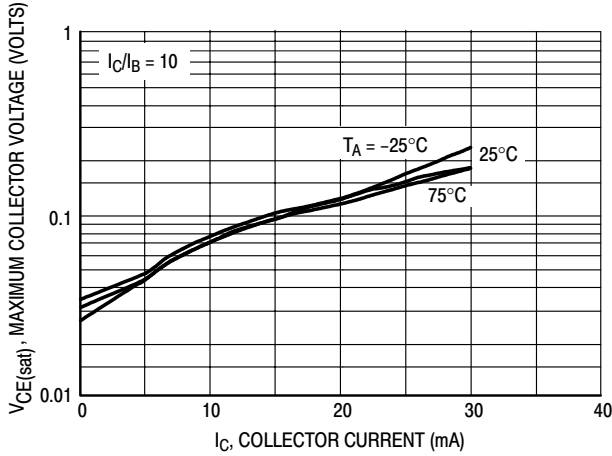


Figure 12.  $V_{CE(sat)}$  versus  $I_C$

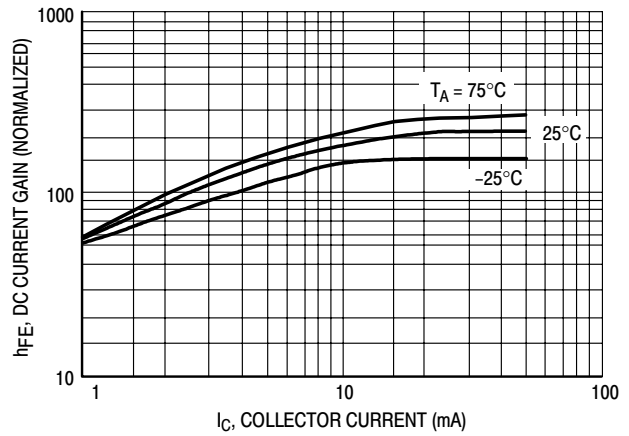


Figure 13. DC Current Gain

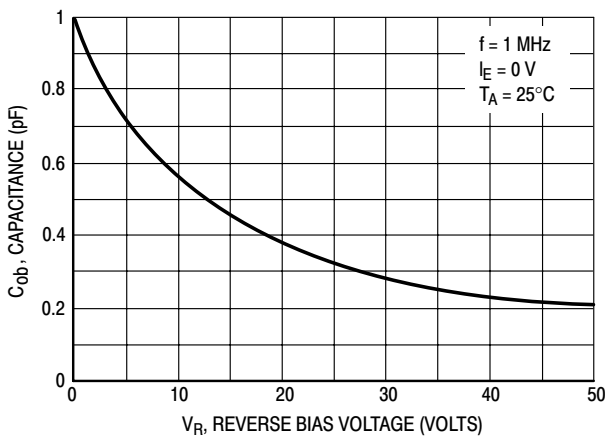


Figure 14. Output Capacitance

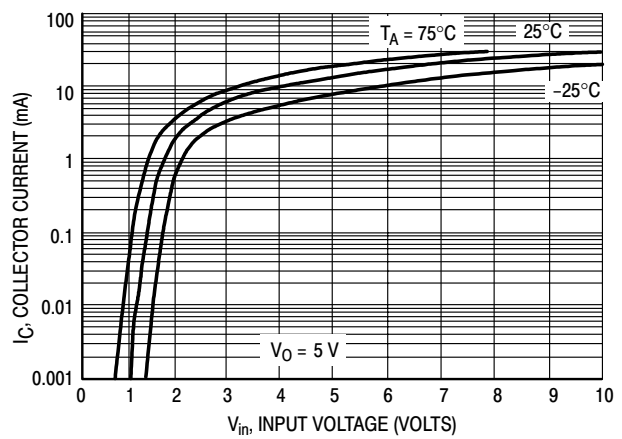


Figure 15. Output Current versus Input Voltage

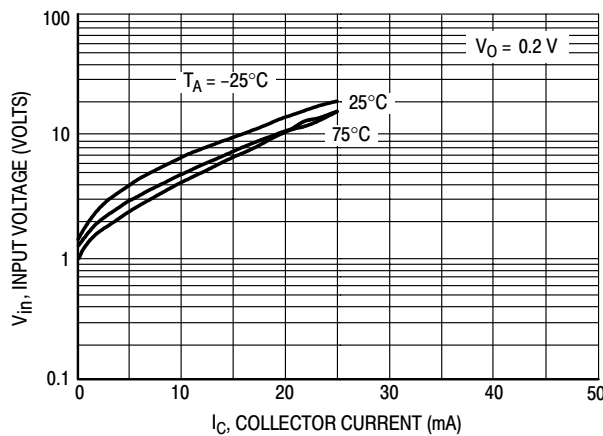


Figure 16. Input Voltage versus Output Current

LDTA114EM3T5G\_Series

TYPICAL ELECTRICAL CHARACTERISTICS – LDTA114YM3T5G

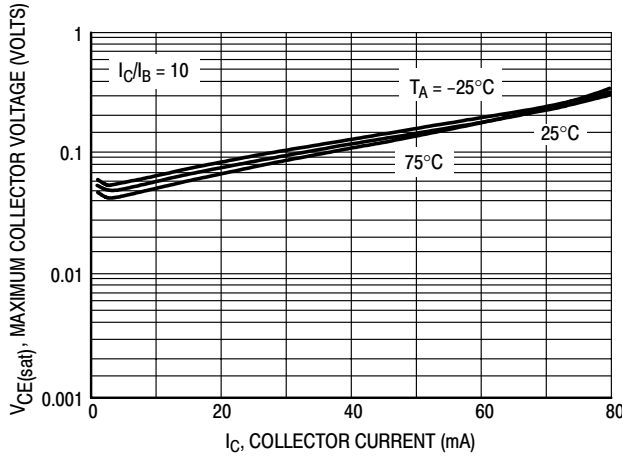


Figure 17.  $V_{CE(sat)}$  versus  $I_C$

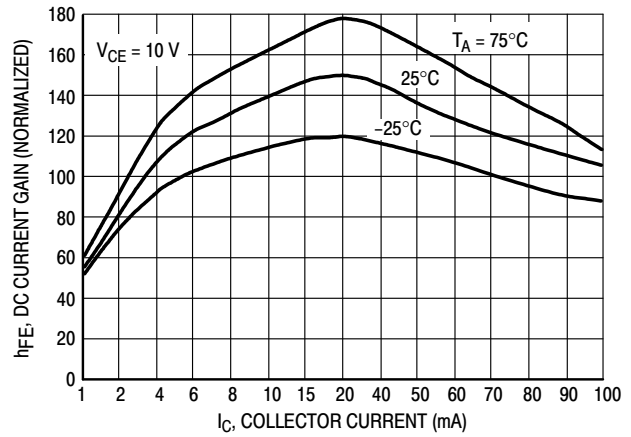


Figure 18. DC Current Gain

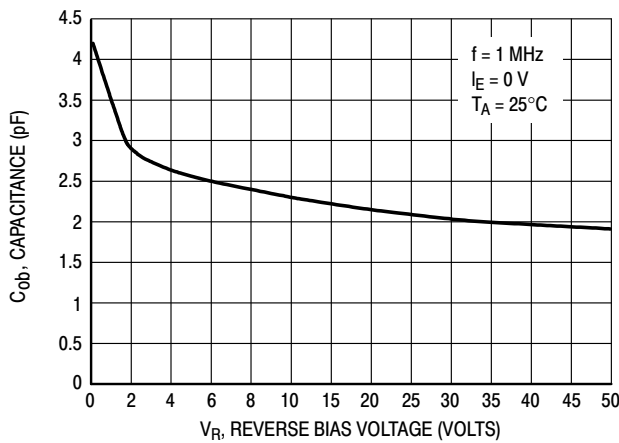


Figure 19. Output Capacitance

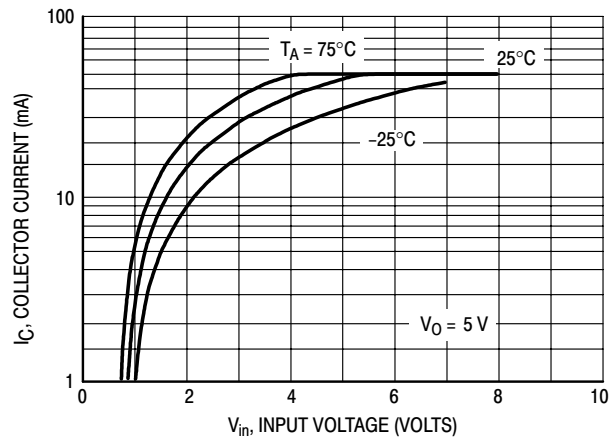


Figure 20. Output Current versus Input Voltage

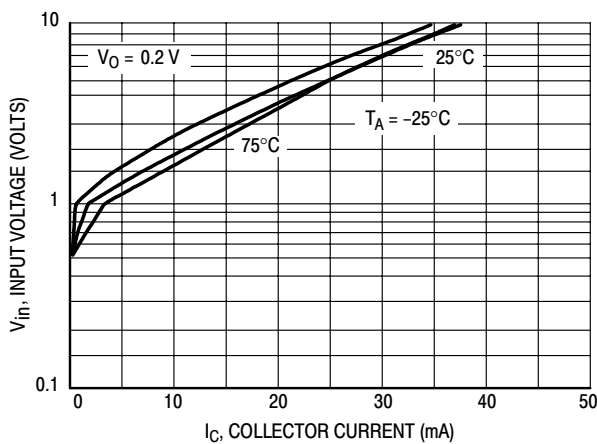


Figure 21. Input Voltage versus Output Current

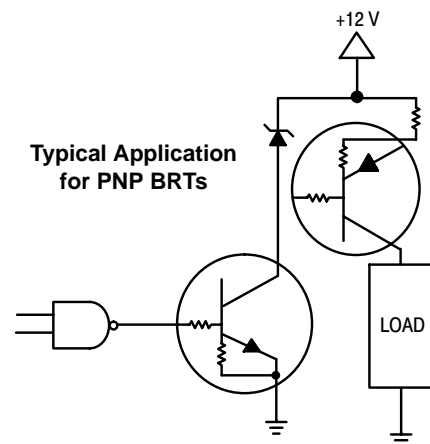


Figure 22. Inexpensive, Unregulated Current Source



LDTA114EM3T5G\_Series

TYPICAL ELECTRICAL CHARACTERISTICS — LDTA115EM3T5G

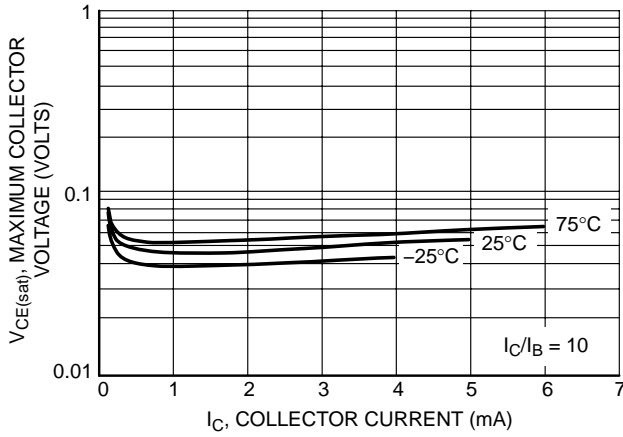


Figure 23. Maximum Collector Voltage versus Collector Current

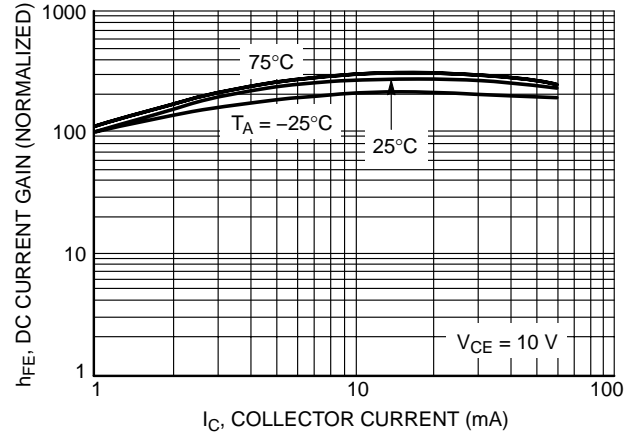


Figure 24. DC Current Gain

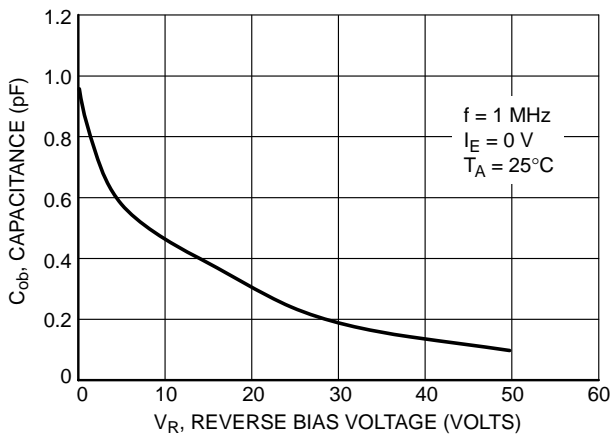


Figure 25. Output Capacitance

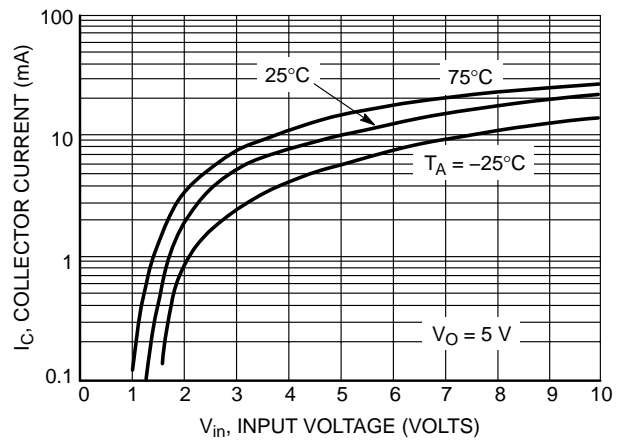


Figure 26. Output Current versus Input Voltage

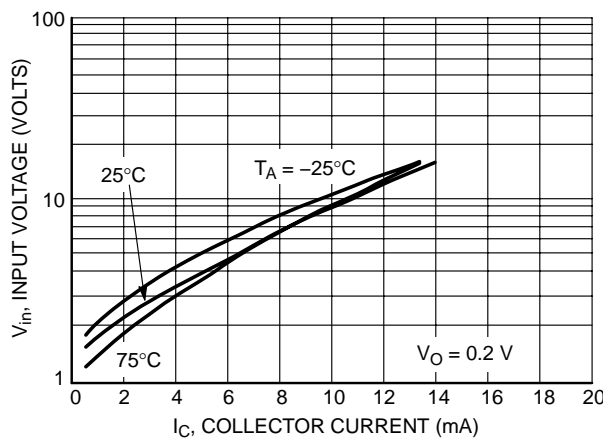


Figure 27. Input Voltage versus Output Current

LDTA114EM3T5G\_Series

TYPICAL ELECTRICAL CHARACTERISTICS — LDTA144WM3T5G

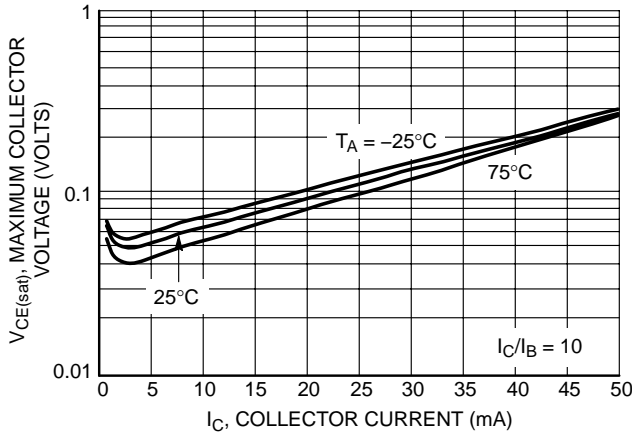


Figure 28. Maximum Collector Voltage versus Collector Current

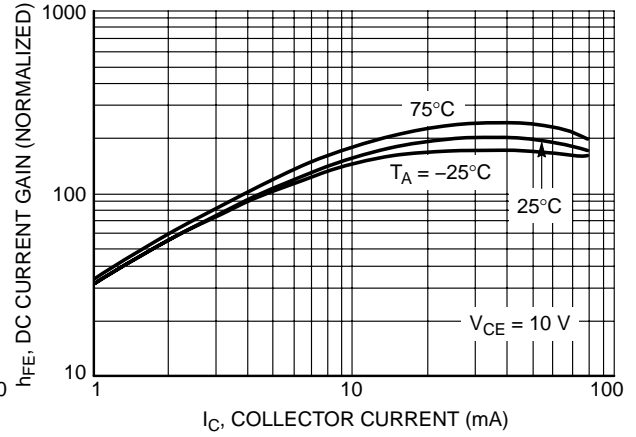


Figure 29. DC Current Gain

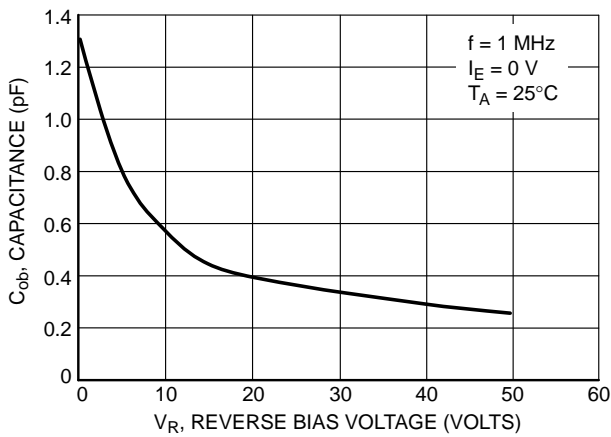


Figure 30. Output Capacitance

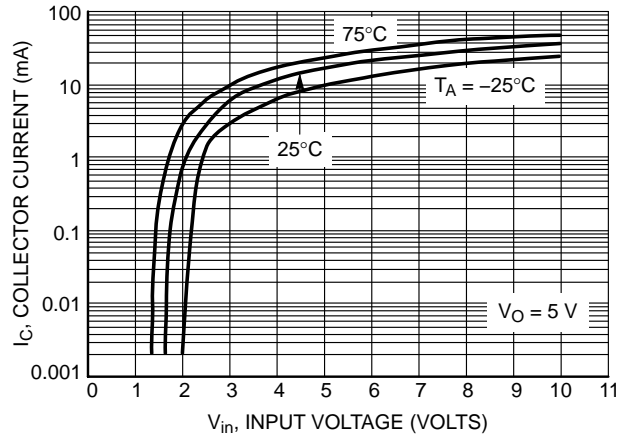


Figure 31. Output Current versus Input Voltage

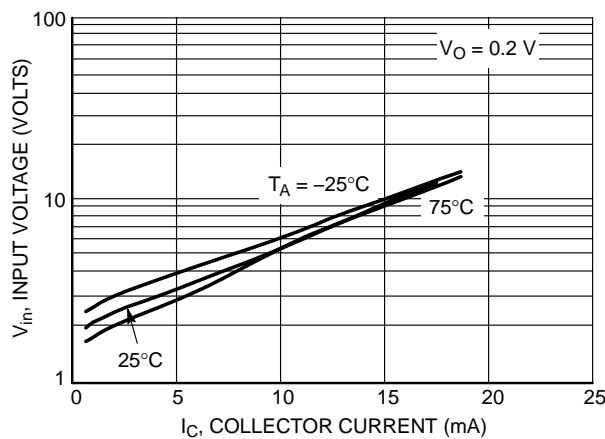
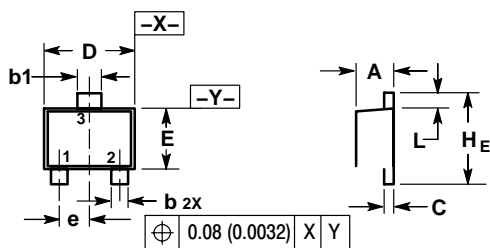


Figure 32. Input Voltage versus Output Current

**LDTA114EM3T5G\_Series**

**PACKAGE DIMENSIONS**

**SOT-723**



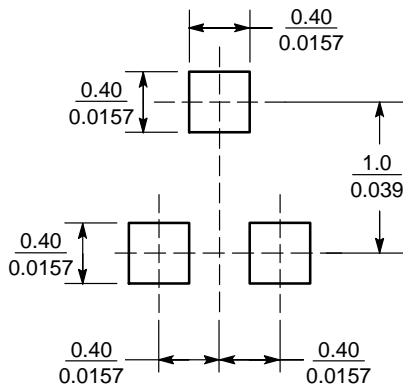
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
b	0.15	0.20	0.27	0.0059	0.0079	0.0106
b1	0.25	0.3	0.35	0.010	0.012	0.014
C	0.07	0.12	0.17	0.0028	0.0047	0.0067
D	1.15	1.20	1.25	0.045	0.047	0.049
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.40 BSC			0.016 BSC		
H E	1.15	1.20	1.25	0.045	0.047	0.049
L	0.15	0.20	0.25	0.0059	0.0079	0.0098

- PIN 1. BASE
2. EMITTER
3. COLLECTOR

**SOLDERING FOOTPRINT**



( mm / inches )