# 1024MB DDR3 – SDRAM UDIMM

**240 Pin UDIMM**

**SGU01G64A1BG1SA-xxR**

**1GByte in FBGA Technology**

**RoHS compliant**

## Options:

- Data Rate / Latency — Marking
  - DDR3 1066 MT/s CL7 — -BB
  - DDR3 1333 MT/s CL9 — -CC
  - DDR3 1600 MT/s CL11 — -DC
- Module Density
  1024MB with 8 dies and 1 rank

| | | |
|---|---|---|
| Standard Grade | ($T_A$) | 0°C to 70°C |
| | ($T_C$) | 0°C to 85°C |
| W-Grade | ($T_A$) | -40°C to 85°C |
| | ($T_C$) | -40°C to 95°C |

The refresh rate has to be doubled when 85°C<$T_C$<95°C

## Environmental Requirements:

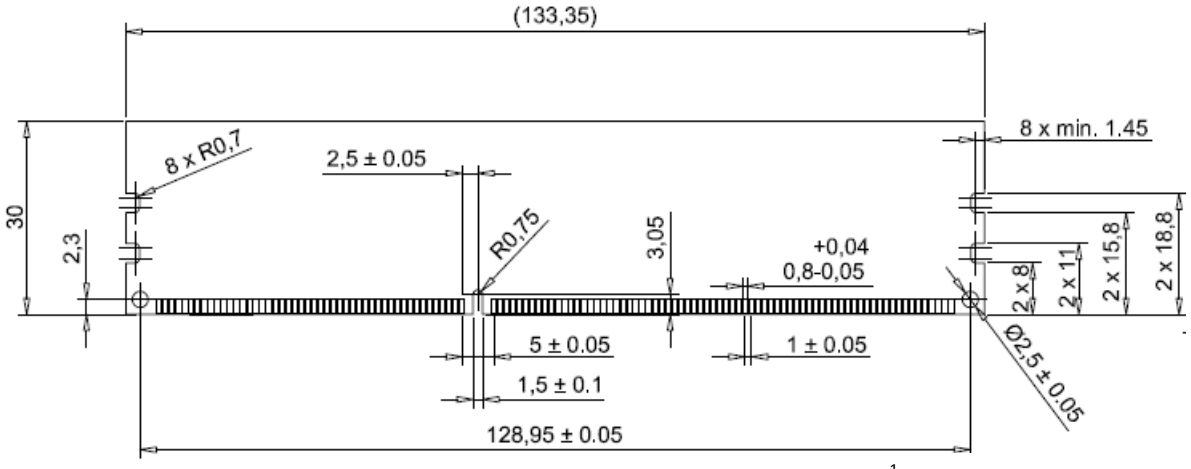
- Operating temperature (ambient)
  Standard Grade 0°C to 70°C
  W-Grade -40°C to 85°C
- Operating Humidity
  10% to 90% relative humidity, noncondensing
- Operating Pressure
  105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
  -55°C to 100°C
- Storage Humidity
  5% to 95% relative humidity, noncondensing
- Storage Pressure
  1682 PSI (up to 5000 ft.) at 50°C

## Features:

- 240-pin 64-bit DDR3 unbuffered Dual-In-Line Double Data Rate Synchronous DRAM module
- Module organization: single rank 128M x 64
- $V_{DD}$ = 1.5V ±0.075V, $V_{DDQ}$ 1.5V ±0.075V
- 1.5V I/O ( SSTL_15 compatible)
- serial presence-detect (SPD) EEPROM
- Gold-contact pads
- This module is fully pin and functional compatible to the JEDEC PC3-10600 spec. and JEDEC- Standard MO-269. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

- **DDR3 - SDRAM component Samsung K4B1G0846G**
- 128Mx8 DDR3 SDRAM in PG-TFBGA-78 package
- 8-bit pre-fetch architecture
- Programmable CAS Latency, CAS Write Latency, Additive Latency, Burst Length and Burst Type.
- On-Die-Termination (ODT) and Dynamic ODT for improved signal integrity.
- Refresh. Self Refresh and Power Down Modes.
- ZQ Calibration for output driver and ODT.
- System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern.

**Figure:** mechanical dimensions[1]




[1] if no tolerances specified ± 0.15mm

This Swissbit module is an industry standard 240-pin 8-byte DDR3 SDRAM Dual-In-line Memory Module (UDIMM) which is organized as x64 high speed CMOS memory arrays. The module uses internally configured octal-bank DDR3 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR3 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR3 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR3 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving “power-down” mode. All inputs and all full drive-strength outputs are SSTL_15 compatible.
The DDR3 SDRAM module uses the serial presence detect (SPD) function implemented via serial EEPROM using the standard $I^2C$ protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the DIMM manufacturer (Swissbit) to identify the module type, the module’s organization and several timing parameters. The second 128 bytes are available to the end user.

### Module Configuration

| Organization | DDR3 SDRAMs used | Row Addr. | Device Bank Addr. | Column Addr. | Refresh | Module Bank Select |
|---|---|---|---|---|---|---|
| 128M x 64bit | 8 x 128M x 8bit (1024Mbit) | 14 | BA0, BA1, BA2 | 10 | 8k | S0# |

| Module Dimensions<br>in mm |
|---|
| 133.35 (long) x 30(high) x 2.70[max] (thickness) |

### Timing Parameters

| Part Number | Module Density | Transfer Rate | Clock Cycle/Data bit rate | Latency |
|---|---|---|---|---|
| SGU01G64A1BG1SA-BBR | 1024 MB | 8.5 GB/s | 1.87ns/1066MT/s | 7-7-7 |
| SGU01G64A1BG1SA-CCR | 1024 MB | 10.6 GB/s | 1.5ns/1333MT/s | 9-9-9 |
| SGU01G64A1BG1SA-DCR | 1024 MB | 12.8 GB/s | 1.25ns/1600MT/s | 11-11-11 |

### Pin Name

| | |
|---|---|
| A0 – A9, A11 – A13 | Address Inputs |
| A10/AP | Address Input / Autoprecharge Bit |
| BA0 – BA2 | Bank Address Inputs |
| DQ0 – DQ63 | Data Input / Output |
| DM0 – DM7 | Input Data Mask |
| DQS0 – DQS7 | Data Strobe, positive line |
| DQS0# - DQS7# | Data Strobe, negative line (only used when differential data strobe mode is enabled) |
| S0# | Chip Select |
| RAS# | Row Address Strobe |
| CAS# | Column Address Strobe |
| WE# | Write Enable |
| CKE0 | Clock Enable |

| | |
|---|---|
| ODT0 | On-Die Termination |
| CK0 | Clock Inputs, positive line |
| CK0# | Clock Inputs, negative line |
| $V_{DD}$ | Supply Voltage (1.5V± 0.075V) |
| $V_{REF}DQ$ | Reference voltage: DQ, DM ($V_{DD}/2$) |
| $V_{REF}CA$ | Reference voltage: Control, command, and address ($V_{DD}/2$) |
| $V_{SS}$ | Ground |
| $V_{TT}$ | Termination voltage: Used for control, command, and address ($V_{DD}/2$). |
| $V_{DDSPD}$ | Serial EEPROM Positive Power Supply |
| SCL | Serial Clock for Presence Detect |
| SDA | Serial Data Out for Presence Detect |
| SA0 – SA1 | Presence Detect Address Inputs |
| NC | No Connection |

## Pin Configuration

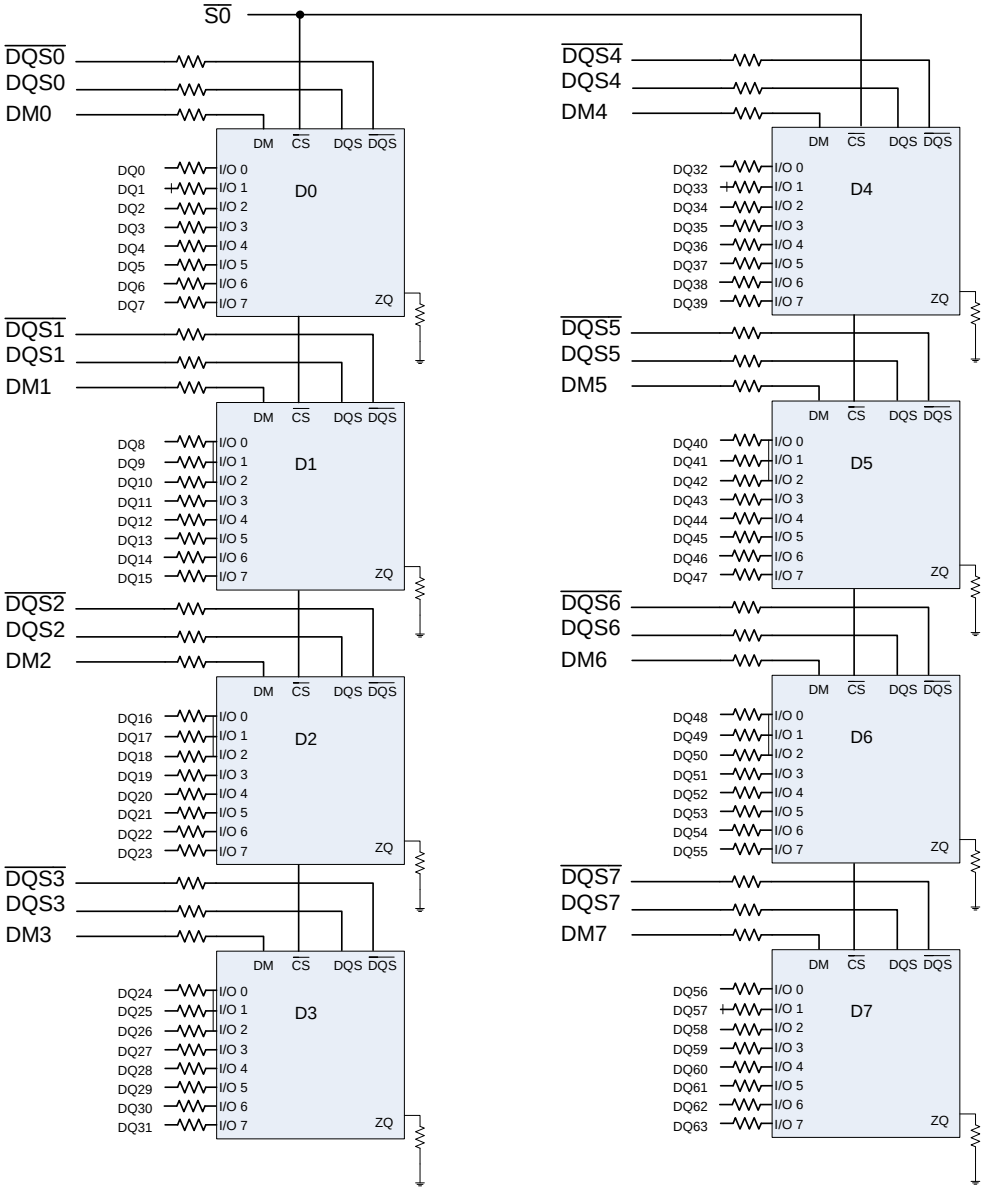
| Frontside | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **PIN** | **Symbol** | **PIN** | **Symbol** | **PIN** | **Symbol** | **PIN** | **Symbol** | **PIN** | **Symbol** |
| 1 | $V_{REF}DQ$ | 27 | DQ18 | 49 | NC($V_{TT}$) | 75 | $V_{DD}$ | 101 | $V_{SS}$ |
| 2 | $V_{SS}$ | 28 | DQ19 | 50 | CKE0 | 76 | NC(S1#) | 102 | DQS6# |
| 3 | DQ0 | 29 | $V_{SS}$ | 51 | $V_{DD}$ | 77 | NC(ODT1) | 103 | DQS6 |
| 4 | DQ1 | 30 | DQ24 | 52 | BA2 | 78 | $V_{DD}$ | 104 | $V_{SS}$ |
| 5 | $V_{SS}$ | 31 | DQ25 | 53 | NC(Err_Out#) | 79 | NC(S2#) | 105 | DQ50 |
| 6 | DQS0# | 32 | $V_{SS}$ | 54 | $V_{DD}$ | 80 | $V_{SS}$ | 106 | DQ51 |
| 7 | DQS0 | 33 | DQS3# | 55 | A11 | 81 | DQ32 | 107 | $V_{SS}$ |
| 8 | $V_{SS}$ | 34 | DQS3 | 56 | A7 | 82 | DQ33 | 108 | DQ56 |
| 9 | DQ2 | 35 | $V_{SS}$ | 57 | $V_{DD}$ | 83 | $V_{SS}$ | 109 | DQ57 |
| 10 | DQ3 | 36 | DQ26 | 58 | A5 | 84 | DQS4# | 110 | $V_{SS}$ |
| 11 | $V_{SS}$ | 37 | DQ27 | 59 | A4 | 85 | DQS4 | 111 | DQS7# |
| 12 | DQ8 | 38 | $V_{SS}$ | 60 | $V_{DD}$ | 86 | $V_{SS}$ | 112 | DQS7 |
| 13 | DQ9 | 39 | NC(CB0) | 61 | A2 | 87 | DQ34 | 113 | $V_{SS}$ |
| 14 | $V_{SS}$ | 40 | NC(CB1) | 62 | $V_{DD}$ | 88 | DQ35 | 114 | DQ58 |
| 15 | DQS1# | 41 | $V_{SS}$ | 63 | NC(CK1) | 89 | $V_{SS}$ | 115 | DQ59 |
| 16 | DQS1 | 42 | NC(DQS8#) | 64 | NC(CK1#) | 90 | DQ40 | 116 | $V_{SS}$ |
| 17 | $V_{SS}$ | 43 | NC(DQS8) | 65 | $V_{DD}$ | 91 | DQ41 | 117 | SA0 |
| 18 | DQ10 | 44 | $V_{SS}$ | 66 | $V_{DD}$ | 92 | $V_{SS}$ | 118 | SCL |
| 19 | DQ11 | 45 | NC(CB2) | 67 | $V_{REF}CA$ | 93 | DQS5# | 119 | SA2 |
| 20 | $V_{SS}$ | 46 | NC(CB3) | 68 | NC(Par_In) | 94 | DQS5 | 120 | $V_{TT}$ |
| 21 | DQ16 | 47 | $V_{SS}$ | 69 | $V_{DD}$ | 95 | $V_{SS}$ | | |
| 22 | DQ17 | 48 | NC($V_{TT}$) | 70 | A10/ AP | 96 | DQ42 | | |
| 23 | $V_{SS}$ | | | 71 | BA0 | 97 | DQ43 | | |
| 24 | DQS2# | | | 72 | $V_{DD}$ | 98 | $V_{SS}$ | | |
| 25 | DQS2 | | | 73 | WE# | 99 | DQ48 | | |
| 26 | $V_{SS}$ | | | 74 | CAS# | 100 | DQ49 | | |

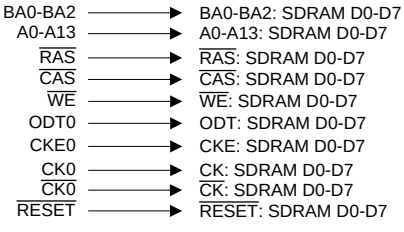
Signals in brackets (…) may be connected at the DIMM socket, but are not used on the DIMM

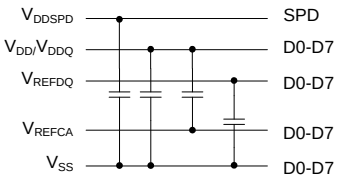
| Backside | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **PIN** | **Symbol** | **PIN** | **Symbol** | **PIN** | **Symbol** | **PIN** | **Symbol** | **PIN** | **Symbol** |
| 121 | $V_{SS}$ | 147 | DQ23 | 169 | NC(CKE1) | 195 | ODT0 | 221 | DM6(DQS15) |
| 122 | DQ4 | 148 | $V_{SS}$ | 170 | $V_{DD}$ | 196 | A13 | 222 | NC(DQS15#) |
| 123 | DQ5 | 149 | DQ28 | 171 | NC(A15) | 197 | $V_{DD}$ | 223 | $V_{SS}$ |
| 124 | $V_{SS}$ | 150 | DQ29 | 172 | NC(A14) | 198 | NC(S3#) | 224 | DQ54 |
| 125 | DM0(DQS9) | 151 | $V_{SS}$ | 173 | $V_{DD}$ | 199 | $V_{SS}$ | 225 | DQ55 |
| 126 | NC(DQS9#) | 152 | DM3(DQS12) | 174 | A12/BC# | 200 | DQ36 | 226 | $V_{SS}$ |
| 127 | $V_{SS}$ | 153 | NC(DQS12#) | 175 | A9 | 201 | DQ37 | 227 | DQ60 |
| 128 | DQ6 | 154 | $V_{SS}$ | 176 | $V_{DD}$ | 202 | $V_{SS}$ | 228 | DQ61 |
| 129 | DQ7 | 155 | DQ30 | 177 | A8 | 203 | DM4(DQS13) | 229 | $V_{SS}$ |
| 130 | $V_{SS}$ | 156 | DQ31 | 178 | A6 | 204 | NC(DQS13#) | 230 | DM7(DQS16) |
| 131 | DQ12 | 157 | $V_{SS}$ | 179 | $V_{DD}$ | 205 | $V_{SS}$ | 231 | NC(DQS16#) |
| 132 | DQ13 | 158 | NC(CB4) | 180 | A3 | 206 | DQ38 | 232 | $V_{SS}$ |
| 133 | $V_{SS}$ | 159 | NC(CB5) | 181 | A1 | 207 | DQ39 | 233 | DQ62 |
| 134 | DM1(DQS10) | 160 | $V_{SS}$ | 182 | $V_{DD}$ | 208 | $V_{SS}$ | 234 | DQ63 |
| 135 | NC(DQS10#) | 161 | DM8(DQS17) | 183 | $V_{DD}$ | 209 | DQ44 | 235 | $V_{SS}$ |
| 136 | $V_{SS}$ | 162 | NC(DQS17#) | 184 | CK0 | 210 | DQ45 | 236 | $V_{DDSPD}$ |
| 137 | DQ14 | 163 | $V_{SS}$ | 185 | CK0# | 211 | $V_{SS}$ | 237 | SA1 |
| 138 | DQ15 | 164 | NC(CB6) | 186 | $V_{DD}$ | 212 | DM5(DQS14) | 238 | SDA |
| 139 | $V_{SS}$ | 165 | NC(CB7) | 187 | NC(EVENT#) | 213 | NC(DQS14#) | 239 | $V_{SS}$ |
| 140 | DQ20 | 166 | $V_{SS}$ | 188 | A0 | 214 | $V_{SS}$ | 240 | $V_{TT}$ |
| 141 | DQ21 | 167 | NC(TEST) | 189 | $V_{DD}$ | 215 | DQ46 | | |
| 142 | $V_{SS}$ | 168 | RESET# | 190 | BA1 | 216 | DQ47 | | |
| 143 | DM2(DQS11) | | | 191 | $V_{DD}$ | 217 | $V_{SS}$ | | |
| 144 | NC(DQS11#) | | | 192 | RAS# | 218 | DQ52 | | |
| 145 | $V_{SS}$ | | | 193 | S0# | 219 | DQ53 | | |
| 146 | DQ22 | | | 194 | $V_{DD}$ | 220 | $V_{SS}$ | | |

Signals in brackets (…) may be connected at the DIMM socket, but are not used on the DIMM

## FUNCTIONAL BLOCK DIAGRAMM 1024MB DDR3 SDRAM DIMM, 1 RANK AND 8 COMPONENTS




Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/$\overline{DQS}$/ODT/DM/CKE/$\overline{S}$ relationship must be maintained as shown.
3. DQ, DM, DQS/$\overline{DQS}$ resistors: Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of the JEDED document.
5. For each DRAM, a unique ZQ resistor is connected to GND. The ZQ resistor is 240Ω±1%.
6. Refer to associated figure for SPD details.

## MAXIMUM ELECTRICAL DC CHARACTERISTICS

| PARAMETER/ CONDITION | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.4 | 1.975 | V |
| I/O Supply Voltage | $V_{DDQ}$ | -0.4 | 1.975 | V |
| $V_{DDL}$ Supply Voltage | $V_{DDL}$ | -0.4 | 1.975 | V |
| Voltage on any pin relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -0.4 | 1.975 | V |
| INPUT LEAKAGE CURRENT<br>Any input 0V ≤ $V_{IN}$ ≤ $V_{DD}$, $V_{REF}$ pin 0V ≤ $V_{IN}$ ≤ 0.95V<br>(All other pins not under test = 0V) | $I_I$ | | | µA |
| Command/Address<br>RAS#, CAS#, WE#, S#, CKE | | -16 | 16 | |
| CK, CK# | | -16 | 16 | |
| DM | | -2 | 2 | |
| OUTPUT LEAKAGE CURRENT<br>(DQ's and ODT are disabled; 0V ≤ $V_{OUT}$ ≤ $V_{DDQ}$) | $I_{OZ}$ | -5 | 5 | µA |
| DQ, DQS, DQS# | | | | |
| $V_{REF}$ LEAKAGE CURRENT ; $V_{REF}$ is on a valid level | $I_{VREF}$ | -8 | 8 | µA |

## DC OPERATING CONDITIONS

| PARAMETER/ CONDITION | SYMBOL | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 1.425 | 1.5 | 1.575 | V |
| I/O Supply Voltage | $V_{DDQ}$ | 1.425 | 1.5 | 1.575 | V |
| $V_{DDL}$ Supply Voltage | $V_{DDL}$ | 1.425 | 1.5 | 1.575 | V |
| I/O Reference Voltage | $V_{REF}$ | 0.49 x $V_{DDQ}$ | 0.50 x $V_{DDQ}$ | 0.51x $V_{DDQ}$ | V |
| I/O Termination Voltage (system) | $V_{TT}$ | 0.49 x $V_{DDQ}$-20mV | 0.50 x $V_{DDQ}$ | 0.51x $V_{DDQ}$+20mV | V |
| Input High (Logic 1) Voltage | $V_{IH\ (DC)}$ | $V_{REF}$ + 0.1 | | $V_{DDQ}$ + 0.3 | V |
| Input Low (Logic 0) Voltage | $V_{IL\ (DC)}$ | -0.3 | | $V_{REF}$ – 0.1 | V |

## AC INPUT OPERATING CONDITIONS

| PARAMETER/ CONDITION | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| Input High (Logic 1) Voltage | $V_{IH\ (AC)}$ | $V_{REF}$ + 0.175 | - | V |
| Input Low (Logic 0) Voltage | $V_{IL\ (AC)}$ | - | $V_{REF}$ - 0.175 | V |

## CAPACITANCE

At DDR3 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

## $I_{DD}$ Specifications and Conditions

(0°C ≤ $T_{CASE}$ ≤ + 85°C°, $V_{DDQ}$ = +1.5V ± 0.075V, $V_{DD}$ = +1.5V ± 0.075V)

| Parameter & Test Condition | | Symbol | max. | | | Unit |
|---|---|---|---|---|---|---|
| | | | 12800-CL11 | 10600-CL9 | 8500-CL7 | |
| **OPERATING CURRENT *) :** One device bank Active-Precharge; $t_{RC}$= $t_{RC}$ ($I_{DD}$); $t_{CK}$ = $t_{CK}$ ($I_{DD}$); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles | | $I_{DD0}$ | 280 | 280 | 280 | mA |
| **OPERATING CURRENT *) :** One device bank; Active-Read-Precharge; $I_{OUT}$ = 0mA; BL = 4, CL = CL ($I_{DD}$), AL = 0; $t_{CK}$ = $t_{CK}$ ($I_{DD}$), $t_{RC}$= $t_{RC}$ ($I_{DD}$), $t_{RAS}$ = $t_{RAS}$ MIN ($I_{DD}$), $t_{RCD}$ = $t_{RCD}$ ($I_{DD}$); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as $I_{DD4W}$ | | $I_{DD1}$ | 360 | 336 | 320 | mA |
| **PRECHARGE POWER-DOWN CURRENT:** All device banks idle; Power-down mode; $t_{CK}$ = $t_{CK}$ ($I_{DD}$); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at $V_{REF}$ | Fast Exit | $I_{DD2P}$ | 96 | 96 | 96 | mA |
| | Slow Exit | | 80 | 80 | 80 | |
| **PRECHARGE QUIET STANDBY CURRENT:** All device banks idle; $t_{CK}$ = $t_{CK}$ ($I_{DD}$); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at $V_{REF}$ | | $I_{DD2Q}$ | 120 | 120 | 120 | mA |
| **PRECHARGE STANDBY CURRENT:** All device banks idle; $t_{CK}$ = $t_{CK}$ ($I_{DD}$); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle | | $I_{DD2N}$ | 120 | 120 | 120 | mA |
| **ACTIVE POWER-DOWN CURRENT:** All device banks open; $t_{CK}$ = $t_{CK}$ ($I_{DD}$); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at $V_{REF}$ (always fast exit) | | $I_{DD3P}$ | 120 | 120 | 120 | mA |
| **ACTIVE STANDBY CURRENT:** All device banks open; $t_{CK}$ = $t_{CK}$ ($I_{DD}$), $t_{RAS}$ = $t_{RAS}$ MAX ($I_{DD}$), $t_{RP}$ = $t_{RP}$ ($I_{DD}$); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle | | $I_{DD3N}$ | 160 | 160 | 160 | mA |
| **OPERATING READ CURRENT:** All device banks open, Continuous burst reads; One module rank active; $I_{OUT}$ = 0mA; BL = 4, CL = CL ($I_{DD}$), AL = 0; $t_{CK}$ = $t_{CK}$ ($I_{DD}$), $t_{RAS}$ = $t_{RAS}$ MAX ($I_{DD}$), $t_{RP}$ = $t_{RP}$ ($I_{DD}$); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle | | $I_{DD4R}$ | 600 | 520 | 440 | mA |

| Parameter & Test Condition | Symbol | max. | | | Unit |
|---|---|---|---|---|---|
| | | 12800-CL11 | 10600-CL9 | 8500-CL7 | |
| **OPERATING WRITE CURRENT:** All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL ($I_{DD}$), AL = 0; $t_{CK} = t_{CK}$ ($I_{DD}$), $t_{RAS} = t_{RAS}$ MAX ($I_{DD}$), $t_{RP} = t_{RP}$ ($I_{DD}$); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle | $I_{DD4W}$ | 640 | 560 | 480 | mA |
| **BURST REFRESH CURRENT:** $t_{CK} = t_{CK}$ ($I_{DD}$); refresh command at every $t_{RFC}$ ($I_{DD}$) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle | $I_{DD5}$ | 720 | 720 | 680 | mA |
| **SELF REFRESH CURRENT:** CK and CK# at 0V; CKE $\leq 0.2V$; All other Control and Address bus inputs are floating at $V_{REF}$; DQ's are floating at $V_{REF}$ | $I_{DD6}$ | 80 | 80 | 80 | mA |
| **OPERATING CURRENT*) :** Four device bank interleaving READs, $I_{OUT}$ = 0mA; BL = 4, CL = CL ($I_{DD}$), AL = $t_{RCD}$ ($I_{DD}$) – 1 x $t_{CK}$ ($I_{DD}$); $t_{CK} = t_{CK}$ ($I_{DD}$), $t_{RC} = t_{RC}$ ($I_{DD}$), $t_{RRD} = t_{RRD}$ ($I_{DD}$), $t_{RCD} = t_{RCD}$ ($I_{DD}$); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle | $I_{DD7}$ | 1024 | 1000 | 800 | mA |

***) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.**

## TIMING VALUES USED FOR $I_{DD}$ MEASUREMENT

| | $I_{DD}$ MEASUREMENT CONDITIONS | | | |
|---|---|---|---|---|
| **SYMBOL** | **12800-CL11** | **10600-CL9** | **8500-CL7** | **Unit** |
| CL ($I_{DD}$) | 11 | 9 | 7 | $t_{CK}$ |
| $t_{RCD}$ ($I_{DD}$) | 13.75 | 13.5 | 13.125 | ns |
| $t_{RC}$ ($I_{DD}$) | 48.75 | 49.5 | 50.625 | ns |
| $t_{RRD}$ ($I_{DD}$) | 6.25 | 6 | 7.5 | ns |
| $t_{CK}$ ($I_{DD}$) | 1.25 | 1.5 | 1.87 | ns |
| $t_{RAS}$ MIN ($I_{DD}$) | 35 | 36 | 37.5 | ns |
| $t_{RAS}$ MAX ($I_{DD}$) | 70'200 | 70'200 | 70'200 | ns |
| $t_{RP}$ ($I_{DD}$) | 13.75 | 13.5 | 13.125 | ns |
| $t_{RFC}$ ($I_{DD}$) | 110 | 110 | 110 | ns |

## DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ $T_{CASE}$ ≤ + 85°C°, $V_{DDQ}$ = +1.5V ± 0.075V, $V_{DD}$ = +1.5V ± 0.075V)

| AC CHARACTERISTICS | | | 12800-CL11 | | 10600-CL9 | | 8500-CL7 | | |
|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | | SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | Unit |
| Clock cycle time | CL = 11 | $t_{CK}$ (11) | 1.25 | 1.5 | - | - | - | - | ns |
| | CL = 10 | $t_{CK}$ (10) | 1.5 | <1.875 | 1.5 | <1.875 | - | - | |
| | CL = 9 | $t_{CK}$ (9) | 1.5 | <1.875 | 1.5 | <1.875 | - | - | |
| | CL = 8 | $t_{CK}$ (8) | 1.875 | <2.5 | 1.875 | <2.5 | - | - | |
| | CL = 7 | $t_{CK}$ (7) | 1.875 | <2.5 | 1.875 | <2.5 | 1.875 | <2.5 | |
| | CL = 6 | $t_{CK}$ (6) | 2.5 | 3.3 | 2.5 | 3.3 | 2.5 | 3.3 | |
| | CL = 5 | $t_{CK}$ (5) | 3.0 | 3.3 | 3.0 | 3.3 | 3.0 | 3.3 | |
| Read CMD to 1st data | | $t_{AA}$ | 13.75 | - | 13.5 | - | 13.125 | - | |
| CK high-level width | | $t_{CH}$ | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | $t_{CK}$ |
| CK low-level width | | $t_{CL}$ | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | $t_{CK}$ |
| Data-out high-impedance window from CK/CK# | | $t_{HZ}$ | - | 225 | - | 0.25 | - | 0.3 | ns |
| Data-out low-impedance window from CK/CK# | | $t_{LZ}$ | -450 | 225 | -0.5 | 0.25 | -0.6 | 0.3 | ns |
| DQ and DM input setup time relative to DQS | | $t_{DS(Base)}$ | - | - | 30 | - | 25 | - | ps |
| DQ and DM input hold time relative to DQS | | $t_{DH(Base)}$ | - | - | 65 | - | 100 | - | ps |
| DQ and DM input setup time relative to DQS $V_{REF}$=1V/ns | | $t_{DS1V}$ | 160 | - | 180 | - | 200 | - | ps |
| DQ and DM input hold time relative to DQS $V_{REF}$=1V/ns | | $t_{DH1V}$ | 145 | - | 165 | - | 200 | - | ps |
| DQ and DM input pulse width ( for each input ) | | $t_{DIPW}$ | 360 | - | 0.4 | - | 0.49 | - | ns |
| DQS, DQS# to DQ skew, per access | | $t_{DQSQ}$ | - | 100 | - | 125 | - | 150 | ps |
| DQ-DQS hold, DQS to first DQ to go non-valid, per access | | $t_{QH}$ | 0.38 | - | 0.38 | - | 0.38 | - | $t_{CK}$ (AVG) |
| DQS input high pulse width | | $t_{DQSH}$ | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ |
| DQS input low pulse width | | $t_{DQSL}$ | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ |
| DQS, DQS# rising to/from CK, CK# | | $t_{DQSCK}$ | -225 | 225 | -255 | +255 | -300 | 300 | ps |
| DQS, DQS# rising to/from CK, CK# when DLL disabled | | $t_{DQSCK\ DLL\_DIS}$ | 1 | 10 | 1 | 10 | 1 | 10 | ns |
| DQS falling edge to CK rising - setup time | | $t_{DSS}$ | 0.18 | - | 0.2 | - | 0.2 | - | $t_{CK}$ |
| DQS falling edge from CK rising - hold time | | $t_{DSH}$ | 0.18 | - | 0.2 | - | 0.2 | - | $t_{CK}$ |
| DQS read preamble | | $t_{RPRE}$ | 0.9 | Note1 | 0.9 | Note1 | 0.9 | Note1 | $t_{CK}$ |
| DQS read postamble | | $t_{RPST}$ | 0.3 | Note2 | 0.3 | Note2 | 0.3 | Note2 | $t_{CK}$ |
| DQS write preamble | | $t_{WPRE}$ | 0.9 | - | 0.9 | - | 0.9 | - | $t_{CK}$ |
| DQS write postamble | | $t_{WPST}$ | 0.3 | - | 0.3 | - | 0.3 | - | $t_{CK}$ |
| Positive DQS latching edge to associated clock edge | | $t_{DQSS}$ | - 0.27 | + 0.27 | - 0.25 | + 0.25 | - 0.25 | + 0.25 | $t_{CK}$ |
| Address and control input pulse width ( for each input ) | | $t_{IPW}$ | 560 | - | 620 | - | 780 | - | ps |
| CTRL, CMD, Addr setup to CK, CK# | | $t_{IS(Base)}$ | 45 | - | 65 | - | 125 | - | ps |
| CTRL, CMD, Addr setup to CK, CK# $V_{REF}$ @ 1V/ns | | $t_{IS(1V)}$ | 220 | - | 240 | - | 300 | - | ps |

1 The maximum preamble is bound by tLZDQS (MAX)

2 The maximum postamble is bound by tHZDQS (MAX)

## DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ $T_{CASE}$ ≤ + 85°C ; $V_{DDQ}$ = +1.5V ± 0.075V, $V_{DD}$ = +1.5V ± 0.075V)

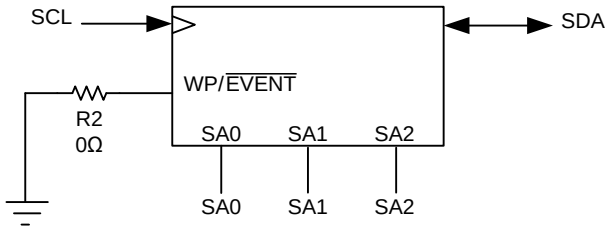
| AC CHARACTERISTICS | | | 12800-CL11 | | 10600-CL9 | | 8500-CL7 | | |
|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | | SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | Unit |
| CTRL, CMD, Addr hold to CK, CK# | | $t_{IH(Base)}$ | 120 | - | 140 | - | 200 | - | ps |
| CTRL, CMD, Addr hold to CK, CK# $V_{REF}$ @ 1V/ns | | $t_{IH(1V)}$ | 220 | - | 240 | - | 300 | - | ps |
| CAS# to CAS# command delay | | $t_{CCD}$ | 4 | - | 4 | - | 4 | - | $t_{CK}$ |
| ACTIVE to ACTIVE (same bank) command period | | $t_{RC}$ | 48.75 | - | 49.5 | - | 50.625 | - | ns |
| ACTIVE bank *a* to ACTIVE bank *b* command | | $t_{RRD}$ | max 4nCK,6ns | - | max 4nCK,7.5ns | - | max 4nCK,7.5ns | - | ns |
| ACTIVE to READ or WRITE delay | | $t_{RCD}$ | 13.75 | - | 13.5 | - | 13.125 | - | ns |
| Four bank Activate period | 1K Page size | $t_{FAW}$ | 30 | - | 30 | - | 37.5 | - | ns |
| | 2K Page size | | 40 | - | 45 | - | 50 | - | |
| ACTIVE to PRECHARGE command | | $t_{RAS}$ | 35 | 70’200 | 36 | 70’200 | 37.5 | 70’200 | ns |
| Internal READ to precharge command delay | | $t_{RTP}$ | max 4nCK,7.5ns | - | max 4nCK,7.5ns | - | max 4nCK,7.5ns | - | ns |
| Write recovery time | | $t_{WR}$ | 15 | - | 15 | - | 15 | - | ns |
| Auto precharge write recovery + precharge time | | $t_{DAL}$ | $t_{WR}$ + $t_{RP}/t_{CK}$ | - | $t_{WR}$ + $t_{RP}/t_{CK}$ | - | $t_{WR}$ + $t_{RP}/t_{CK}$ | - | ns |
| Internal WRITE to READ command delay | | $t_{WTR}$ | max 4nCK,7.5ns | - | max 4nCK,7.5ns | - | max 4nCK,7.5ns | - | ns |
| PRECHARGE command period | | $t_{RP}$ | 13.75 | - | 13.5 | - | 13.125 | - | ns |
| LOAD MODE command cycle time | | $t_{MRD}$ | 4 | - | 4 | - | 4 | - | $t_{CK}$ |
| REFRESH to ACTIVE or REFRESH to REFRESH command interval | | $t_{RFC}$ | 110 | 70’200 | 110 | 70’200 | 110 | 70’200 | ns |
| Average periodic refresh interval 0 °C ≤ $T_{CASE}$ ≤ 85°C | | $t_{REFI}$ | - | 7.8 | - | 7.8 | - | 7.8 | µs |
| 85 °C < $T_{CASE}$ ≤ 95°C | | $t_{REFI\,IT}$ | - | 3.9 | - | 3.9 | - | 3.9 | |
| RTT turn-on from ODTL on reference | | $t_{AON}$ | -225 | 225 | -250 | 250 | -300 | 300 | ps |
| RTT turn-on from ODTL off reference | | $t_{AOF}$ | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | $t_{CK}$ |
| Asynchronous RTT turn-on delay (power Down with DLL off) | | $t_{AONPD}$ | 2 | 8,5 | 1 | 9 | 1 | 9 | ns |
| Asynchronous RTT turn-off delay (power Down with DLL off) | | $t_{AOFPD}$ | 2 | 8,5 | 1 | 9 | 1 | 9 | ns |
| RTT dynamic change skew | | $t_{ADC}$ | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | $t_{CK}$ |
| Exit self refresh to commands not requiring a locked DLL | | $t_{XS}$ | max 5nCK,tR FC + 10ns | - | max 5nCK,tR FC + 10ns | - | max 5nCK,tR FC + 10ns | - | ns |
| Write levelling setup from rising CK, CK# crossing to rising DQS, DQS# crossing | | $t_{WLS}$ | 165 | - | 195 | - | 245 | - | ps |
| Write levelling setup from rising DQS, DQS# crossing to rising CK, CK# crossing | | $t_{WLH}$ | 165 | - | 195 | - | 245 | - | ps |
| First DQS, DQS# rising edge | | $t_{WLMRD}$ | 40 | - | 40 | - | 40 | - | $t_{CK}$ |
| DQS, DQS# delay | | $t_{WLDQSEN}$ | 25 | - | 25 | - | 25 | - | $t_{CK}$ |

**DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)**

(0°C ≤ $T_{CASE}$ ≤ + 85°C ; $V_{DDQ}$ = +1.5V ± 0.075V, $V_{DD}$ = +1.5V ± 0.075V)

| AC CHARACTERISTICS | | 12800-CL11 | | 10600-CL9 | | 8500-CL7 | | |
|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **Unit** |
| Exit reset from CKE HIGH to a valid command | $t_{XPR}$ | max 5nCK, $t_{RFC}$ + 10ns | - | max 5nCK, $t_{RFC}$ + 10ns | - | max 5nCK, $t_{RFC}$ + 10ns | - | $t_{CK}$ |
| Begin power supply ramp to power supplies stable | $t_{VDDPR}$ | - | 200 | - | 200 | - | 200 | ms |
| RESET# LOW to power supplies stable | $t_{RPS}$ | - | 200 | - | 200 | - | 200 | ms |
| RESET# LOW to I/O and RTT High-Z | $t_{IOz}$ | - | 20 | - | 20 | - | 20 | ns |
| Exit precharge power-down to any non-READ command | $t_{XP}$ | max 3nCK,6ns | - | max 3nCK,6ns | - | max 3nCK,7.5ns | - | $t_{CK}$ |
| CKE minimum high/low time | $t_{CKE}$ | max 3nCK, 5ns | - | max 3nCK, 5.625ns | - | max 3nCK, 5.625ns | - | $t_{CK}$ |

## Serial Presence-Detect EEPROM

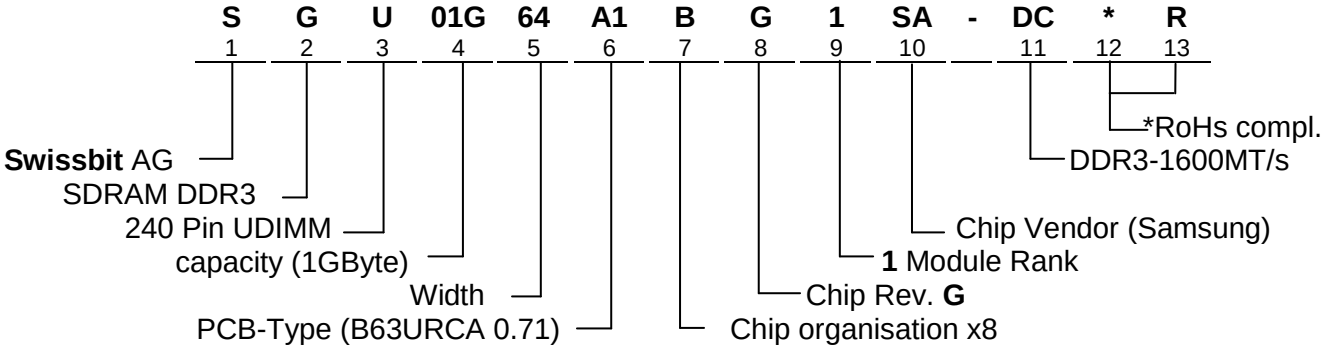


## SERIAL PRESENCE-DETECT MATRIX

| Byte | Byte Description | 12800-CL11 | 10600-CL9 | 8500-CL7 |
|---|---|---|---|---|
| 0 | CRC RANGE, EEPROM BYTES, BYTES USED | 0x92 | | |
| 1 | SPD REVISON | 0x11 | 0x10 | |
| 2 | DRAM DEVICE TYPE | 0x0B | | |
| 3 | MODULE TYPE (FORM FACTOR) | 0x02 | | |
| 4 | SDRAM DEVICE DENSITY & BANKS | 0x02 | | |
| 5 | SDRAM DEVICE ROW & COLUMN COUNT | 0x11 | | |
| 6 | BYTE 6 RESERVED | 0x00 | | |
| 7 | MODULE RANKS & DEVICE DQ COUNT | 0x01 | | |
| 8 | ECC TAG & MODULE MEMORY BUS WIDTH | 0x03 | | |
| 9 | FINE TIMEBASE DIVIDEND/DIVISOR | 0x11 | 0x52 | |
| 10 | MEDIUM TIMEBASE DIVIDEND | 0x01 | | |
| 11 | MEDIUM TIMEBASE DIVISOR | 0x08 | | |
| 12 | MIN SDRAM CYCLE TIME ($t_{CK\ MIN}$) | 0x0A | 0x0C | 0x0F |
| 13 | BYTE 13 RESERVED | 0x00 | | |
| 14 | CAS LATENCIES SUPPORTED (CL4 => CL11) | 0xFE | 0x3C | 0x1C |
| 15 | CAS LATENCIES SUPPORTED (CL12 => CL18) | 0x00 | | |
| 16 | MIN CAS LATENCY TIME ($t_{AA\ MIN}$) | 0x69 | | |
| 17 | MIN WRITE RECOVERY TIME ($t_{WR\ MIN}$) | 0x78 | | |
| 18 | MIN RAS# TO CAS# DELAY ($t_{RCD\ MIN}$) | 0x69 | | |
| 19 | MIN ROW ACTIVE TO ROW ACTIVE DELAY ($t_{RRD\ MIN}$) | 0x30 | | 0x3C |
| 20 | MIN ROW PRECHARGE DELAY ($t_{RP\ MIN}$) | 0x69 | | |
| 21 | UPPER NIBBLE FOR $t_{RAS}$ & $t_{RC}$ | 0x11 | | |
| 22 | MIN ACTIVE TO PRECHARGE DELAY ($t_{RAS\ MIN}$) | 0x18 | 0x20 | 0x2C |
| 23 | MIN ACTIVE TO ACTIVE/REFRESH DELAY ($t_{RC\ MIN}$) | 0x81 | 0x89 | 0x95 |
| 24 | MIN REFRESH RECOVERY DELAY ($t_{RFC\ MIN}$) LSB | 0x70 | | |
| 25 | MIN REFRESH RECOVERY DELAY ($t_{RFC\ MIN}$) MSB | 0x03 | | |
| 26 | MIN INTERNAL WRITE TO READ CMD DELAY ($t_{WTR\ MIN}$) | 0x3C | | |
| 27 | MIN INTERNAL READ TO PRECHARGE CMD DELAY ($t_{RTP\ MIN}$) | 0x3C | | |
| 28 | MIN FOUR ACTIVE WINDOW DELAY ($t_{FAW\ MIN}$) MSB | 0x00 | | 0x01 |
| 29 | MIN FOUR ACTIVE WINDOW DELAY ($t_{FAW\ MIN}$) LSB | 0xF0 | | 0x2C |
| 30 | SDRAM DEVICE OUTPUT DRIVERS SUPPORTED | 0x83 | | |
| 31 | SDRAM DEVICE THERMAL & REFRESH OPTIONS | 0x01 | | |

| Byte | Byte Description | 12800-CL11 | 10600-CL9 | 8500-CL7 |
|---|---|---|---|---|
| 32-59 | BYTES 32-59 RESERVED | 0x00 | | |
| 60 | MODULE HEIGHT (NOMINAL) | 0x0F | | |
| 61 | MODULE THICKNESS (MAX) | 0x01 | | |
| 62 | REFERENCE RAW CARD ID | 0x00 | | |
| 63 | ADDRESS MAPPING EDGE CONECTOR TO DRAM | 0x00 | | |
| 64-116 | BYTES 64-116 RESEVED | 0x00 | | |
| 117 | MODULE MFR ID (LSB) | 0x83 | | |
| 118 | MODULE MFR ID (MSB) | 0xDA | | |
| 119 | MODULE MFR LOCATION ID | 0x01 (Switzerland)<br>0x02 (Germany)<br>0x03 (USA) | | |
| 120 | MODULE MFR YEAR | X | | |
| 121 | MODULE MFR WEEK | X | | |
| 122-125 | MODULE SERIAL NUMBER | X | | |
| 126-127 | CRC | 0xF431 | 0x1FA5 | 0x5D0C |
| 128-145 | MODULE PART NUMBER | "SGU01G64A1BG1SA-xx" | | |
| 146 | MODULE DIE REV | X | | |
| 147 | MODULE PCB REV | X | | |
| 148 | DRAM DEVICE MFR ID (LSB) | 0x80 | | |
| 149 | DRAM DEVICE MFR (MSB) | 0x2C | | |
| 150-175 | MFR RESERVED BYTES 150-175 | 0x00 | | |
| 176-255 | CUSTOMER RESERVED BYTES 176-255 | 0xFF | | |

## Part Number Code




* optional / additional information

| Revision History | | |
|---|---|---|
| Revision | Changes | Date |
| 1.0 | Initial Revision | 14.01.2011 |
| 1.1 | New Speed-Grade added (DDR3 1600MT/s)<br>Extendet Temperature-Grade added (E- and W-Grade) | 11.04.2013 |
| | | |

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# CE Declaration of Conformity

We

**Manufacturer:** **Swissbit AG**
**Industriestrasse 4**
**CH-9552 Bronschhofen**
**Switzerland**

declare under our sole responsibility that the product

**Product Type:** **1GB DDR3 UDIMM**
**Brand Name:** **SWISSMEMORY™**
**Product Series:** **DDR3 UDIMM**
**Part Number:** **SGU01G64A1BG1SA-xxxR**

to which this declaration relates is in conformity with the following directives:

**2002/96/EC Category 3 (WEEE)**

following the provisions of Directive

**Restriction of the use of certain hazardous substances**
**2011/65/EU**

Swissbit AG, April 2013

Manuela Kögel
Head of Quality Management