19-0548; Rev 0; 5/06

HDTV Continuously Variable Anti-Aliasing Filters

General Description

The MAX7469/MAX7470 triple-channel, anti-aliasing filters and buffers are ideal for high-definition (HD) and standard-definition (SD) television (TV) applications. Compatible with 1080i, 720p, 720i, 480p, and 480i scanning system standards and computer format signals, the MAX7469/MAX7470 support component video (Y P_b P_r, G_SBR, and RGBHV), as well as composite (CVBS) and S-video (Y/C).

The MAX7469/MAX7470 limit the input bandwidth for anti-aliasing and out-of-band noise reduction prior to digital conversion by an ADC or video decoder. The MAX7469/MAX7470 frequency response can be continuously varied in 256 linear steps through an I²C* interface from below SD resolution to beyond HD resolution.

The output buffers of the MAX7469/MAX7470 drive a $2V_{P-P}$ video signal into a standard 150Ω load. The inputs are AC-coupled, and the outputs can be either DC- or AC-coupled. The MAX7469 has a gain of 0dB, and the MAX7470 has a gain of +6dB. Both devices are available in a 20-pin TQFN package and are fully specified over the 0°C to +85°C upper-commercial temperature range.

Applications

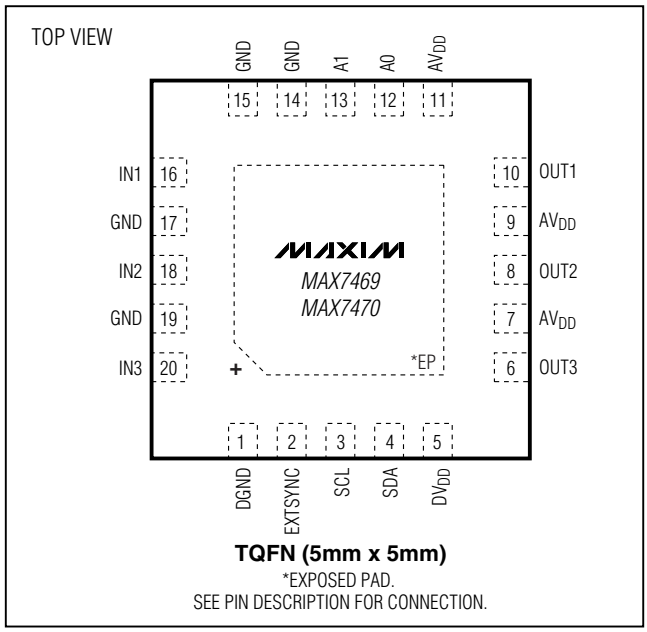
HDTV (LCD, PDP, DLP, CRT)

Set-Top Boxes

Personal Video Recorders

Home Theaters

Pin Configuration



TQFN (5mm x 5mm)

*EXPOSED PAD.
SEE PIN DESCRIPTION FOR CONNECTION.

Features

- **Continuously Variable Anti-Aliasing Filter**
  5MHz to 34MHz in 256 Steps
- **Supports All Standard Video and Computer Input Formats**
  480i, 480p, 720i, 720p, 1080i
  QVGA, VGA, SVGA, XGA, SXGA, UXGA
  Y P_b P_r, G_SBR, RGBHV, Y/C, CVBS
- **Accepts Any Input Sync Format**
  Sync on Y, Sync on G, External Sync (Positive or Negative)
  Sync on All Channels
- **Buffered Outputs Drive Standard 150Ω Video Load**
  0dB (MAX7469)
  +6dB (MAX7470)
- **DC- or AC-Coupled Outputs**
- **Single +5V Analog and +3.3V Digital Supplies**
- **5mW Power-Down Mode**
- **20-Pin TQFN Lead-Free Package**

**Purchase of I²C components from Maxim Integrated Products, Inc., or one of its sublicensed Associate Companies, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification defined by Philips.*

Ordering Information

PART	PIN-PACKAGE	BUFFER GAIN (dB)	PKG CODE
MAX7469UTP+	20 TQFN-EP*	0	T2055-4
MAX7470UTP+**	20 TQFN-EP*	+6	T2055-4

Note: *All devices are specified over the 0°C to +85°C operating temperature range.*
+ Indicates lead-free packaging.
**EP = Exposed pad.*
***Future product—contact factory for availability.*

Typical Operating Circuit appears at end of data sheet.

HDTV Continuously Variable Anti-Aliasing Filters

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to GND.....-0.3V to +6V
DV_{DD} to DGND.....-0.3V to +4V
IN_, EXTSYNC to GND .....
.....-0.3V to the lower of (AV_{DD} + 3V) and +6V
OUT_ to GND .....
.....-0.3V to the lower of (AV_{DD} + 3V) and +6V
A_ to GND .....
.....-0.3V to the lower of (AV_{DD} + 3V) and +6V
SCL, SDA to DGND .....-0.3V to +6V

Continuous Power Dissipation (T_A = +70°C)
20-Pin TQFN (derate 33.3mW/°C above +70°C) ...2666.7mW
Maximum Current into IN_, A_, GND,
SCL, SDA, and EXTSYNC.....±50mA
Operating Temperature Range.....0°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = +5V ±5%, DV_{DD} = 2.7V to 3.6V, R_{LOAD} = 150Ω to GND, C_{IN} = 0.1µF, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at AV_{DD} = 5V, DV_{DD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Filter Passband Response	A_{PB}	HD: f = 100kHz to 30MHz, relative to 100kHz (Note 1)	-3	-0.6	+1	dB
		SD: f = 100kHz to 5.75MHz, relative to 100kHz (Note 2)		±0.1	±1.0	
Filter Stopband Attenuation	A_{SB}	HD: f = 74MHz (Note 1)	45	57		dB
		SD: f = 27MHz (Note 2)	52	63		
Group Delay Deviation	Δt_G	HD: 100kHz to 30MHz, relative to 100kHz (Note 1)		20		ns
		SD: 100kHz to 5.75MHz, relative to 100kHz (Note 2)		15		
Group Delay Matching	$t_{G(MATCH)}$	HD: channel to channel, 100kHz to 2MHz, (Note 1)		5		ns
		SD: channel to channel, 100kHz to 500kHz, (Note 2)		1.5		
Bypass Frequency Response		-3dB, bypass mode, independent of filter setting		100		MHz
SD Differential Gain	dG	Five-step modulated staircase (Note 2)		0.25		%
SD Differential Phase	dϕ	Five-step modulated staircase (Note 2)		0.25		Degrees
Signal-to-Noise Ratio	SNR	Output signal ($2V_{P-P}$) to RMS noise (100kHz to 30MHz), f = 30MHz		69		dB
SD Line-Time Distortion	H_{DIST}	Deviations in a line with an 18µs, 100 IRE bar; 1 line = 63.5µs (Note 2)			0.3	%
SD Field-Time Distortion	V_{DIST}	Deviations in 130 lines with 18µs, 100 IRE bars (Note 2)			0.3	%

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = +5V ±5%, DV_{DD} = 2.7V to 3.6V, R_{LOAD} = 150Ω to GND, C_{IN} = 0.1µF, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at AV_{DD} = 5V, DV_{DD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Clamp Settling Time		To 1% with 100 IRE step (Note 4)	Positive		350		H
			Negative		650		
Minimum Functional Input Sync Amplitude				125			mV
Low-Frequency Gain (Note 1)		MAX7469		-0.5	0	+0.5	dB
		MAX7470		5.5	6	6.5	
Low-Frequency Gain Matching		100kHz			0.05		dB
Maximum Output Voltage Amplitude		DC to 30MHz			2.4		V_{P-P}
Maximum Input Voltage Amplitude		MAX7469			2.4		V_{P-P}
		MAX7470			1.2		
Channel-to-Channel Isolation					62		dB
Output Clamping Level Variation		(Notes 1, 4)				±100	mV
Power-Supply Rejection Ratio	PSRR	DC			50		dB
DIGITAL INPUTS (EXTSYNC, A1, A0)							
Input Logic-High Voltage	V_{IH}			2.0			V
Input Logic-Low Voltage	V_{IL}					0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0 to DV_{DD}			±1	±10	µA
Input Capacitance	C_{IN}				6		pF
DIGITAL INPUTS (SDA, SCL)							
Input Logic-High Voltage	V_{IH}			0.7 x DV_{DD}			V
Input Logic-Low Voltage	V_{IL}					0.3 x DV_{DD}	V
Input Hysteresis	V_{HYST}			0.05 x DV_{DD}			V
Input Leakage Current	I_{IN}	V_{IN} = 0 to DV_{DD}			±0.1	±10	µA
Input Capacitance	C_{IN}				6		pF
DIGITAL OUTPUT (SDA)							
Output Logic-Low Voltage	V_{OL}	I_{SINK} = 3mA				0.4	V
Tri-State Leakage Current	I_L	V_{IN} = 0 to DV_{DD}			±0.1	±10	µA
Tri-State Output Capacitance	C_{OUT}				6		pF
POWER REQUIREMENTS							
Analog Supply Voltage Range	AV_{DD}			4.75	5	5.25	V
Digital Supply Voltage Range	DV_{DD}			2.7	3.3	3.6	V
Analog Supply Current	I_{AVDD}	Normal operation, no load			180	200	mA
		Power-down mode, no load			1	1.5	
Digital Supply Current	I_{DVDD}	f_{SCL} = 400kHz			25		µA

HDTV Continuously Variable Anti-Aliasing Filters

TIMING CHARACTERISTICS

(AV_{DD} = +5V ±5%, DV_{DD} = 2.7V to 3.6V, R_{LOAD} = 150Ω to GND, C_{IN} = 0.1µF, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at AV_{DD} = 5V, DV_{DD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP (P) and START (S) Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START (Sr) Condition	$t_{HD;STA}$	After this period, the first clock pulse is generated	0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START (Sr) Condition	$t_{SU;STA}$		0.6			µs
Data Hold Time	$t_{HD;DAT}$	(Note 5)	0.0		0.9	µs
Data Setup Time	$t_{SU;DAT}$		100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_r		0		300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_f		0		300	ns
Fall Time of SDA Signal, Transmitting	t_f	(Note 6)	$20 + 0.1C_b$		250	ns
Setup Time for STOP (P) Condition	$t_{SU;STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_b				400	pF
Pulse Width of Spikes that Are Suppressed by the Input Filter	t_{SP}	(Note 7)	0		50	ns

Note 1: The filter passband edge is set to code 255.
Note 2: The filter passband edge is set to code 40.
Note 3: 1H is the total line period, depending on the video standard. For NTSC, this is 63.5µs; for HDTV, the line period is 29.64µs.
Note 4: The clamp level is at the sync tip for signals with sync pulses, and at the blanking level otherwise.
Note 5: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.
Note 6: C_b = total capacitance of one bus line in pF. t_R and t_F measured between $0.3V_{DD}$ and $0.7V_{DD}$.
Note 7: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

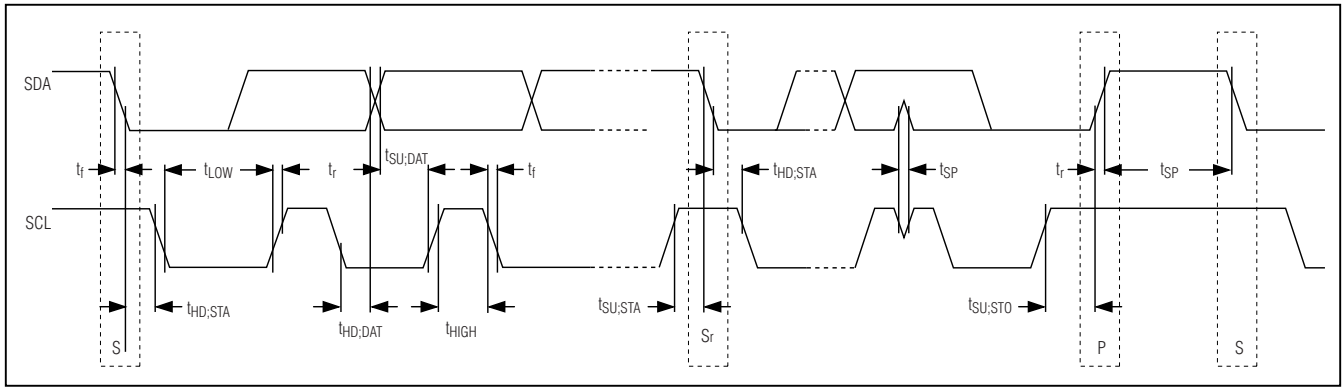
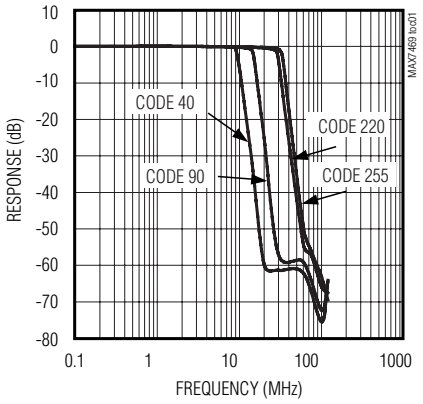


Figure 1. 2-Wire, Serial-Interface Timing Diagram

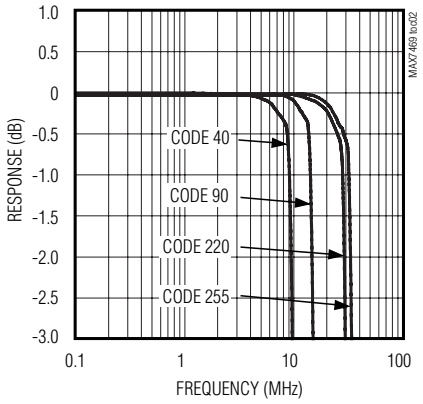
Typical Operating Characteristics

(AV_{DD} = +5V, DV_{DD} = 3.3V, R_{LOAD} = 150Ω to GND, C_{LOAD} = 0 to 20pF to GND, C_{IN} = 0.1µF, T_A = +25°C, unless otherwise noted.)

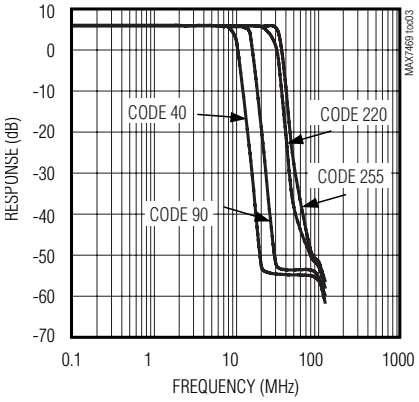
FREQUENCY RESPONSE (MAX7469)



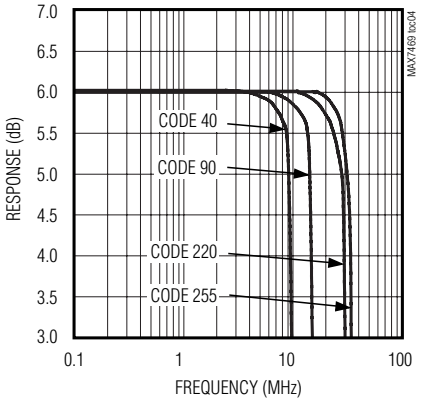
PASSBAND FLATNESS (MAX7469)



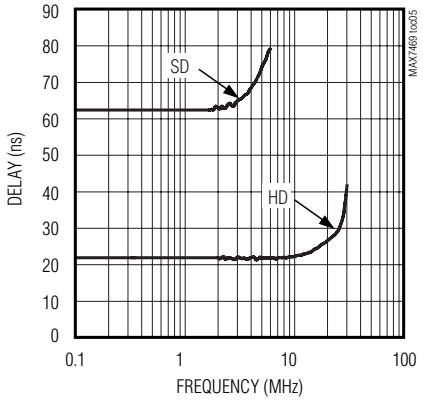
FREQUENCY RESPONSE (MAX7470)



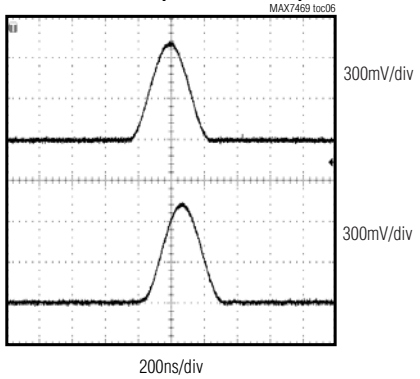
PASSBAND FLATNESS (MAX7470)



GROUP DELAY



2T RESPONSE (1 IRE = 7.14mV)



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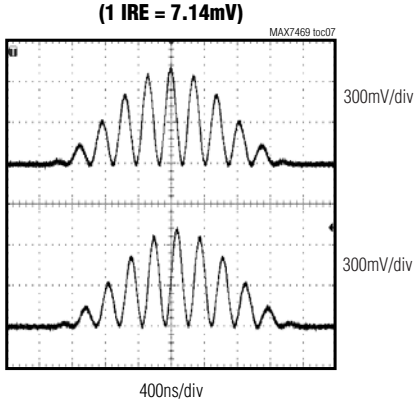
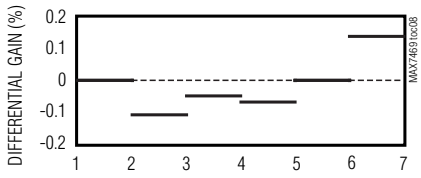
Typical Operating Characteristics (continued)

(AV_{DD} = +5V, DV_{DD} = 3.3V, R_{LOAD} = 150Ω to GND, C_{LOAD} = 0 to 20pF to GND, C_{IN} = 0.1µF, T_A = +25°C, unless otherwise noted.)

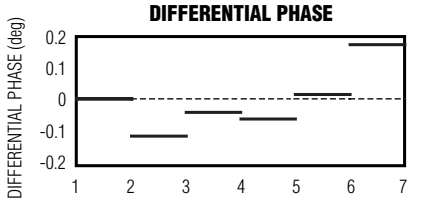
MODULATED 12.5T RESPONSE (1 IRE = 7.14mV)



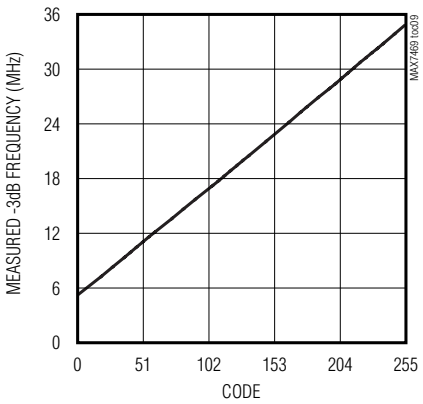
DIFFERENTIAL GAIN



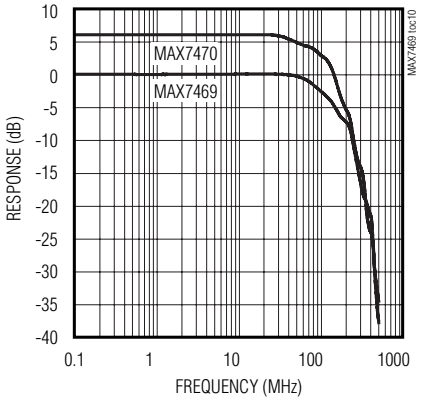
DIFFERENTIAL PHASE



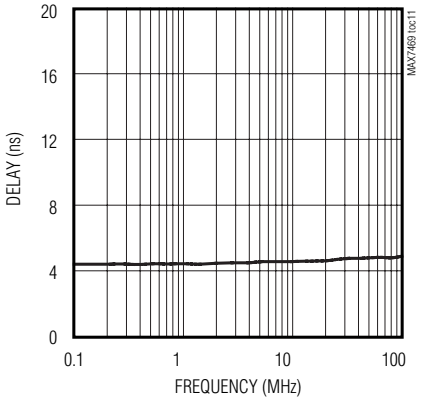
-3dB FREQUENCY vs. CONTROL CODE



BYPASS-MODE FREQUENCY RESPONSE



BYPASS-MODE GROUP DELAY



Pin Description

PIN	NAME	FUNCTION
1	DGND	Digital Ground. See the *Power-Supply Bypassing and Layout Considerations* section.
2	EXTSYNC	External Sync Input. EXTSYNC has an internal 3MΩ resistor to ground. Connect to ground if not used.
3	SCL	I²C-Compatible Serial-Clock Input
4	SDA	I²C-Compatible Serial-Data Input/Output
5	DV_{DD}	Digital Power Supply. Bypass to DGND with a 0.1µF capacitor. See the *Power-Supply Bypassing and Layout Considerations* section.
6	OUT3	Video Output 3. OUT3 can be either DC- or AC-coupled.
7, 9, 11	AV_{DD}	Analog Power Supply. Bypass to GND with a 0.1µF capacitor. See the *Power-Supply Bypassing and Layout Considerations* section.
8	OUT2	Video Output 2. OUT2 can be either DC- or AC-coupled.
10	OUT1	Video Output 1. OUT1 can be either DC- or AC-coupled.
12	A0	I²C Device Address Bit 0
13	A1	I²C Device Address Bit 1
14, 15, 17, 19	GND	Ground. Connect all GND pins to the ground plane. See the *Power-Supply Bypassing and Layout Considerations* section.
16	IN1	Video Input 1. AC-couple IN1 with a series 0.1µF capacitor.
18	IN2	Video Input 2. AC-couple IN2 with a series 0.1µF capacitor.
20	IN3	Video Input 3. AC-couple IN3 with a series 0.1µF capacitor.
—	EP	Exposed Pad. Internally connected to GND. Do not route any PC board traces under package. Connect EP to the ground plane. See the *Power-Supply Bypassing and Layout Considerations* section.

Detailed Description

The MAX7469/MAX7470 are complete video anti-aliasing solutions, ideal for fixed-pixel HDTV display technologies, such as plasma and LCD, which digitize the input video signal and then scale the resolution to match the native pixel format of the display. With a software-selectable corner frequency ranging from 5MHz to 34MHz, the MAX7469/MAX7470 support both SD and HD video signals, including 1080i, 720p, 720i, 480p, and 480i. Higher bandwidth computer resolution signals are also supported.

Integrated lowpass filters limit the analog video input bandwidth for anti-aliasing and out-of-band noise reduction prior to sampling by an ADC or video decoder. By allowing the corner frequency to be adjusted from below SD resolution to beyond HD resolutions in 256 linear steps, the filter's corner frequency can be optimized dynamically for a specific input video signal and the sampling frequency of the ADC or video decoder. For applications requiring a passband greater than the maximum frequency setting, a filter bypass mode is also provided.

An I²C interface allows a microcontroller (µC) to configure the MAX7469/MAX7470s' performance and functionality, including the clamp voltage, the filter corner frequency, the sync source (internal/external), filter bypassing, etc.

The *Typical Operating Circuit* shows the MAX7469/MAX7470 block diagram and typical external connections.

Sync Detector and Clamp Settings

The MAX7469/MAX7470 use a video clamp circuit to establish a DC offset for the incoming video signal after the AC-coupling capacitor. This video clamp sets the DC bias level of the circuit at the optimum operating point.

The MAX7469/MAX7470 support both internal and external sync detection. Selection of internal vs. external detection is achieved by programming the command byte (see Table 3). After extracting the sync information from channel 1 (or an external sync: SYNCA, SYNCB, or SYNC), the MAX7469/MAX7470 clamp the video signal during the sync tip portion of the video. Select one of two possible clamp levels according to the input signal format. Use the low level when the input signal contains sync information, such as a Y (luma) or CVBS signal.

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Table 1. Clamp Levels

INPUT SIGNAL FORMAT	CLAMP LEVEL		
	CHANNEL 1	CHANNEL 2	CHANNEL 3
Y P_b P_r	Low	High	High
G_SBR	Low	High	High
CVBS Y C	Low	Low	High
Y P_b P_r (sync on all signals)	Low	Low	Low
R G B H V	High	High	High

Use the high level for bipolar signals, such as C (chroma) or P_b/P_r. See Table 1 for more details.

Component/Composite Selection

The MAX7469/MAX7470 accept component or composite inputs. When configured for composite video inputs, the color-burst filter is enabled; if configured for component video inputs, the color-burst filter is disabled. This filter is separate from the main filter and not in the direct signal path so that it has no effect on the overall frequency response. With normal video signals and levels, the use of this color-burst filter has a negligible effect on the sync detection. It has a more significant effect under conditions of low-signal amplitude coupled with higher relative amplitude color burst.

External Sync Detection (EXTSYNC)

When filtering a video signal without embedded sync information, such as computer formats (RGBHV) with separate sync signals, use the external sync mode (see Table 3) and apply the horizontal sync source to the EXTSYNC pin. The sync detector determines when the clamp circuit is turned on.

The MAX7469/MAX7470 are able to detect positive or negative polarity external syncs with TTL logic levels. Use the I²C interface to program the polarity of the external sync signal.

Filter

The internal video filter delivers an optimized response with a steep transition band to achieve a wide passband along with excellent stopband rejection. In addition, the filter is optimized to provide an excellent time domain response with low overshoot.

Setting the Filter Frequency

Use the I²C interface to vary the frequency response (-3dB cutoff frequency) of the filter in the MAX7469/MAX7470 from less than the SD passband to beyond the HD passband in 256 linear steps. Write command byte 12h to access the frequency register, followed by an 8-bit data word that corresponds to the desired frequency. See the *Frequency Register* section for more details.

The frequency set by the MAX7469/MAX7470 is the -3dB point. Set the frequency according to the desired flat passband response.

Optimizing the Frequency Response

Select the frequency response according to the resolution of the video-signal format. High-definition signals require higher bandwidth, while standard-definition signals require less bandwidth. The actual bandwidth contained in the video signal is a function of the visual resolution of the signal. This bandwidth is typically less than what is indicated by the format resolution (1080i, 720p, etc.). For more information, see Maxim Application Note 750: *Bandwidth Versus Video Resolution*, which is available on www.maxim-ic.com.

The frequency response can be optimized to improve the overall performance. It is important, at a minimum, to meet the Nyquist criterion. Beyond this, the frequency response can be further optimized. In oversampled systems, the sample rate is significantly more than the desired passband response. The extra frequency span between the passband and the sample rate contains noise and other undesirable interferers that can be eliminated by setting the corner frequency of the filter to just pass the desired bandwidth. This results in a higher signal-to-noise ratio of the overall system.

Filter Bypass

The MAX7469/MAX7470 offer selectable filter bypassing that allows the input video signals to bypass the internal filters and reach the output buffers unfiltered. Write the appropriate command byte to enable (0Eh) or disable (0Fh) filter-bypass mode as shown Table 3.

Output Buffer

Each output buffer can drive a $2V_{P-P}$ signal into a 150Ω video load. The MAX7469/MAX7470 can drive a DC- or AC-coupled load. Output AC-coupling capacitors can be eliminated when driving a cable, thereby eliminating the normal adverse effects caused by these large capacitors, such as line, and field-time distortion, also known as droop. The output DC level is controlled to limit the DC voltage on the cable so that the blanking level of the video signal is always less than 1V, meeting digital TV specification. See the *Output Considerations* section for more information.

Gain Options

The MAX7469 features an overall gain of 0dB, while the MAX7470 features an overall gain of +6dB. Use the MAX7470 when driving a back-matched cable and the

MAX7469 when driving an ADC or video decoder with an input range the same as the input to the MAX7469. For added flexibility, the MAX7469 accepts input signals with twice the standard video-signal range, which can be used for driving an ADC or video decoder with an input signal range that accepts a larger signal swing. The MAX7470 can also be used to drive an ADC or video decoder when a gain of two is desired.

Output Clamp Level

The MAX7469/MAX7470 output can be DC- or AC-coupled. The nominal output clamp level in the DC-coupled case depends on the clamp voltage setting and can be determined according to Table 2.

Table 2. Output Clamp Level

CLAMP SETTING	OUTPUT CLAMP LEVEL (V)
Low	1.0 (typ)
High	1.6 (typ)

As shown in the *Sync Detector and Clamp Settings* section, the low clamp level is used for signals with sync information and determines the voltage level of the sync tip, while the high clamp level is used for signals without sync information and sets the blanking level.

The absolute voltage level of the output signal is relative to the output clamp level. A video signal containing sync information (i.e., CVBS or Y) is unipolar above the clamp level and conversely, a video signal without sync (i.e., P_b P_r or C) is bipolar around the clamp level.

Power-Down Mode

The MAX7469/MAX7470 include a power-down mode that reduces the supply current from 180mA (typ) to 1mA (typ) by powering down the analog circuitry. The I^2C interface remains active, allowing the device to return to full-power operation. The clamp settling time (see the *Electrical Characteristics* section) limits the wake-up time of the MAX7469/MAX7470. After exiting the power-down mode, the MAX7469/MAX7470 resume normal operation using the settings stored prior to power-down. The power-down and wake-up modes are controlled through the command byte (see Table 3). A software reset sets the control/status register to its default conditions, but the frequency register is not affected.

Power-On Reset (POR)

The MAX7469/MAX7470 include a POR circuit that resets the internal registers and I^2C interface to their default conditions (see Tables 4, 5, and 6).

Serial Interface

The MAX7469/MAX7470 feature an I^2C-compatible, 2-wire serial interface consisting of a bidirectional serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX7469/MAX7470 and the master at rates up to 400kHz.

The MAX7469/MAX7470 have a command interpreter that is accessed by writing a valid command byte. Once a command byte is written to the MAX7469/MAX7470, the command interpreter updates the control/status register accordingly. See the *Control/Status Register* section for more information. The command interpreter also controls access to the frequency register through a command byte (see the *Command Byte (Write Cycle)* section).

The MAX7469/MAX7470 are transmit/receive slave-only devices, relying upon a master to generate a clock signal. The master (typically a µC) initiates data transfer on the bus and generates SCL.

A master device communicates to the MAX7469/MAX7470 by transmitting the proper address (see the *Slave Address* section) followed by a command and/or data words. Each transmit sequence is framed with a START (S) or REPEATED START (Sr) condition and a STOP (P) condition.

The SDA driver is an open-drain output, requiring a pullup resistor (2.4kΩ or greater) to generate a logic-high voltage. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot of the bus signals.

Bit Transfer

Each SCL rising edge transfers 1 data bit. Nine clock cycles are required to transfer the data into or out of the MAX7469/MAX7470. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are read as control signals (see the *START and STOP Conditions* section). When the serial interface is inactive, SDA and SCL idle high.

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START and STOP Conditions

A master device initiates communication by issuing a START condition, a high-to-low transition on SDA with SCL high (Figure 2). The master terminates transmission by a STOP condition (see the *Acknowledge Bit (ACK) and Not-Acknowledge Bit (NACK)* section). A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 2). The STOP condition frees the bus. If a repeated START condition is generated instead of a STOP condition, the bus remains active. When a STOP condition or incorrect address is detected, the MAX7469/MAX7470 then ignore all communication on the I²C bus until the next START or REPEATED START condition, minimizing digital noise and feedthrough.

Early STOP Conditions

The MAX7469/MAX7470 recognize a STOP condition at any point during transmission except when a STOP condition occurs in the same high pulse as a START condition (Figure 3). This condition is not a legal I²C format; at least one clock pulse must separate any START and STOP conditions. The MAX7469/MAX7470 discard any data received during a data transfer aborted by an early STOP condition.

Repeated START (S_r) Conditions

An Sr condition is used to indicate a change in direction of data flow (see the *Read Cycle* section). Sr can also be used when the bus master is writing to several I²C devices and does not want to relinquish control of the bus. The MAX7469/MAX7470 serial interface supports continuous write operations with (or without) an Sr condition separating them.

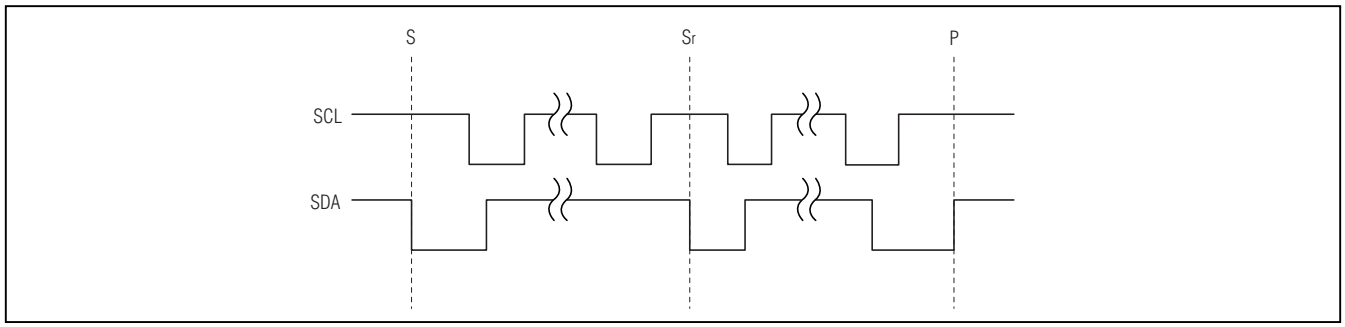

Figure 2. START/STOP Conditions

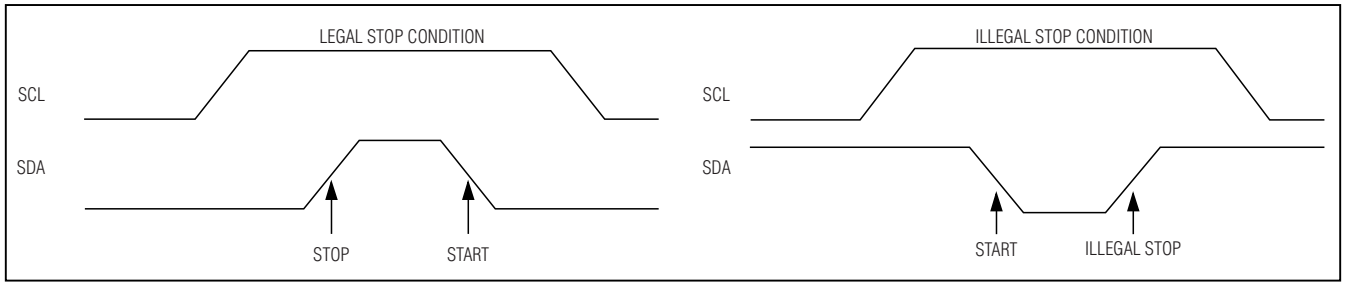

Figure 3. Early STOP Conditions

Acknowledge Bit (ACK) and Not-Acknowledge Bit (NACK)

Successful data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX7469/MAX7470 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse (Figure 4). To generate a NACK, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse (ninth pulse) and leaves it high during the high period of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the master should reattempt communication at a later time.

The MAX7469/MAX7470 generate an acknowledge bit when receiving an address or data by pulling SDA low during the ninth clock pulse. When transmitting data during a read, the MAX7469/MAX7470 do not drive SDA during the ninth clock pulse (i.e., the external pullups define the bus as a logic-high) so that the receiver of the data can pull SDA low to acknowledge receipt of data.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition, followed by the 7-bit slave address (Figure 5). When idle, the MAX7469/MAX7470 wait for a START condition, followed by their slave address. The serial interface compares each address bit by bit, allowing the interface to power down and disconnect from SCL immediately if an incorrect address is detected. After recognizing a START condition followed by the correct address, the MAX7469/MAX7470 are ready to accept or send data. The least significant bit (LSB) of the address byte (R/$\overline{W}$) determines whether the master is writing to or reading from the MAX7469/MAX7470 (R/$\overline{W}$ = 0 selects a write condition, R/$\overline{W}$ = 1 selects a read condition). After receiving the proper address, the MAX7469/MAX7470 (slave) issue an ACK by pulling SDA low for one clock cycle.

The MAX7469/MAX7470 slave address consists of 5 fixed bits, A6–A2 (set to 10010), followed by 2 pin-programmable bits, A1 and A0. The most significant address bit (A6) is transmitted first, followed by the remaining bits. Addresses A1 and A0 can also be driven dynamically if required, but the values must be stable when they are expected in the address sequence.

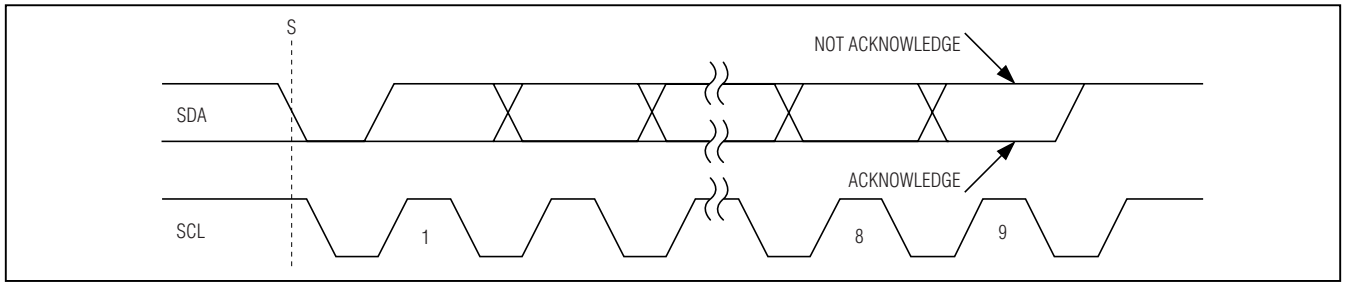

Figure 4. Acknowledge and Not-Acknowledge Bits

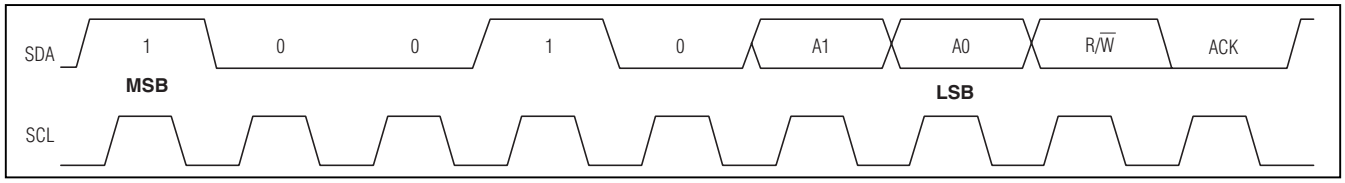

Figure 5. Slave-Address Byte Definition

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Command Byte (Write Cycle)

A write cycle begins with the bus master issuing a START condition followed by 7 address bits (Figure 5) and 1 write bit ($R/\overline{W} = 0$). After successfully receiving its address, the MAX7469/MAX7470 (slave) issue an ACK. The slave recognizes the next byte after a successfully received address as the command byte (Table 3).

Use the command byte to configure the MAX7469/MAX7470. While most of the commands listed in Table 3 modify the functionality of the MAX7469/MAX7470, some commands prepare the device for further data transfers (see the *Control/Status Register* and *Frequency Register* sections). If the write cycle is prematurely aborted, the register is not updated, and the

Table 3. Command Byte Definition

COMMAND BYTE: INDIVIDUAL BIT DEFINITIONS								DESCRIPTION
C7	C6	C5	C4	C3	C2	C1	C0	
0	0	0	0	0	0	0	0	Enters power-down mode.
0	0	0	0	0	0	0	1	Wake-up; resumes normal operation using the frequency/status previously stored (unless power has been cycled).
0	0	0	0	0	0	1	0	Sets IN1 clamp voltage level to low.
0	0	0	0	0	0	1	1	Sets IN1 clamp voltage level to high.
0	0	0	0	0	1	0	0	Sets IN2 clamp voltage level to low.
0	0	0	0	0	1	0	1	Sets IN2 clamp voltage level to high.
0	0	0	0	0	1	1	0	Sets IN3 clamp voltage level to low.
0	0	0	0	0	1	1	1	Sets IN3 clamp voltage level to high.
0	0	0	0	1	0	0	0	Selects component input, color-burst filter disabled.
0	0	0	0	1	0	0	1	Selects composite input, color-burst filter enabled.
0	0	0	0	1	0	1	0	Selects internal sync.
0	0	0	0	1	0	1	1	Selects external sync.
0	0	0	0	1	1	0	0	Selects positive polarity external sync.
0	0	0	0	1	1	0	1	Selects negative polarity external sync.
0	0	0	0	1	1	1	0	Enables filters.
0	0	0	0	1	1	1	1	Disables filters, enters bypass mode.
0	0	0	1	0	0	0	0	Resets the control/status register to the default values as described in the *Control/Status Register* section. This command does not affect the frequency register.
0	0	0	1	0	0	0	1	Requests a control/status register read. The interface expects an Sr condition to follow with address and read/write set to read so data can be driven onto the bus.
0	0	0	1	0	0	1	0	Loads the frequency register with the data byte following the command byte.
0	0	0	1	0	0	1	1	Requests a frequency register read. The interface expects an Sr condition to follow with address and read/write set to read so data can be driven onto the bus.

write sequence must be repeated. Figures 6 and 7 show examples of write sequences.

Read Cycle

In read mode (R/$\overline{W}$ = 1), the MAX7469/MAX7470 write the contents of the control/status or frequency registers to the bus. When the command byte indicates a read operation of either the control/status or the frequency register, the serial interface expects an Sr condition to follow the command byte. After sending an Sr, the master sends the MAX7469/MAX7470 slave address byte followed by a R/$\overline{W}$ bit (set to 1 to indicate a read). The slave device (MAX7469/MAX7470) generates an ACK for the second address word and immediately after the ACK clock pulse, the direction of data flow reverses. The slave (MAX7469/MAX7470) then transmits 1 byte of data containing the value of the register that was

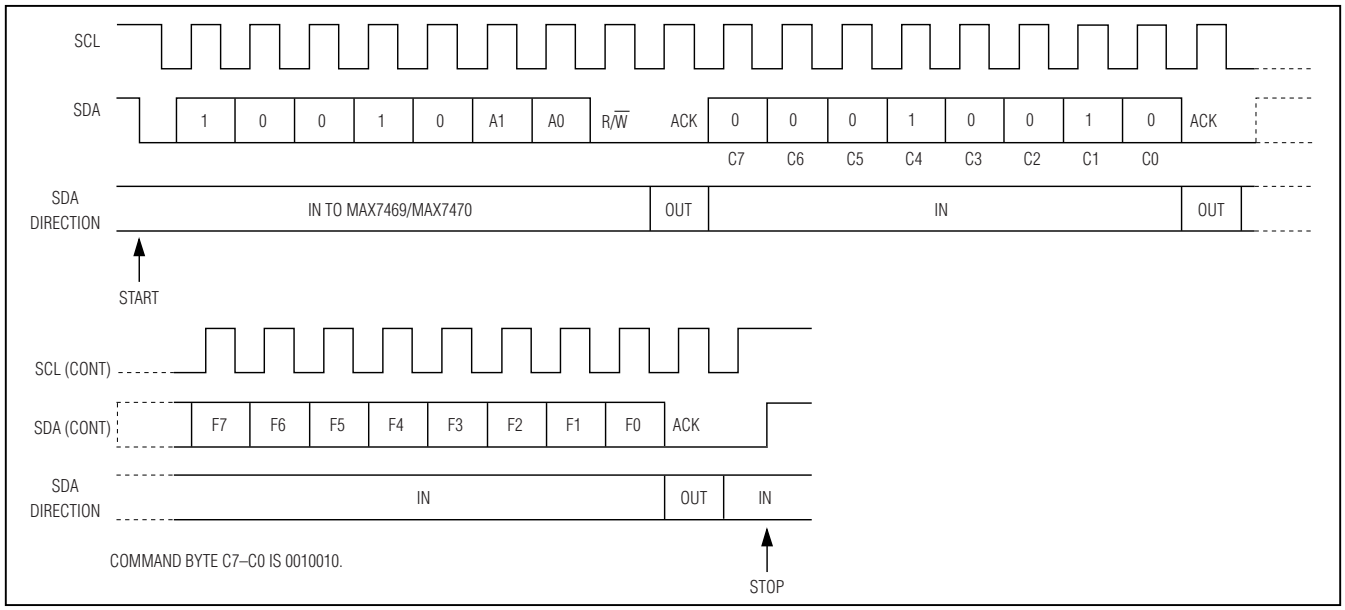

Figure 6. Write Sequence to Update the Frequency Register

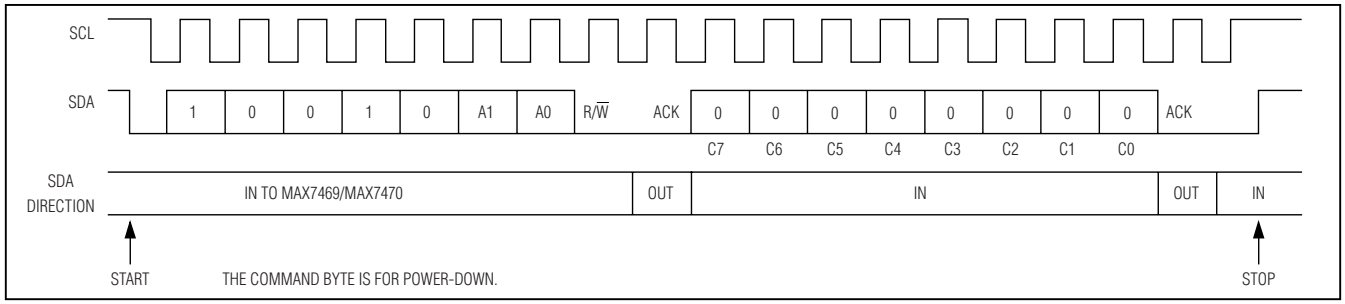

Figure 7. Write Sequence for a Command Byte

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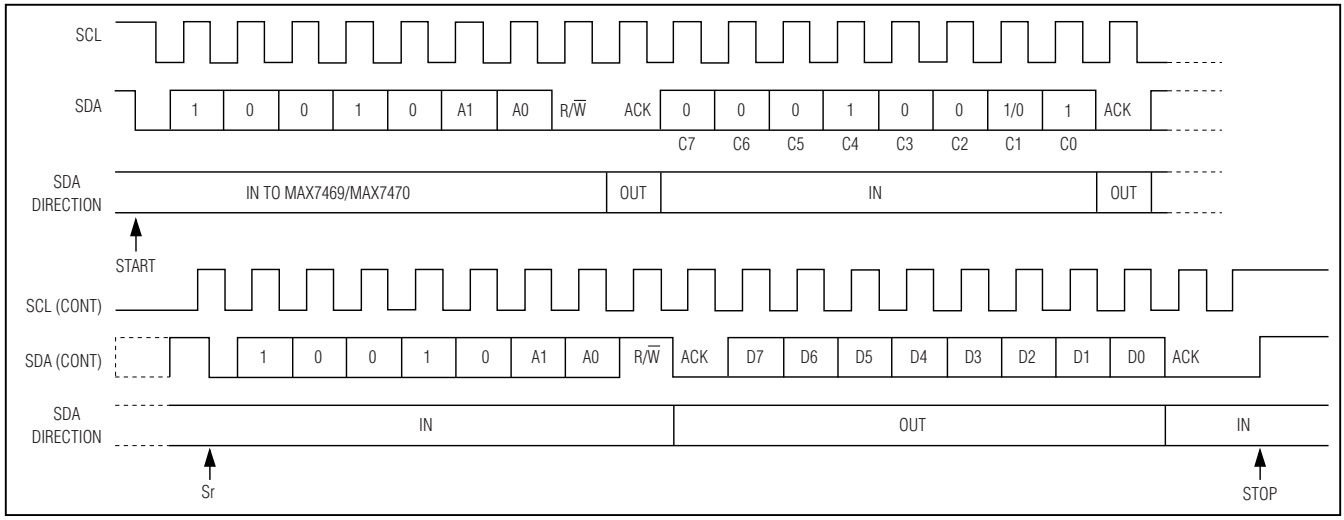

Figure 8. Basic Read Sequence

selected in the command byte. Figure 8 shows a basic read sequence.

Note: The master has to write a command byte, requesting to read the control/status or frequency register, to the slave (MAX7469/MAX7470) before the master can read the contents of the selected register.

Control/Status Register

The MAX7469/MAX7470 store their status in an 8-bit register that can be read back by the master. The individual bits of the control/status register are summarized in Tables 4 and 5. The power-on default value of this register is 03h.

Frequency Register

The frequency response (-3dB passband edge) of the MAX7469/MAX7470 can be continuously varied in 256 linear steps by changing the codes in the frequency register (Table 6). See the *Command Byte* (*Write Cycle)* section for a write sequence to update the frequency register.

Table 4. Control/Status Register

CONTROL/STATUS REGISTER							
S7	S6	S5	S4	S3	S2	S1	S0

Table 5. Control/Status Register Bit Description

BIT	DESCRIPTION
S7	0 = component input signal selected (default). 1 = composite input signal selected.
S6	0 = internal sync enabled (default). 1 = external sync enabled.
S5	0 = external sync: positive polarity (default). 1 = external sync: negative polarity.
S4	0 = normal operation mode (default). 1 = power-down mode.
S3	0 = filters enabled (default). 1 = bypass mode—no filtering.
S2	0 = clamp voltage for IN1 set to low (default). 1 = clamp voltage for IN1 set to high.
S1	0 = clamp voltage for IN2 set to low. 1 = clamp voltage for IN2 set to high (default).
S0	0 = clamp voltage for IN3 set to low. 1 = clamp voltage for IN3 set to high (default).

Table 6. Frequency Register Setting for Different Video-Signal Formats

VIDEO-SIGNAL FORMAT	F7	F6	F5	F4	F3	F2	F1	F0	CODE NO.	APPROXIMATE FREQUENCY (-3dB) MHz
Standard Definition (Interlaced)	0	0	1	0	1	0	0	0	40	10
Standard Definition (Progressive)	0	1	0	1	1	0	1	0	90	15
High-Definition Low Bandwidth	1	1	0	1	1	1	0	0	220	30
High-Definition High Bandwidth	1	1	1	1	1	1	1	1	255	34 (default)

I²C Compatibility

The MAX7469/MAX7470 are compatible with existing I²C systems supporting standard I²C 8-bit communications. The general call address is ignored, and CBUS formats are not supported. The device's address is compatible with 7-bit I²C addressing protocol only; 10-bit address formats are not supported.

Applications Information

Input Considerations

Use 0.1µF ceramic capacitors to AC-couple the inputs. The inputs cannot be DC-coupled. The internal clamp circuit stores a DC voltage across the input capacitors to obtain the appropriate output DC voltage level. Increasing the value of these capacitors to improve line-time distortion is not necessary due to the extremely low input leakage current yielding a very low line-time distortion performance.

The MAX7469/MAX7470 provide a high input impedance to allow a nonzero source impedance to be used, such as when the input is connected directly to a back-matched video cable, ensuring the external resistance determines the termination impedance.

Output Considerations

The MAX7469/MAX7470 outputs can be DC- or AC-coupled. The MAX7470, with its +6dB gain, is typically connected to a 75Ω series back-match resistor followed by the video cable. Because of the inherent divide-by-two of this configuration, the blanking level of the video signal is always less than 1V, which complies with digital TV requirements.

The MAX7469, with its 0dB gain, is typically connected to an ADC or video decoder. This can be a DC or AC connection. If a DC connection is used, ensure that the DC input requirements of the ADC or video decoder are compatible.

If an AC connection is used, choose an AC-coupling capacitor value that ensures that the lowest frequency content in the video signal is passed and the line-time distortion is kept within desired limits. The selection of this value is a function of the input impedance and, more importantly, the input leakage of the circuit being driven. Use a video clamp to reestablish the DC level, if not already included in the subsequent circuit.

The outputs of the MAX7469/MAX7470 are fully protected against a short-circuit condition either to ground or the positive supply of the device.

Power-Supply Bypassing and Layout Considerations

The MAX7469/MAX7470 operate from a single +5V analog supply and a +3.3V digital supply. Bypass AV_{DD} to GND with a 0.1µF capacitor and an additional 1µF capacitor in parallel for additional low-frequency decoupling. Determine the proper power-supply bypassing necessary by taking into account the desired disturbance level tolerable on the output, the power-supply rejection of the MAX7469/MAX7470, and the amplitude and frequency of the disturbance signals present in the vicinity of the MAX7469/MAX7470. Use an extensive ground plane to ensure optimum performance. The three AV_{DD} pins (pins 7, 9, and 11) that supply the individual channels can be connected together and bypassed as one, provided the components are close to the pins. Bypass DV_{DD} to DGND with a 0.1µF capacitor. All ground pins (GND) must be connected to a low impedance ground plane as close as possible to the device.

Place the input termination resistors as close as possible to the device. Alternatively, the terminations can be placed further from the device if the PC board traces are designed to be a controlled impedance of 75Ω. Minimize parasitic capacitance as much as possible to avoid performance degradation in the upper frequency range possible with the MAX7469/MAX7470.

Refer to the MAX7469/MAX7470 evaluation kit for a proven PC board layout.

Exposed Pad and Heat Dissipation

The MAX7469/MAX7470 TQFN package has an exposed pad on its bottom. This pad is electrically connected, internal to the device, to GND. Do not route any PC board traces under the package.

The MAX7469/MAX7470 typically dissipate 900mW of power, therefore, pay careful attention to heat dispersion. The use of at least a two-layer board with a good ground plane is recommended. To maximize heat dispersion, place copper directly under the MAX7469/MAX7470 package so that it matches the outline of the plastic encapsulated area. Do the same thing on the bottom ground plane layer and then place as many vias as possible connecting the top and bottom layers to thermally connect it to the ground plane.

Maxim has evaluated a four-layer board using FR-4 material and 1oz copper with equal areas of metal on the top and bottom side coincident with the plastic encapsulated area of the 20-pin TQFN package. The two middle layers are used as power and ground

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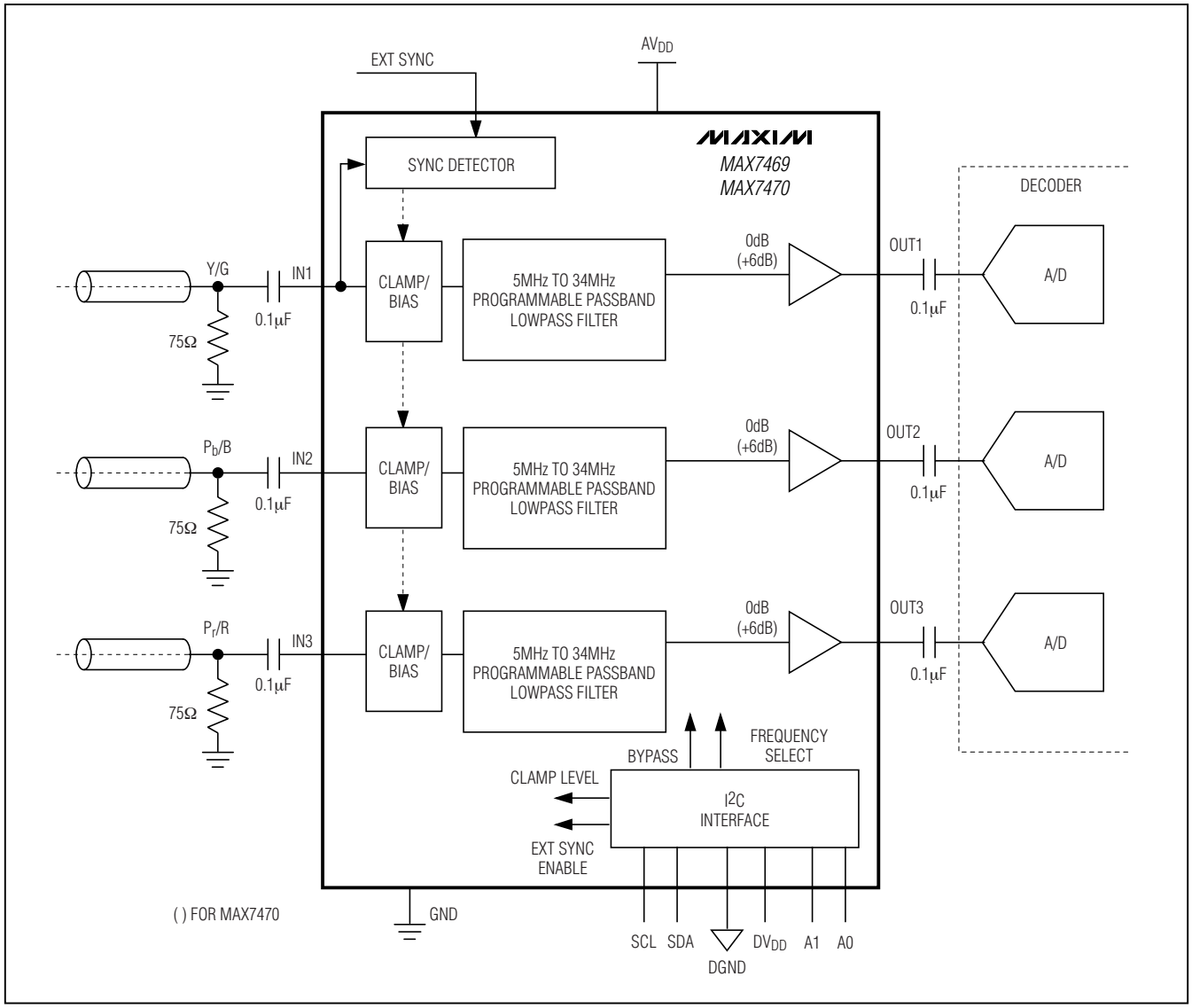
planes. The board has 21, 15-mil, plated-through via holes between the top, bottom, and ground plane layers. Thermocouple measurements confirm device temperatures to be safely within maximum limits.

Chip Information

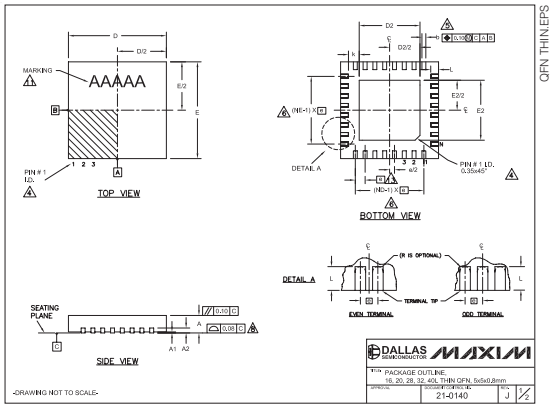
PROCESS: BiCMOS

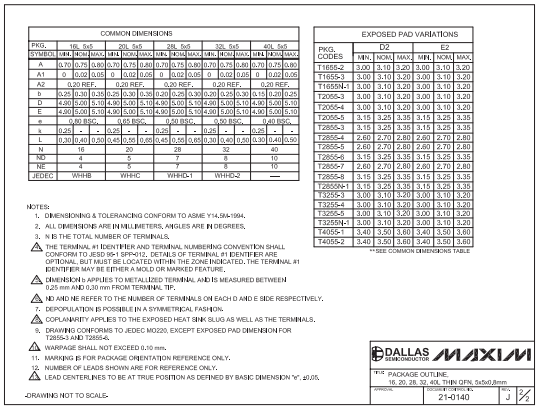
Typical Operating Circuit



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)





COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2		0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.	
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e		0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.	
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			—		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

** SEE COMMON DIMENSIONS TABLE

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1 AND T2855-4.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e". ±0.05.

-DRAWING NOT TO SCALE-

PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm
21-0140