

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE3050KA uses advanced trench technology and design to provide excellent R_{DS(ON)} with low gate charge. It can be used in a wide variety of applications.

General Features

V_{DS} =30V,I_D =50A

 $R_{DS(ON)}$ < 11m Ω @ V_{GS} =10V

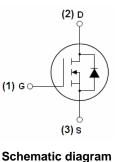
 $R_{DS(ON)}$ < 16m Ω @ V_{GS} =5V

- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible Power Supply

100% UIS TESTED!





Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE3050KA	NCE3050KA	TO-252-2L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _G s	±20	V
Drain Current-Continuous	I _D	50	Α
Drain Current-Continuous(T _C =100°C)	I _D (100°C)	35	Α
Pulsed Drain Current	I _{DM}	140	Α
Maximum Power Dissipation	P _D	60	W
Derating factor		0.4	W/℃
Single pulse avalanche energy (Note 5)	E _{AS}	225	mJ
Operating Junction and Storage Temperature Range	T_{J}, T_{STG}	-55 To 175	$^{\circ}$



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NCE3050KA

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	R _{eJC}	2.5	°C/W	Ī
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Electrical Characteristics (T_c=25 ℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit	
Off Characteristics			•				
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	30	33	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V,V _{GS} =0V	-	-	1	μΑ	
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA	
On Characteristics (Note 3)							
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$	1.0	1.1	1.4	V	
Drain-Source On-State Resistance	1	V _{GS} =10V, I _D =25A	-	8	11		
Diam-Source On-State Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =20A -		10	16	mΩ	
Forward Transconductance	g FS	V _{DS} =5V,I _D =20A	15	-	-	S	
Dynamic Characteristics (Note4)	<u>.</u>						
Input Capacitance	C _{lss}	\/ -45\/\/ -0\/	-	2000	-	PF	
Output Capacitance	Coss	V_{DS} =15V, V_{GS} =0V, F=1.0MHz	-	280	-	PF	
Reverse Transfer Capacitance	C _{rss}	F=1.UIVIFIZ	-	160	-	PF	
Switching Characteristics (Note 4)							
Turn-on Delay Time	t _{d(on)}		-	10	-	nS	
Turn-on Rise Time	t _r	V _{DD} =15V,I _D =25A	-	8	-	nS	
Turn-Off Delay Time	t _{d(off)}	V_{GS} =10V, R_{GEN} =1.8 Ω	-	30	-	nS	
Turn-Off Fall Time	t _f		-	5	-	nS	
Total Gate Charge	Qg	\/ -40\/1 -25A	-	23	-	nC	
Gate-Source Charge	Q _{gs}	$V_{DS}=10V,I_{D}=25A,$ $V_{GS}=10V$	-	7	-	nC	
Gate-Drain Charge	Q _{gd}	V _{GS} =10V	-	4.5	-	nC	
Drain-Source Diode Characteristics							
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =25A	-	0.85	1.2	V	
Diode Forward Current (Note 2)	Is		-	-	40	Α	
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF = 25A	-	22	35	nS	
Reverse Recovery Charge	Qrr	di/dt = 100A/µs ^(Note3)	-	12	20	nC	
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)					

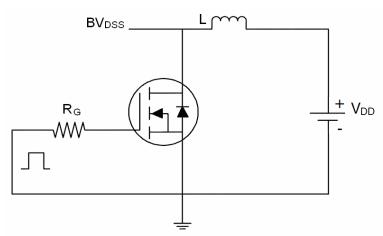
Notes:

- $\textbf{1.} \ \textbf{Repetitive Rating: Pulse width limited by maximum junction temperature.}$
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- 3. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.
- **4.** Guaranteed by design, not subject to production
- **5.** EAS condition: Tj=25 $^{\circ}$ C, V_{DD}=15V,V_G=10V,L=0.5mH, Rg=25 Ω

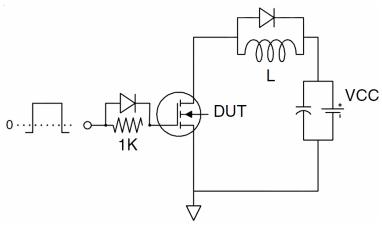


Test circuit

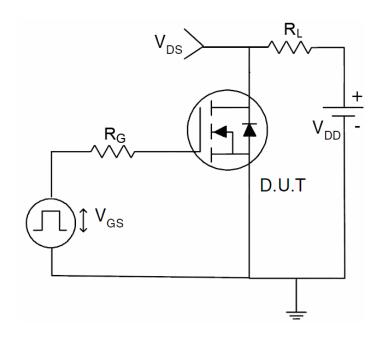
1) E_{AS} test Circuits



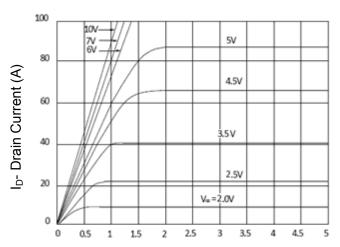
2) Gate charge test Circuit:



3) Switch Time Test Circuit:

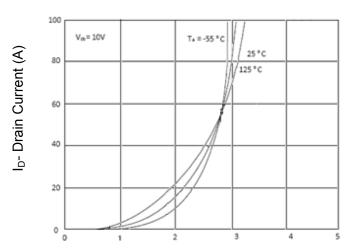


Typical Electrical and Thermal Characteristics (Curves)



Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



Vgs Gate-Source Voltage (V)
Figure 2 Transfer Characteristics

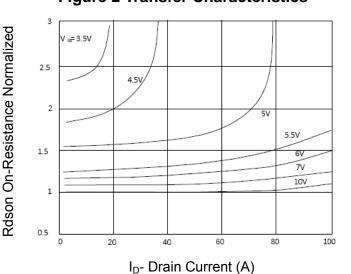


Figure 3 Rdson- Drain Current

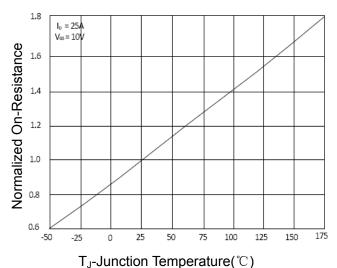
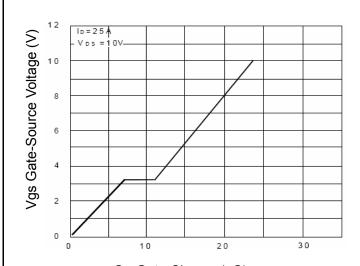


Figure 4 Rdson-JunctionTemperature



Qg Gate Charge (nC)
Figure 5 Gate Charge

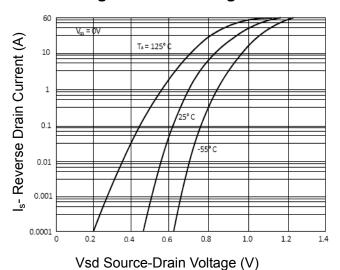


Figure 6 Source- Drain Diode Forward

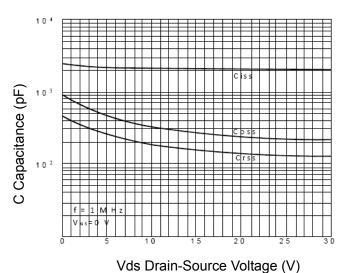
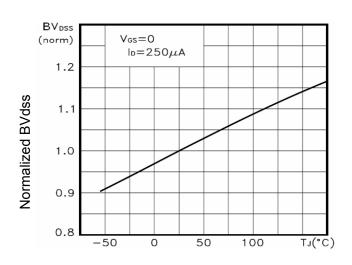
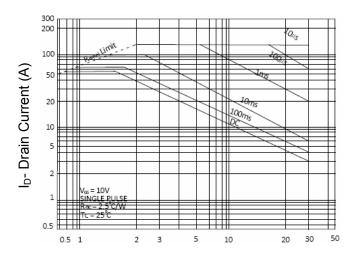


Figure 7 Capacitance vs Vds

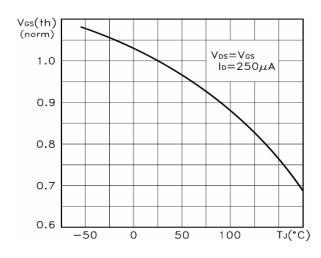


 T_J -Junction Temperature (°C) Figure 9 BV_{DSS} vs Junction Temperature



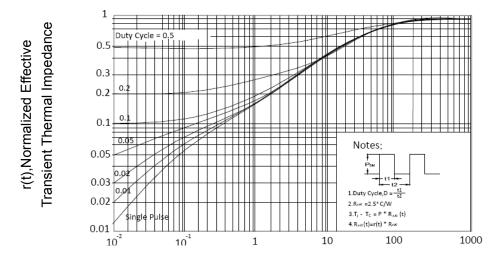
Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



T_J-Junction Temperature(°C)

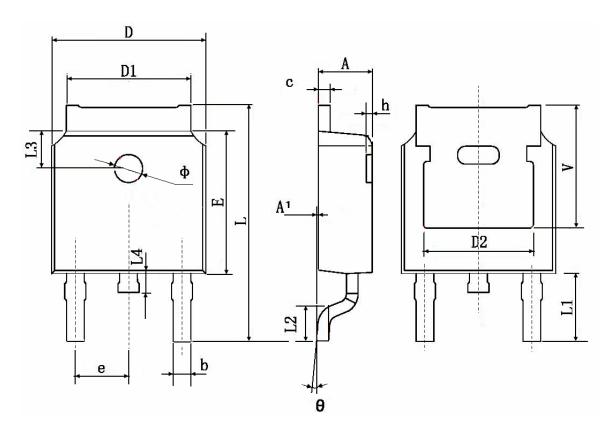
Figure 10 $V_{GS(th)}$ vs Junction Temperature



Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Complete al	Dimensions	In Millimeters	Dimensions In Inches			
Symbol	Min.	Max.	Min.	Max.		
Α	2.200	2.400	0.087	0.094		
A1	0.000	0.127	0.000	0.005		
b	0.660	0.860	0.026	0.034		
С	0.460	0.580	0.018	0.023		
D	6.500	6.700	0.256	0.264		
D1	5.100	5.460	0.201	0.215		
D2	0.483	TYP.	0.190 TYP.			
Е	6.000	6.200	0.236	0.244		
е	2.186	2.386	0.086	0.094		
L	9.800	10.400	0.386	0.409		
L1	2.900	2.900 TYP.		TYP.		
L2	1.400	1.700	0.055	0.067		
L3	1.600	1.600 TYP.		TYP.		
L4	0.600	1.000	0.024	0.039		
Ф	1.100	1.300	0.043	0.051		
θ	0°	8°	0°	8°		
h	0.000	0.300	0.000	0.012		
V	5.350	TYP.	0.211 TYP.			



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