PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8752

LOW SKEW 1-TO-8 LVCMOS CLOCK MULTIPLIER/ZERO DELAY BUFFER

GENERAL DESCRIPTION

The ICS8752 is a low voltage, low skew clock generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. With output frequencies up to 240MHz the ICS8752 is targeted for high performance clock applications. Along with a fully integrated PLL the ICS8752 contains frequency configurable outputs and an external feedback input for regenerating clocks with “zero delay”.

Dual clock inputs, REF_CLK1 and REF_CLK2, support redundant clock applications. The CLK_SEL input determines which reference clock is used. The output divider values of Bank A and B are controlled by the DIV_SELA0:1, and DIV_SELB0:1, respectively.

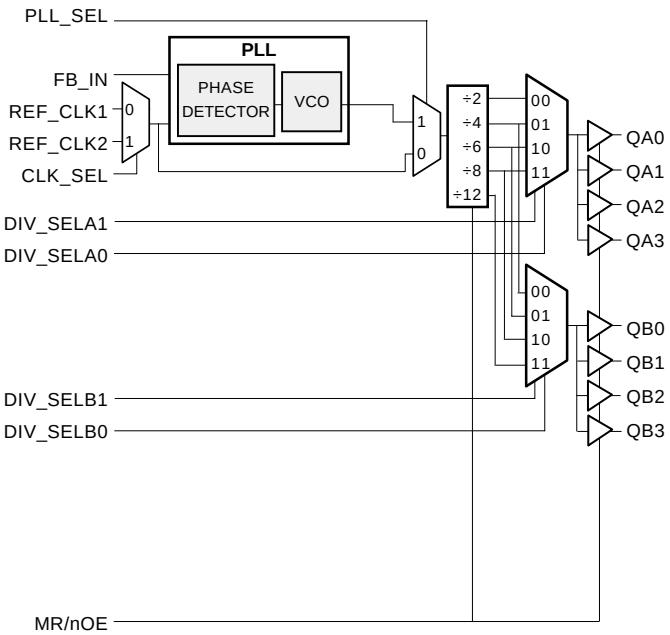
For test and system debug purposes the PLL_SEL input allows the PLL to be bypassed. When HIGH the MR/nOE input resets the internal dividers and forces the outputs to the high impedance state.

The low impedance LVCMOS outputs of the ICS8752 are designed to drive terminated transmission lines. The effective fanout of each output can be doubled by utilizing the ability of each output to drive two series terminated transmission lines.

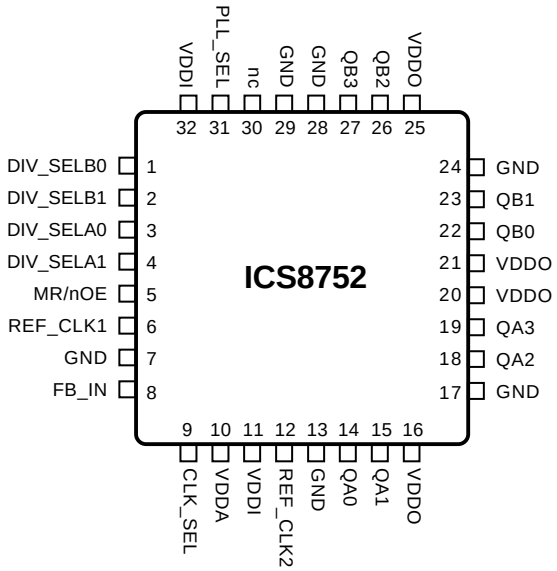
FEATURES

- Fully integrated PLL
- 8 LVCMOS outputs, 7Ω typical output impedance
- External feedback for ”zero delay” clock regeneration
- Output frequency up to 240MHz
- VCO range 220MHz to 480MHz
- Dual LVCMOS clock inputs for redundant clock applications
- LVCMOS control inputs
- Bank skew, tsk(b), 100ps
- Output skew, tsk(o), 150ps
- Multiple-frequency skew, tsk(w), 200ps
- Cycle-to-cycle jitter, tjit(cc), 100ps, typical
- PLL reference zero delay, t(Ø), ±150ps, typical
- Full 3.3V
- 32 lead low-profile QFP (LQFP)
- 7mm x 7mm x 1.4mm package body, 0.8mm lead pitch
- 0°C to 70°C ambient operating temperature
- Functionally compatible with the MPC952 in some applications

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
Y package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	DIV_SELB0, DIV_SELB1	Input	Pulldown	Determines output divider values for bank B as described in Table 3. LVCMOS / LVTTL interface levels.
3, 4	DIV_SELA0, DIV_SELA1	Input	Pulldown	Determines output divider values for bank A as described in Table 3. LVCMOS / LVTTL interface levels.
5	MR/nOE	Input	Pulldown	When HIGH, resets dividers and forces output into high impedance state. LVCMOS / LVTTL interface levels.
6	REF_CLK1	Input	Pulldown	Reference clock input. LVCMOS interface levels.
7, 13 17, 24, 28, 29	GND	Power		Ground pin. Connect to ground.
8	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with "zero delay". LVCMOS / LVTTL interface levels.
9	CLK_SEL	Input	Pulldown	Selects between REF_CLK1 or REF_CLK2 as phase detector reference. When LOW selects REF_CLK1. When HIGH selects REF_CLK2. LVCMOS / LVTTL interface levels.
10	VDDA	Power		PLL power supply pin. Connect to 3.3V.
11, 32	VDDI	Power		Input and core power supply pin. Connect to 3.3V.
12	REF_CLK2	Input	Pulldown	Reference clock input. LVCMOS interface levels.
14, 15, 18, 19	QA0, QA1, QA2, QA3	Output		Bank A clock outputs.7Ω typical output impedance. LVCMOS interface levels.
16, 20, 21, 25	VDDO	Power		Output power supply pins. Connect to 3.3V.
22, 23, 26, 27	QB0, QB1, QB2, QB3	Output		Bank B clock outputs.7Ω typical output impedance. LVCMOS interface levels.
30	nc	Unused		Unused pin.
31	PLL_SEL	Input	Pullup	Selects between the PLL and the reference clock as the input to the dividers. When HIGH select PLL. When LOW selects reference clock. LVCMOS / LVTTL interface levels.
32	VDDI	Power		Input power supply pin. Connect to 3.3V.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	REF_CLK1, REF_CLK2			TBD		pF
		PLL_SEL, FB_IN, CLK_SEL DIV_SELA1, DIV_SELA0, DIV_SELB1, DIV_SELB0			TBD		pF
RPULLUP	Input Pullup Resistor				51		KΩ
RPULLDOWN	Input Pulldown Resistor				51		KΩ
CPD	Power Dissipation Capacitance (per output)		VDDA, VDDI, VDDO = 3.47V		TBD		pF
ROUT	Output Impedance				7		Ω

TABLE 3. CONTROL INPUTS FUNCTION TABLE

Inputs							Outputs	
MR/nOE	PLL_SEL	CLK_SEL	DIV_ SELA1	DIV_ SELA0	DIV_ SELB1	DIV_ SELB0	QAx	QBx
1	X	X	X	X	X	X	Hi-Z	Hi-Z
0	1	X	0	0	0	0	fVCO/2	fVCO/4
0	1	X	0	1	0	1	fVCO/4	fVCO/6
0	1	X	1	0	1	0	fVCO/6	fVCO/8
0	1	X	1	1	1	1	fVCO/8	fVCO/12
0	0	0	0	0	0	0	fREF_CLK1/2	fREF_CLK1/4
0	0	0	0	1	0	1	fREF_CLK1/4	fREF_CLK1/6
0	0	0	1	0	1	0	fREF_CLK1/6	fREF_CLK1/8
0	0	0	1	1	1	1	fREF_CLK1/8	fREF_CLK1/12
0	0	1	0	0	0	0	fREF_CLK2/2	fREF_CLK2/4
0	0	1	0	1	0	1	fREF_CLK2/4	fREF_CLK2/6
0	0	1	1	0	1	0	fREF_CLK2/6	fREF_CLK2/8
0	0	1	1	1	1	1	fREF_CLK2/8	fREF_CLK2/12

NOTE: For normal operation MR/nOE is LOW. When MR/nOE is HIGH all ouputs are disabled.

TABLE 4A. QA OUTPUT FREQUENCY W/FB_IN = QB

INPUTS									OUTPUT
FB_IN	DIV_SELB1	DIV_SELB0	QB OUPUT DIVIDER MODE	REF_CLK1, REF_CLK2 (MHz)		DIV_SELA1	DIV_SELA0	QA OUPUT DIVIDER MODE	QA Multiplier (NOTE 1)
				MIN	MAX				
QB	0	0	÷4	62.5	125	0	0	÷2	2
						0	1	÷4	1
						1	0	÷6	0.667
						1	1	÷8	0.5
QB	0	1	÷6	41.67	83.33	0	0	÷2	3
						0	1	÷4	1.5
						1	0	÷6	1
						1	1	÷8	0.75
QB	1	0	÷8	31.25	62.5	0	0	÷2	4
						0	1	÷4	2
						1	0	÷6	1.33
						1	1	÷8	1
QB	1	1	÷12	20.83	41.67	0	1	÷2	6
						0	1	÷4	3
						1	0	÷6	2
						1	1	÷8	1.5

NOTE 1: NOTE 1: VCO frequency range is 250MHz to 500MHz.
NOTE 2: QA output frequency equal to reference clock frequency times the multiplier;
QB output frequency equal to reference clock.

TABLE 4B. QB OUTPUT FREQUENCY W/FB_IN = QA

INPUTS									OUTPUT
FB_IN	DIV_SELA1	DIV_SELA0	QA OUPUT DIVIDER MODE	REF_CLK1, REF_CLK2 (MHz)		DIV_SELB1	DIV_SELB0	QB OUPUT DIVIDER MODE	QB Multiplier (NOTE 2)
				MIN	MAX				
QA	0	0	÷2	125	250	0	0	÷4	0.5
						0	1	÷6	0.333
						1	0	÷8	0.25
						1	1	÷12	0.083
QA	0	1	÷4	62.5	125	0	0	÷4	1
						0	1	÷6	0.667
						1	0	÷8	0.5
						1	1	÷12	0.333
QA	1	0	÷6	41.67	83.33	0	0	÷4	1.5
						0	1	÷6	1
						1	0	÷8	0.75
						1	1	÷12	0.5
QA	1	1	÷8	31.25	62.5	0	1	÷4	2
						0	1	÷6	1.333
						1	0	÷8	1
						1	1	÷12	0.667

NOTE 1: VCO frequency range is 250MHz to 500MHz.
NOTE 2: QB output frequency equal to reference clock frequency times the multiplier; QA output frequency equal to reference clock.

TABLE 5. PLL INPUT REFERENCE CHARACTERISTICS, VDDI=VDDA=3.3V±5%, T_A=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fREF	Input Reference Frequency		20		240	MHz
tR	Input Rise Time	Measured at 20% to 80% points			TBD	ns
tF	Input Fall Time	Measured at 20% to 80% point			TBD	ns
tDC	Input Reference Duty Cycle		TBD		TBD	%

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDD+0.5 V
Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 6A. POWER SUPPLY DC CHARACTERISTICS, VDDI=VDDA=VDDO=3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage		3.135	3.3	3.465	V
VDDA	Analog Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage		3.135	3.3	3.465	V
IDD	Input Power Supply Current				70	mA

TABLE 6B. LVCMOS/LVTTL DC CHARACTERISTICS, VDDI=VDDA=VDDO=3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage			2		3.765	V
VIL	Input Low Voltage			-0.3		0.8	V
IIH	Input High Current	REF_CLK1, REF_CLK2 FB_IN, CLK_SEL, DIV_SELA1, DIV_SELA0, DIV_SELB1, DIV_SELB0, MR/nOE	VIN = 3.465V			150	µA
		PLL_SEL	VIN = 3.465V			5	µA
IIL	Input Low Current	REF_CLK1, REF_CLK2 FB_IN, CLK_SEL, DIV_SELA1, DIV_SELA0, DIV_SELB1, DIV_SELB0, MR/nOE	VIN = 0V	-5			µA
		PLL_SEL	VIN = 0V	-150			µA
VOH	Output High Voltage		VDDO = 3.135V IOH = -36mA	2.6			V
VOL	Output Low Voltage		VDDO = 3.135V IOL = 36mA			0.5	V

TABLE 7. AC CHARACTERISTICS, VDDI=VDDA=VDDO=3.3V±5%, T_A=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Output Frequency		÷2			240	MHz
			÷4			120	MHz
			÷6			80	MHz
			÷8			60	MHz
			÷12			40	MHz
fVCO	PLL VCO Lock Range			240		480	MHz
tpLH	Propagation Delay, Low-to-High		PLL_SEL=0V, 0MHz ≤ f ≤ 240MHz	TBD		TBD	ns
tpHL	Propagation Delay, High-to-Low		PLL_SEL=0V, 0MHz ≤ f ≤ 240MHz	TBD		TBD	ns
t(Ø)	PLL Reference Zero Delay; NOTE 2		PLL_SEL=3.3V, fREF=TBD, fVCO=TBD		±150		ps
tsk(b)	Bank Skew; NOTE 3	Bank A	Measured on rising edge at VDDO/2			75	ps
		Bank B				100	ps
tsk(o)	Output Skew; NOTE 4		Measured on rising edge at VDDO/2			150	ps
tsk(w)	Multiple Frequency Skew; NOTE 5		Measured on rising edge at VDDO/2			200	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 6				100		ps
tjit(Ø)	Phase Jitter				150		ps
tL	PLL Lock Time					1	mS
tR	Output Rise Time		20% to 80%	300		800	ps
tF	Output Fall Time		20% to 80%	300		800	ps
tPW	Output Pulse Width		0MHz ≤ f ≤ 240MHz	tCYCLE/2 -500	tCYCLE/2	tCYCLE/2 +500	ps
			f = 120MHz	3.65	4.0	4.35	ns
tEN	Output Enable Time					TBD	ns
tDIS	Output Disable Time					TBD	ns

NOTE 1: All parameters measured at fMAX unless noted otherwise. All outputs terminated with 50Ω to VDDO/2.
NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 4: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.
NOTE 5: Defined as skew across banks of outputs operating at different frequency with the same supply voltages and equal load conditions.
NOTE 6: Defined as the variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent pairs of cycles.

PACKAGE OUTLINE - Y SUFFIX

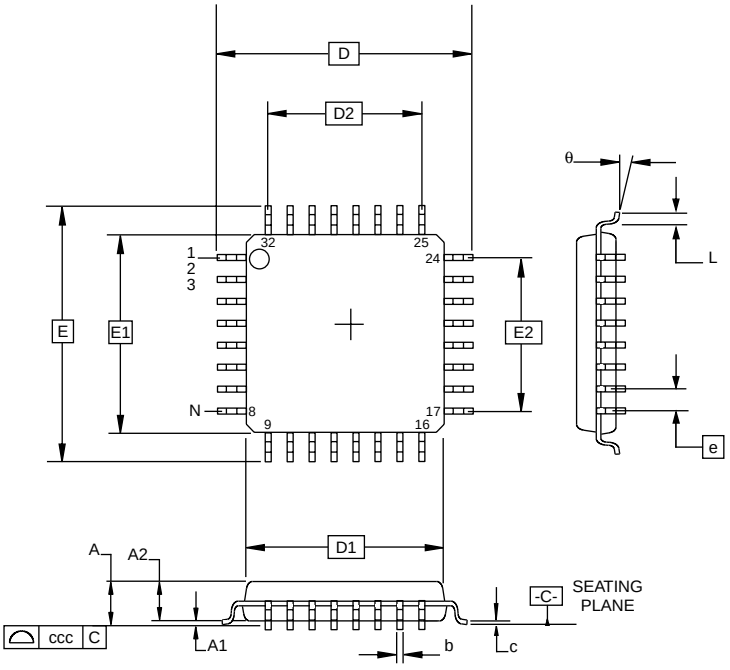


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8752BY	ICS8752BY	32 Lead LQFP	250 per tray	0°C to 70°C
ICS8752BYT	ICS8752BY	32 Lead LQFP on Tape and Reel	1000	0°C to 70°C