

Quad/Five/Six Line ESD Protection Diode Array

UESD54B SC70-5/SC88A/SOT353

UESD55B SC89-6/SOT563/SOT666

UESD56B SC89-6/SOT563/SOT666

UESD57B DFN1616-6L

UESD64B SC89-5/SOT553/SOT665

General Description

The UESD54B/55B/56B/57B/64B of TVS diode array is designed to protect sensitive electronics from damage or latch-up due to ESD for use in applications where board space is at a premium. It is unidirectional device and may be used on lines where the signal polarities are above ground. The UESD54B/55B/64B will protect up to four lines, the UESD56B will protect up to five lines and the UESD57B will protect up to six lines.

TVS diodes are solid-state devices feature large cross-sectional area junctions for conducting high transient currents, specifically for transient suppression. It offers desirable characteristics for board level protection including fast response time, low operating, low clamping voltage, and no device degradation.

The UESD54B/55B/56B/57B/64B may be used to meet the immunity requirements of IEC 61000-4-2, level 4. The small package makes them ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras.

Applications

- Cellular Handsets & Accessories
- Cordless Phones
- Personal Digital Assistants (PDA's)
- Notebooks & Handhelds
- Portable Instrumentation
- Digital Cameras
- Peripherals
- MP3 Players

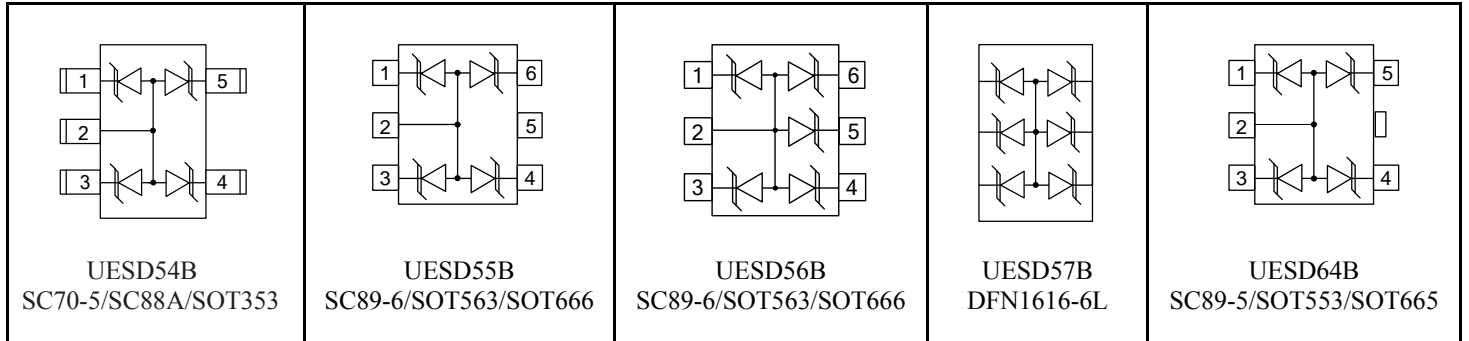
Features

- Transient protection for data & power lines to IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)
- Working Voltages: 5V
- Low Leakage current
- Low clamping voltage
- Solid-state silicon avalanche technology

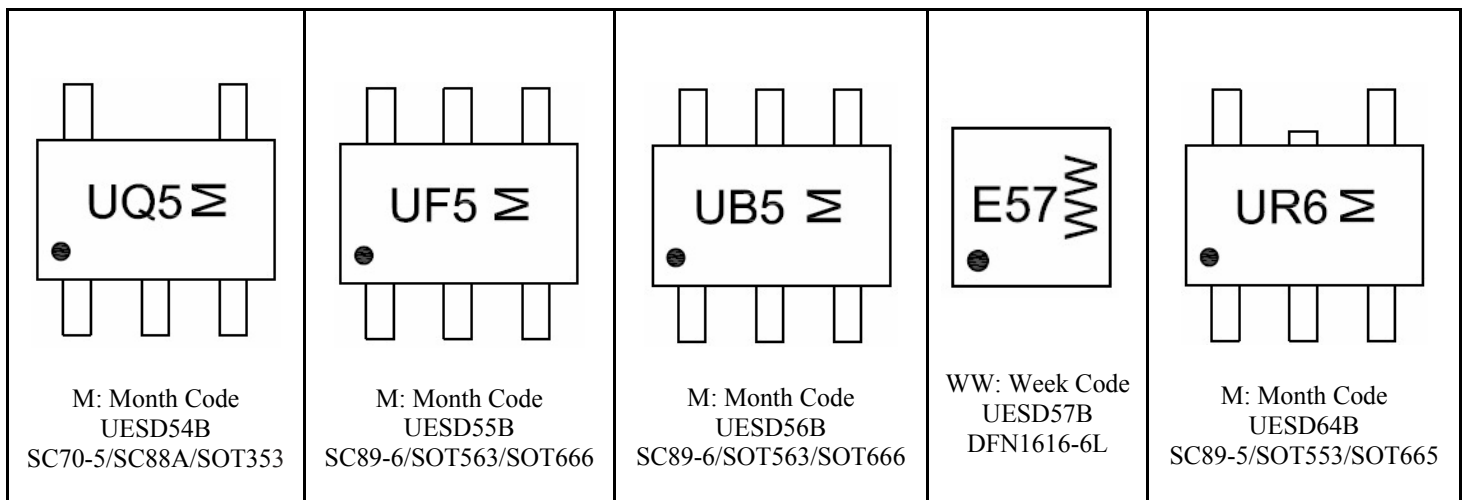
Ordering Information

Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UESD54B	5.0V	SC70-5/SC88A/SOT353	4	UQ5	3000pcs/ 7 Inch Reel
UESD55B	5.0V	SC89-6/SOT563/SOT666	4	UF5	
UESD56B	5.0V	SC89-6/SOT563/SOT666	5	UB5	
UESD57B	5.0V	DFN1616-6L	6	E57	
UESD64B	5.0V	SC89-5/SOT553/SOT665	4	UR6	

Pin Configurations



Top View



Absolute Maximum Ratings

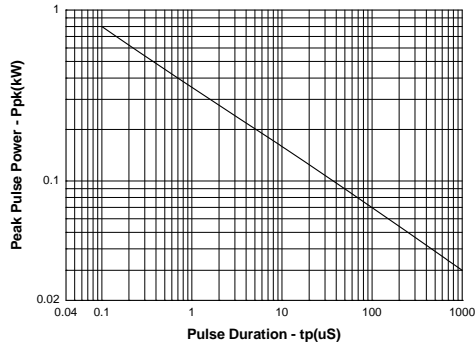
Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P _{PK}	140	Watts
Peak Pulse Current (tp = 8/20μs)	I _{PP}	11	A
Lead Soldering Temperature	T _L	260(10 sec.)	°C
Operating Temperature	T _J	-55 to +125	°C
Storage Temperature	T _{STG}	-55 to +125	°C

Electrical Characteristics

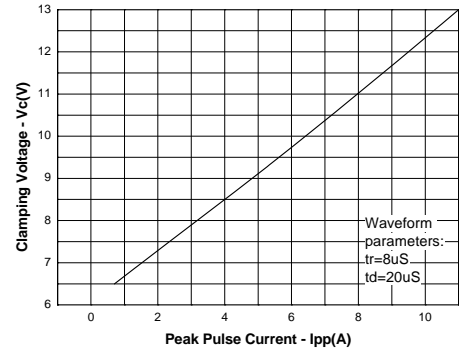
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V _{RWM}				5	V
Reverse Breakdown Voltage	V _{BR}	I _t = 1mA	6	6.8	7.2	V
Reverse Leakage Current	I _R	V _{RWM} = 5V, T=25°C			0.1	μA
Clamping Voltage	V _C	I _{PP} = 5A, t _p = 8/20μS			9.1	V
		I _{PP} = 11A, t _p = 8/20μS			13	
Junction Capacitance	C _J	Between I/O pins and GND V _R = 0V, f = 1MHz		40	50	pF
Junction Capacitance	C _J	Between I/O pins and GND V _R = 2.5V, f = 1MHz		30	40	pF

Typical Operating Characteristics

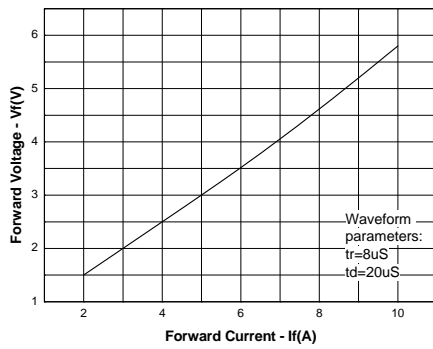
Non-Repetitive Peak Pulse Power vs. Pulse Time



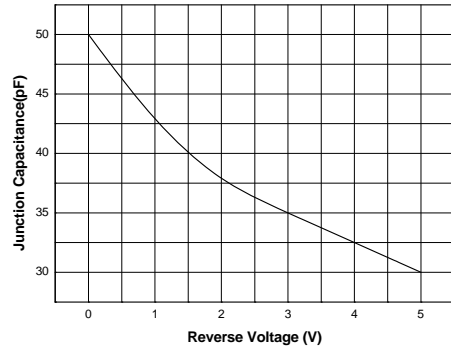
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



Junction Capacitance vs. Reverse Voltage



Applications Information

UESD54B/55B/56B/57B/64B ESD protection diode is designed to protect quad/five/six data, I/O, or power supply line. The device is unidirectional and may be used on lines where the signal polarity is above ground. The cathode should be placed towards the line that is to be protected.

Circuit Board Layout Recommendations for Suppression of ESD

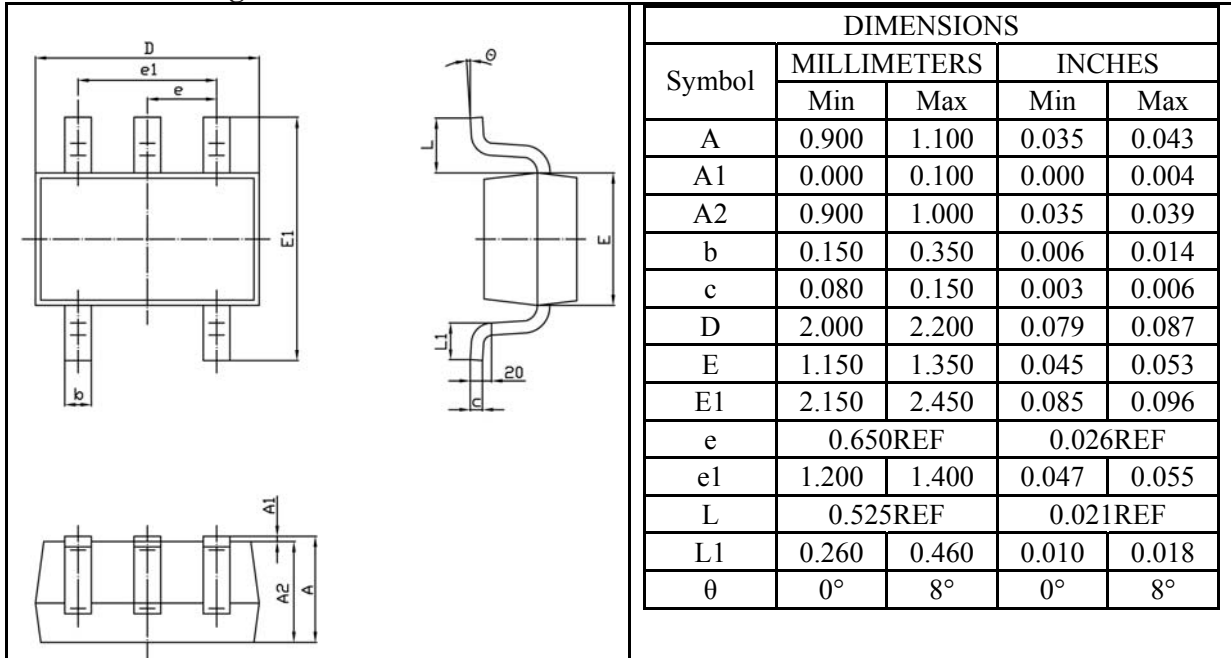
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the input terminals or connectors to restrict transient coupling.
2. Minimize the path length between the TVS and the protected line.
3. Minimize all conductive loops including power and ground loops.
4. The ESD transient return path to ground should be kept as short as possible.
5. Never run critical signals near board edges.
6. Use ground planes whenever possible. For multilayer printed-circuit boards, use ground vias.
7. Keep parallel signal paths to a minimum.
8. Avoid running protection conductors in parallel with unprotected conductor.
9. Minimize all printed-circuit board conductive loops including power and ground loops.
10. Avoid using shared transient return paths to a common ground point.

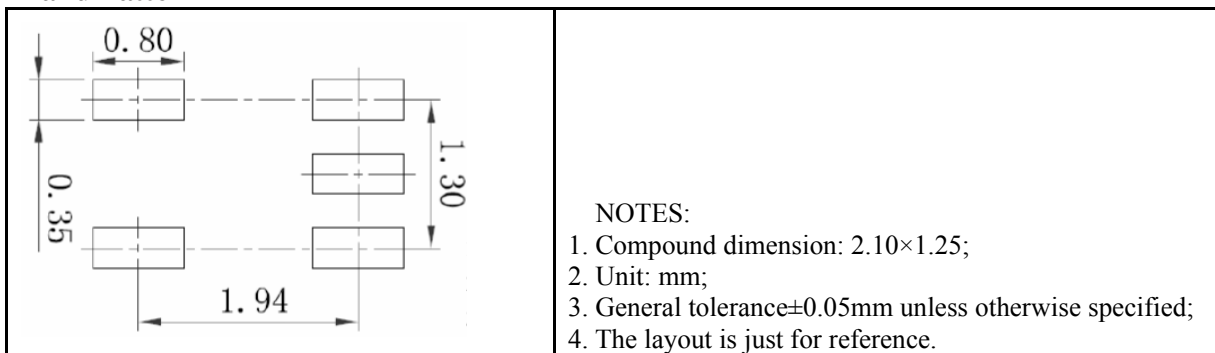
Package Information

UESD54B SC70-5/SC88A/SOT353

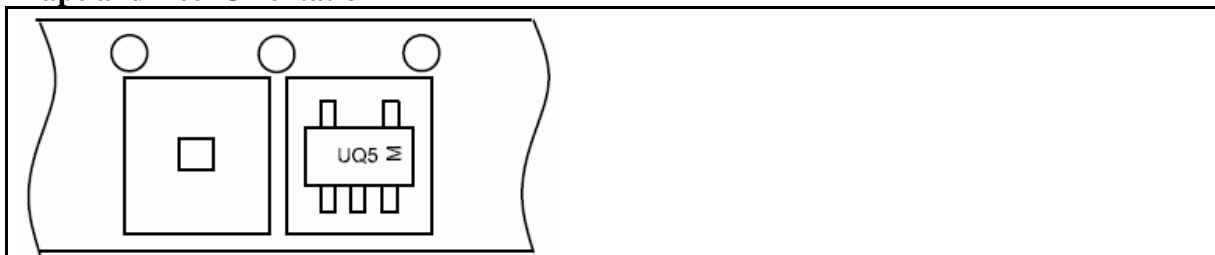
Outline Drawing



Land Pattern

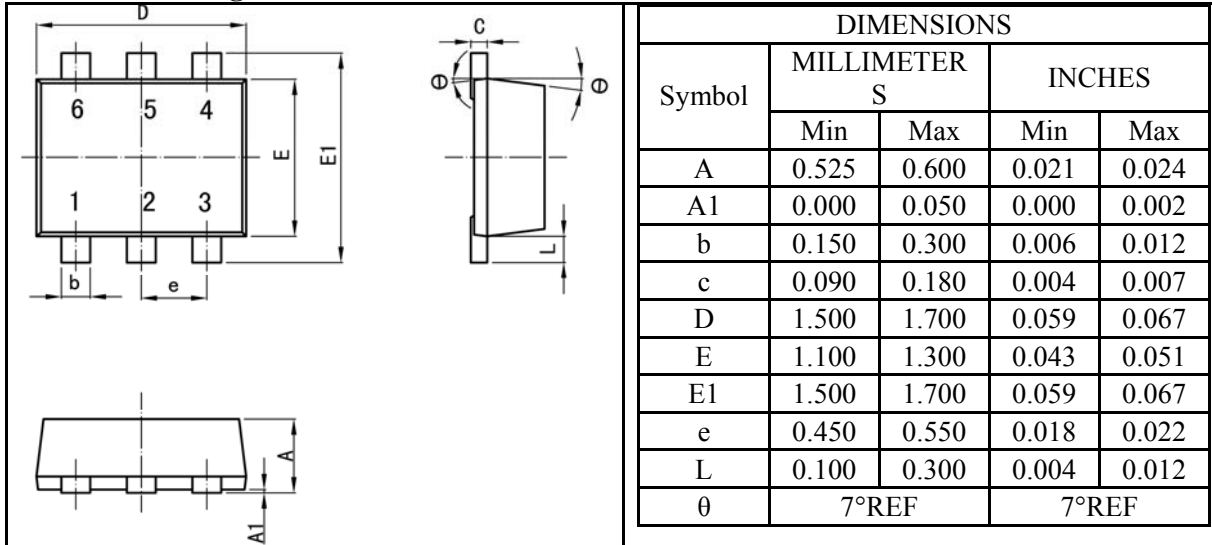


Tape and Reel Orientation

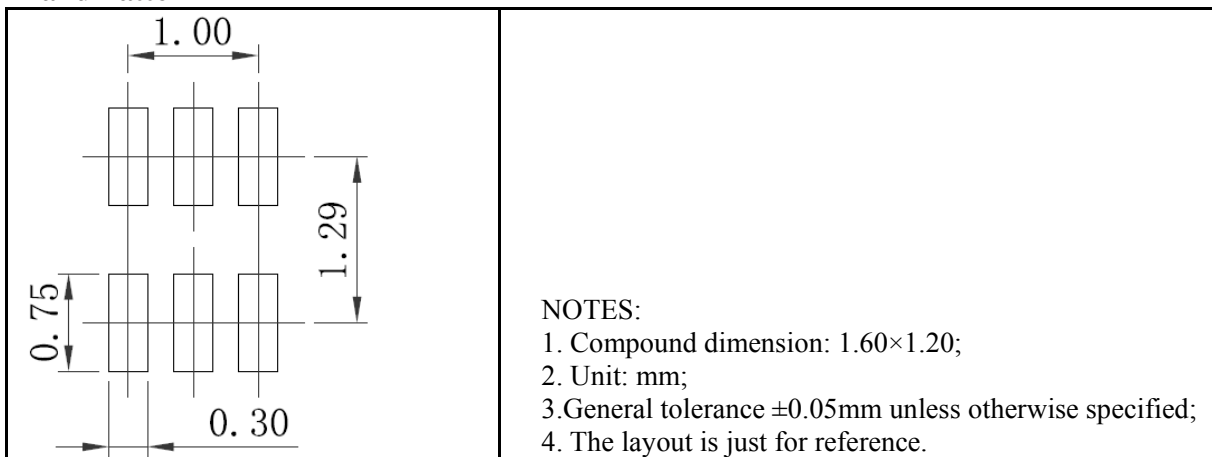


UESD55B SC89-6/SOT563/SOT666

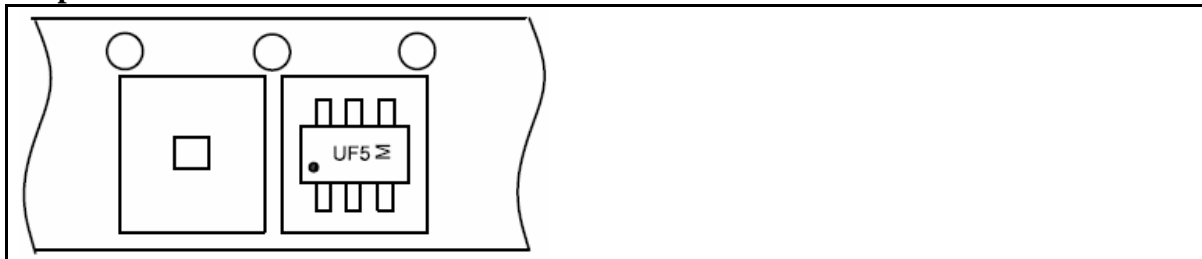
Outline Drawing



Land Pattern

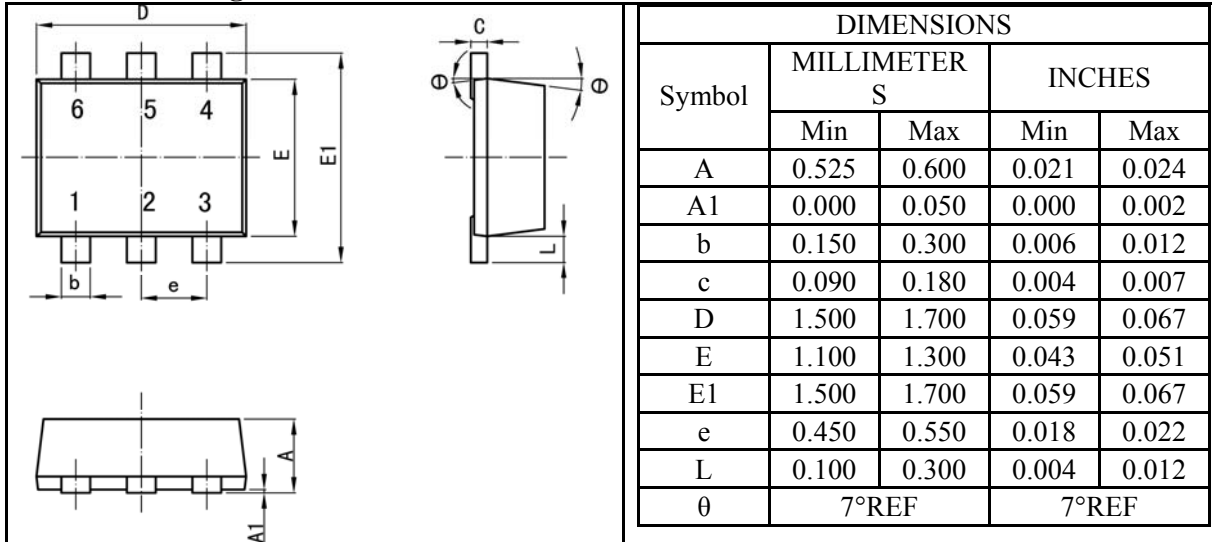


Tape and Reel Orientation

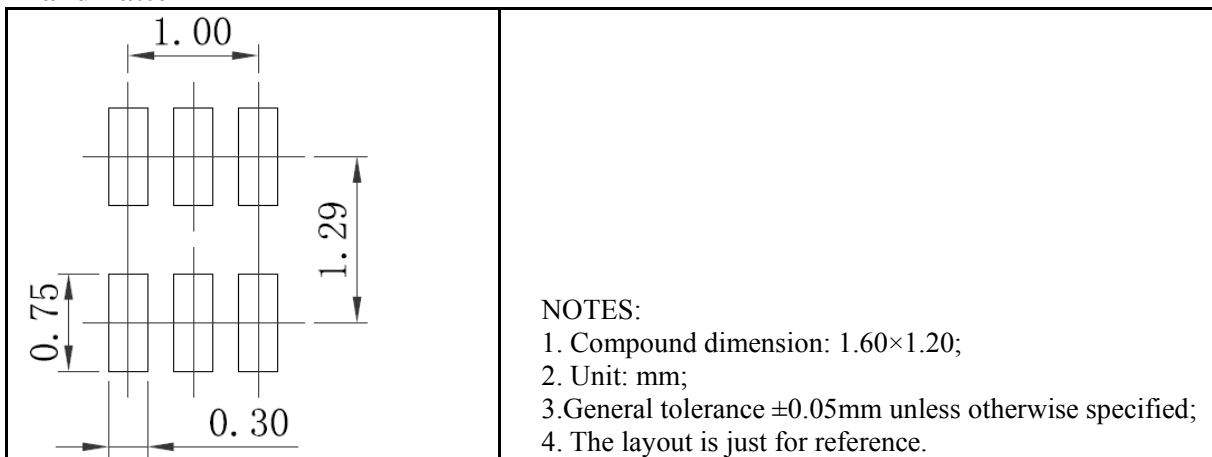


UESD56B SC89-6/SOT563/SOT666

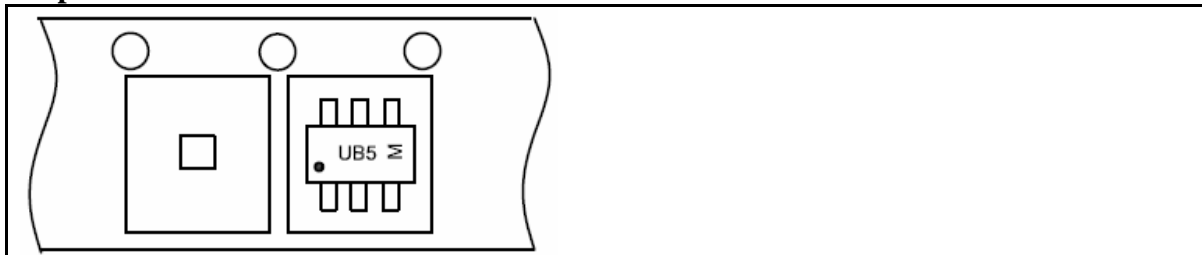
Outline Drawing



Land Pattern

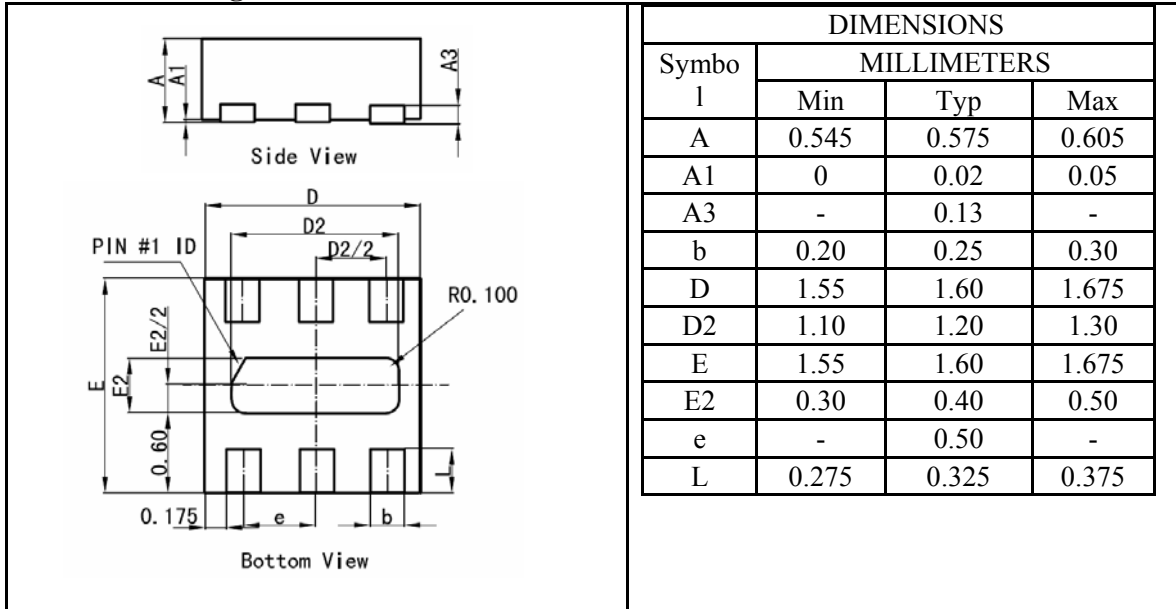


Tape and Reel Orientation

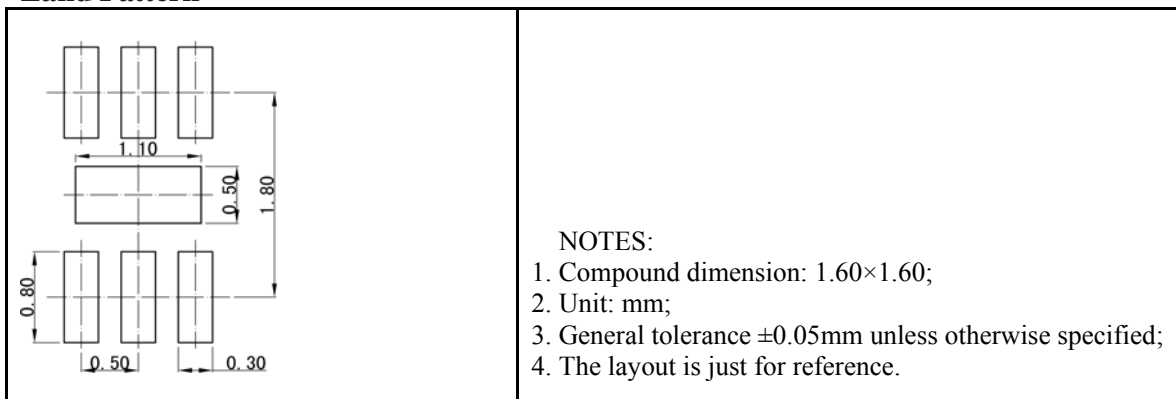


UESD57B DFN6 1.6×1.6

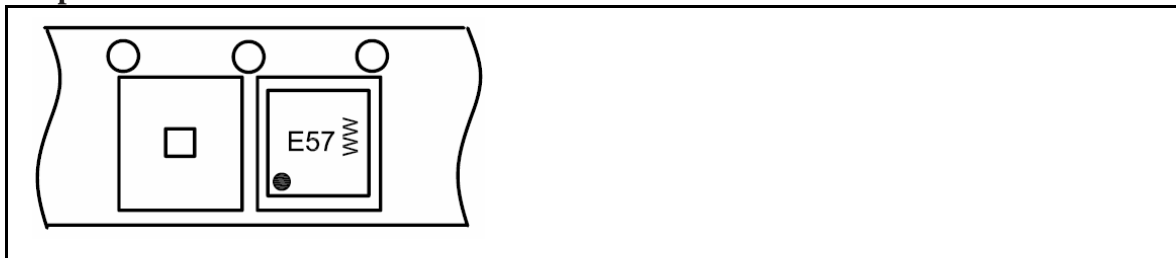
Outline Drawing



Land Pattern

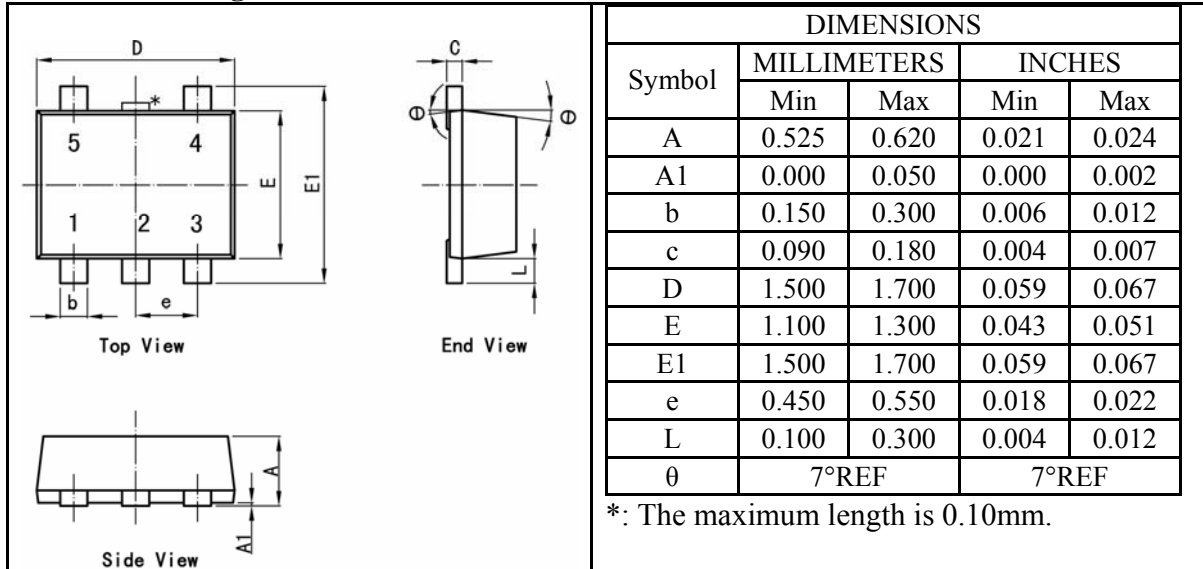


Tape and Reel Orientation

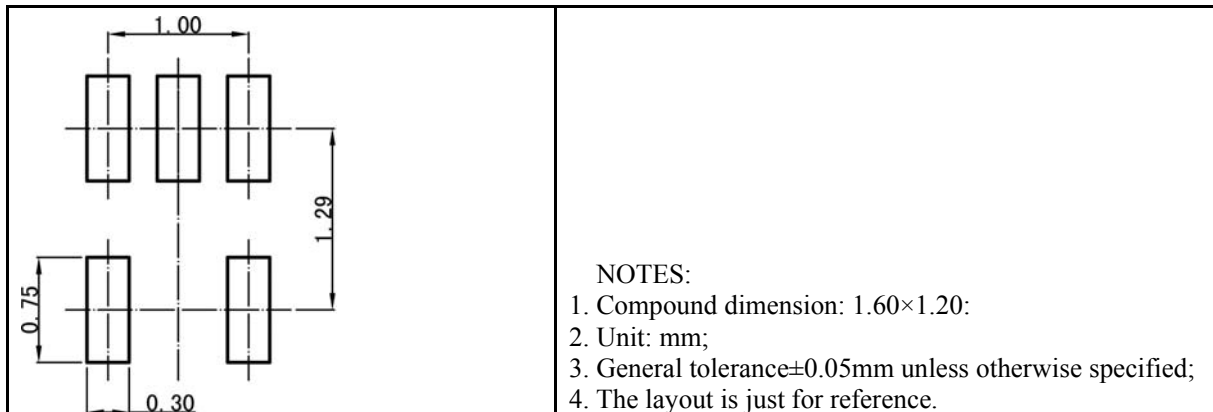


UESD64B SC89-5/SOT553/SOT665

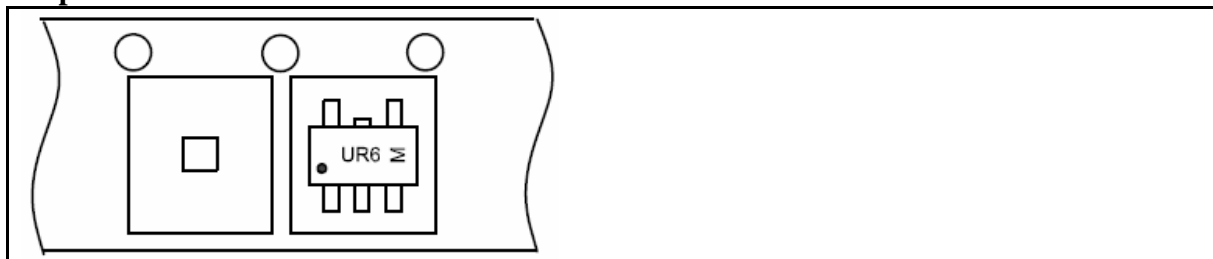
Outline Drawing



Land Pattern



Tape and Reel Orientation



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