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T2700 Series

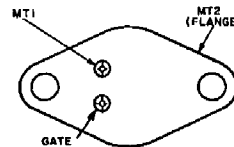
High Voltage, 6-A Silicon Triacs

For Power-Control and Power-Switching Applications

Features:

- 800V, 125 Deg. C T_J Operating
- High dv/dt and di/dt Capability
- Low Switching Losses
- High Pulse Current Capability
- Low Forward and Reverse Leakage
- Sipos Oxide Glass Multilayer Passivation System
- Advanced Unisurface Construction
- Precise Ion Implanted Diffusion Source

TERMINAL DESIGNATIONS



JEDEC TO-214AA

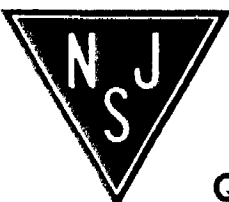
MAXIMUM RATINGS, Absolute-Maximum Values:

	T2700B	T2700D	T2700M	T2700N	
V_{DRM}°	200	400	600	800	V
$I_{T(RMS)} (T_C = 100^{\circ}C)$			8		A
I_{TSM} (for 1 full cycle) 60 Hz			100		A
di/dt			100		A/ μ s
I^2T (at 1.25 to 10 ms)			50		A ² s
I_{GTM}^{\square}			4		A
P_{GM} (for 1 μ s max.)			16		W
$P_{G(AV)}$ (Averaging time 10ms max.)			0.2		W
T Storage \blacktriangle			-65 to 150		$^{\circ}C$
T_C			-65 to 125		$^{\circ}C$
T_r (During soldering): For 10 s max. (terminals and case)			225		$^{\circ}C$

\circ For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

\square For either polarity of gate voltage (V_G) with reference to main terminal 1.

\blacktriangle For temperature measurement reference point, see *Dimensional Outline*.



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Quality Semi-Conductors

T2700 Series

ELECTRICAL CHARACTERISTICS

At Maximum Ratings and at Indicated Case Temperature (T_C) Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	LIMITS			UNITS
		For All Types Unless Otherwise Specified			
		Min.	Typ.	Max.	
Peak Off-State Current: [*] Gate open, $T_J = 125^\circ\text{C}$, $V_{DROM} = \text{Max. rated value}$	I_{DROM}	—	0.1	4	mA
Maximum On-State Voltage: [*] For $I_T = 30\text{A (peak)}$, $T_C = 25^\circ\text{C}$	V_{TM}	—	1.8	2.25	V
DC Holding Current: [*] Gate open, Initial principal current = 150 mA (DC), $v_D = 12\text{V}$; $T_C = 25^\circ\text{C}$	I_{HO}	—	15	30	mA
See Fig. 5					
Critical Rate-of-Rise of Commutation Voltage: [*] For $V_D = V_{DROM}$, $I_{TRMS} = 6\text{A}$, Commutating $di/dt = 3.2\text{A/ms}$, and gate unenergized At $T_C = +100^\circ\text{C}$	dv/dt	3	10	—	V/ μs
Critical Rate of Rise of Off-State Voltage: [*] For $V_D = V_{DROM}$, exponential voltage rise, and gate open At $T_C = 125^\circ\text{C}$					
T2500B	dv/dt	30	150	—	V/ μs
T2500D		20	100	—	
T2500M		15	70	—	
T2500N		10	50	—	
DC Gate-Trigger Current: ^{*†} For $v_D = 12\text{ volts (dc)}$, $R_L = 30\ \Omega$, $T_C = +25^\circ\text{C}$, and Specified Triggering Mode:					
I ⁺ Mode: V_{MT2} positive, V_G positive	I_{GT}	—	15	25	mA
III ⁻ Mode: V_{MT2} negative, V_G negative		—	20	30	
I ⁻ Mode: V_{MT2} positive, V_G negative		—	25	40	
III ⁺ Mode: V_{MT2} negative, V_G positive		—	25	40	
See Figs. 7 & 8					
DC Gate-Trigger Voltage: ^{*†} For $v_D = 12\text{ V (DC)}$, $R_L = 30\ \Omega$ $T_C = 25^\circ\text{C}$	V_{GT}	—	1	2.2	V
For other case temperatures		0.2	—	—	
See Fig. 9					
Gate-Controlled Turn-On Time: (Delay Time + Rise Time) For $V_D = V_{DROM}$, $I_G = 160\text{ mA}$, $t_r = 0.1\ \mu\text{s}$, $i_T = 10\text{ A (peak)}$, $T_C = 25^\circ\text{C}$ (See Fig. 15)	t_{GI}	—	2.2	—	μs
Thermal Resistance: Junction-to-Case (Steady-State)	R_{JA}	—	—	4	$^\circ\text{C/W}$
Junction-to-Case (Transient)		See Fig. 10			

^{*}For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

[†]For either polarity of gate voltage (V_G) with reference to main terminal 1.