MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

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by MCM317400C/D

4M x 4

MCM317400C
Fast Page Mode
2048 Cycle Refresh

Advance Information

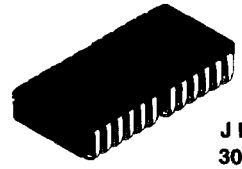
16M CMOS Dynamic RAM Family
Fast Page Mode 4M x 4

The family of 16M dynamic RAMs is fabricated using 0.5µ CMOS high–speed dynamic random access memories. They are organized as 4,194,304 four–bit words and fabricated using a double–layer metal process combined with twin–well CMOS technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

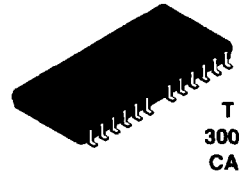
The MCM317400C requires only 11 address lines (2K refresh).

These devices are packaged in a standard 300 mil wide J–lead small outline package (SOJ) and a 300 mil wide thin–scale–outline package (TSOP).

- Three–State Data Outputs
- Fast Page Mode
- TTL–Compatible Inputs and Outputs
- $\overline{RAS}$–Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 2048 Cycle Refresh: MCM317400C = 32 ms
- Fast Access Time (t_{RAC}):
  MCM317400C–60 = 60 ns (Max)
  MCM317400C–70 = 70 ns (Max)
- Low Active Power Dissipation:
  MCM317400C–60 = 660 mW (Max)
  MCM317400C–70 = 580 mW (Max)
- Low Standby Power Dissipation:
  16M DRAM = 11 mW (Max, TTL Levels)
  16M DRAM = 5.5 mW (Max, CMOS Levels)



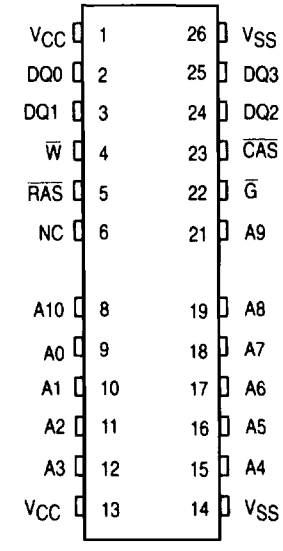
J PACKAGE
300 MIL SOJ
CASE 880A–02



T PACKAGE
300 MIL TSOP II
CASE 892A–02

PIN ASSIGNMENTS

300 MIL SOJ
300 MIL TSOP

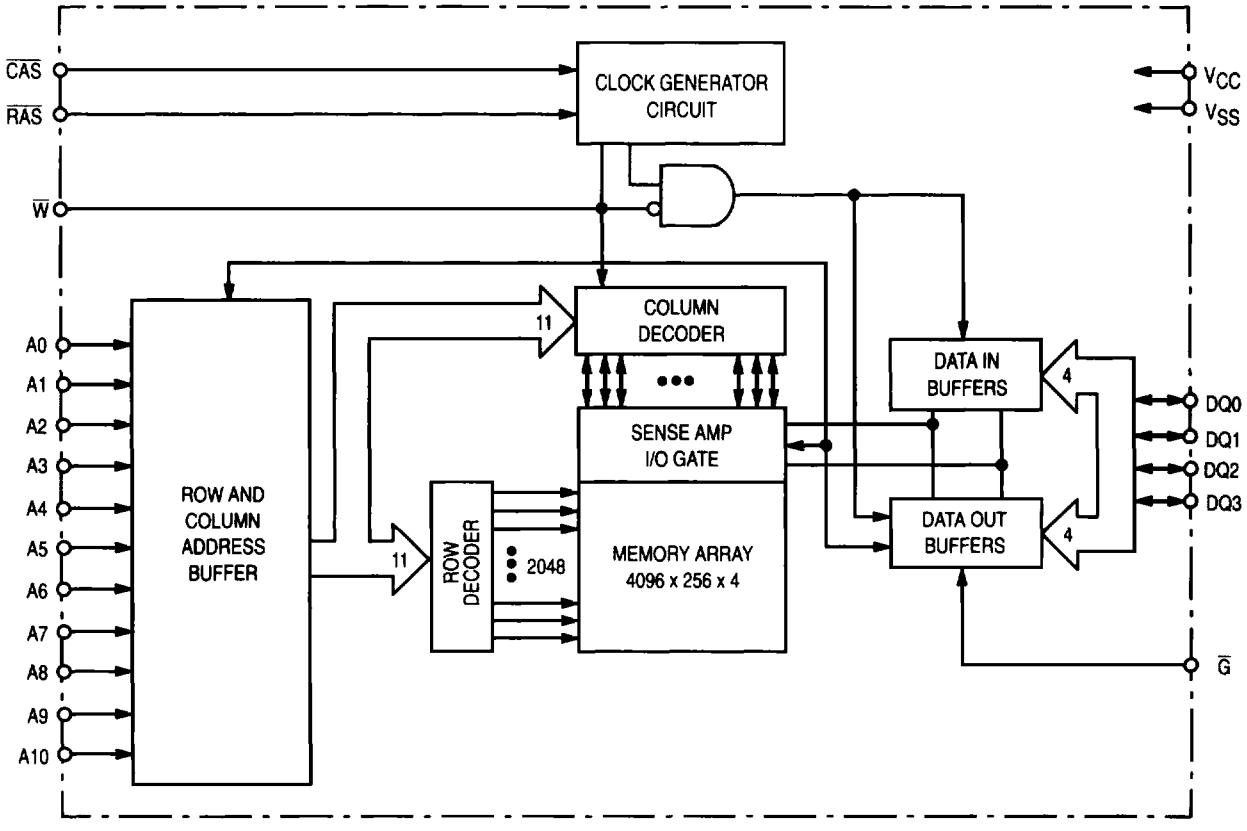


PIN NAMES	
A0 – A11 ..... Address Input	$\overline{RAS}$ ..... Row Address Strobe
DQ0 – DQ3 ..... Data Input/Output	$\overline{CAS}$ ..... Column Address Strobe
$\overline{G}$ ..... Output Enable	V_{CC} ..... Power Supply (+ 5 V)
$\overline{W}$ ..... Read/Write Enable	V_{SS} ..... Ground
NC ..... No Connection	

This document contains information on a new product. Specifications and information herein are subject to change without notice.

8/96

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current	I_{out}	50	mA
Power Dissipation	P_D	1000	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	5.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS (See notes 1 and 2)

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current (Operating)	MCM317400C–60, t_{RC} = 110 ns MCM317400C–70, t_{RC} = 130 ns	I_{CC1}	— —	120 105	mA	3, 4
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) Output Open		I_{CC2}	—	2	mA	
V_{CC} Power Supply Current During $\overline{RAS}$–Only Refresh Cycles ($\overline{CAS}$ = V_{IH}) Output Open	MCM317400C–60, t_{RC} = 110 ns MCM317400C–70, t_{RC} = 130 ns	I_{CC3}	— —	120 105	mA	3
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL}) ($\overline{CAS}$ cycling)s Output Open	MCM317400C–60, t_{PC} = 40 ns MCM317400C–70, t_{PC} = 45 ns	I_{CC4}	— —	70 60	mA	3, 4
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)		I_{CC5}	—	0.5	mA	
V_{CC} Power Supply Current During or $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle, Output Open	MCM317400C–60, t_{RC} = 110 ns MCM317400C–70, t_{RC} = 130 ns	I_{CC6}	— —	120 105	mA	3
Input Leakage Current (0 V ≤ V_{in} ≤ 6.0 V, Other Input Pins = 0 V)		$I_{lkg(I)}$	–10	10	µA	
Output Leakage Current (0 V ≤ V_{out} ≤ 5.5 V, Q Floating)		$I_{lkg(O)}$	–10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)		V_{OH}	2.4	V_{CC}	V	
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	0	0.4	V	

NOTES:
1. All voltage values are with respect to V_{SS}.
2. Current flowing into an IC is positive, out is negative.
3. I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV), and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (T_A = 0 to 70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Unless otherwise noted)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A11,	C_{in}	5	pF
	$\overline{G}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	
I/O Capacitance	DQ0 – DQ3	$C_{I/O}$	8	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

16M FAMILY AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

ALL DEVICES: READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM317400C–60		MCM317400C–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	ns	
Read–Write Cycle Time	t_{RELREL}	t_{RWC}	155	—	180	—	ns	21
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	ns	6, 8
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	15	—	20	ns	6, 7
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6, 10
$\overline{CAS}$ to Output in Low–Z	t_{CELQX}	t_{CLZ}	5	—	5	—	ns	6
Output Buffer and Turn–Off Delay	t_{CEHQZ}	t_{OFF}	0	15	0	15	ns	11
Transition Time (Rise and Fall)	t_T	t_T	1	50	1	50	ns	19
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	15	—	20	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	ns	

NOTES:

1. All voltage values are referenced to V_{SS}.
2. Current flowing into an IC is positive, out is negative.
3. I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV), and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5. An initial pause of 500 μ is required after power–up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$–only refresh).
6. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
7. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{ASC} \geq t_{ASC}$ (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{ASC}$ (max).
10. Assumes that $t_{CP} \leq t_{CP}$ (max) and $t_{ASC} \geq t_{ASC}$ (max).
11. t_{OFF} (max) and t_{GZ} (max) defines the time at which the output achieves the high impedance state ($I_{out} \leq 10$ μA) and is not referenced to V_{OH} (min) or V_{OL} (max).
12. The timing requirements are assumed t_T = 5.0 ns.
13. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
14. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is less than t_{RCD} (max), access time is t_{RAC}. If $t_{RCD} > t_{RCD}$ (max), access time is controlled by t_{CAC} or t_{AA}. t_{RCD} (min) is specified as t_{RCD} (min) = t_{RAH} (min) + 2t_H + t_{ASC} (min).
15. t_{RAD} (max) is specified as a reference point only. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{ASC}$ (max), access time is controlled exclusively by t_{AA}.
16. t_{ASC} (max) is specified as a reference point only. If $t_{RCD} \geq t_{RCD}$ (max) and $t_{ASC} \geq t_{ASC}$ (max), access time is controlled exclusively by t_{CAC}.
17. Either t_{DZC} or t_{DZO} must be satisfied.
18. Either t_{CDD} or t_{ODD} must be satisfied.
19. t_T is measured between V_{IH} (min) and V_{IL} (max).
20. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
21. t_{RWC} is specified as t_{RWC} (min) = t_{RAC} (max) + t_{ODD} (min) + t_{RWL} (min) + t_{RP} (min) + 5t_T.
22. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are specified as reference points only if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the DQ pins remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (for fast page mode cycle only), the cycle is a read–modify–write cycle and the DQ pins will contain the data read from the selected address. If neither of these conditions are met; delayed write or at access time and until $\overline{CAS}$ or OE goes back to V_{IH}, DQ is indeterminate.
23. All previously specified timing requirements and switching characteristic are applicable to their respective fast page mode cycle.
24. t_{RAS} (min) is specified as two cycles of $\overline{CAS}$ input are performed.
25. t_{CP} (max) is specified as a reference point only.
26. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

ALL DEVICES, READ, WRITE, AND READ–WRITE CYCLES (Continued)

Parameter	Symbol		MCM317400C–60		MCM317400C–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	t_{CEHREH}	t_{RHCP}	35	—	40	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	15	10 k	20	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	45	20	50	ns	14
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	ns	15
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	15	10	15	ns	25
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	10	0	10	ns	16
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	20
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	10	—	10	—	ns	20
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	10	—	10	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	10	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	15	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	15	—	20	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	—
Data In Hold Time	t_{CELDX}	t_{DH}	10	—	15	—	ns	—
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	22
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	40		45		ns	22
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	85	—	95	—	ns	22
Column Address to Write Delay	t_{AVWL}	t_{AWD}	55	—	60	—	ns	22
Refresh Period	t_{RVRV}	t_{RFSH}	—	32	—	32	ms	
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	10	—	15	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
Delay Time, Data to $\overline{CAS}$ Low		t_{DZC}	0	—	0	—	ns	17
Delay Time, Data to $\overline{G}$ Low		t_{DZO}	0	—	0	—	ns	17
Delay Time, $\overline{G}$ High to Data		t_{CDD}	15	—	15	—	ns	18
Delay Time, $\overline{G}$ High to Data		t_{ODD}	15	—	15	—	ns	18

DEVICE–SPECIFIC AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

4M x 4 CONFIGURATION–SPECIFIC READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM317400C–60		MCM317400C–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	15	—	20	—	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	—	15	—	20	ns	5
$\overline{G}$ to Data Delay	t_{GLHDX}	t_{GD}	15	—	15	—	ns	7
Output Buffer Turn–Off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	15	0	15	ns	6
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	15	—	15	—	ns	

NOTES:
1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 500 µs is required after power–up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
6. t_{OFF} (max) and/or t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Either t_{CDD} or t_{ODD} must be satisfied.

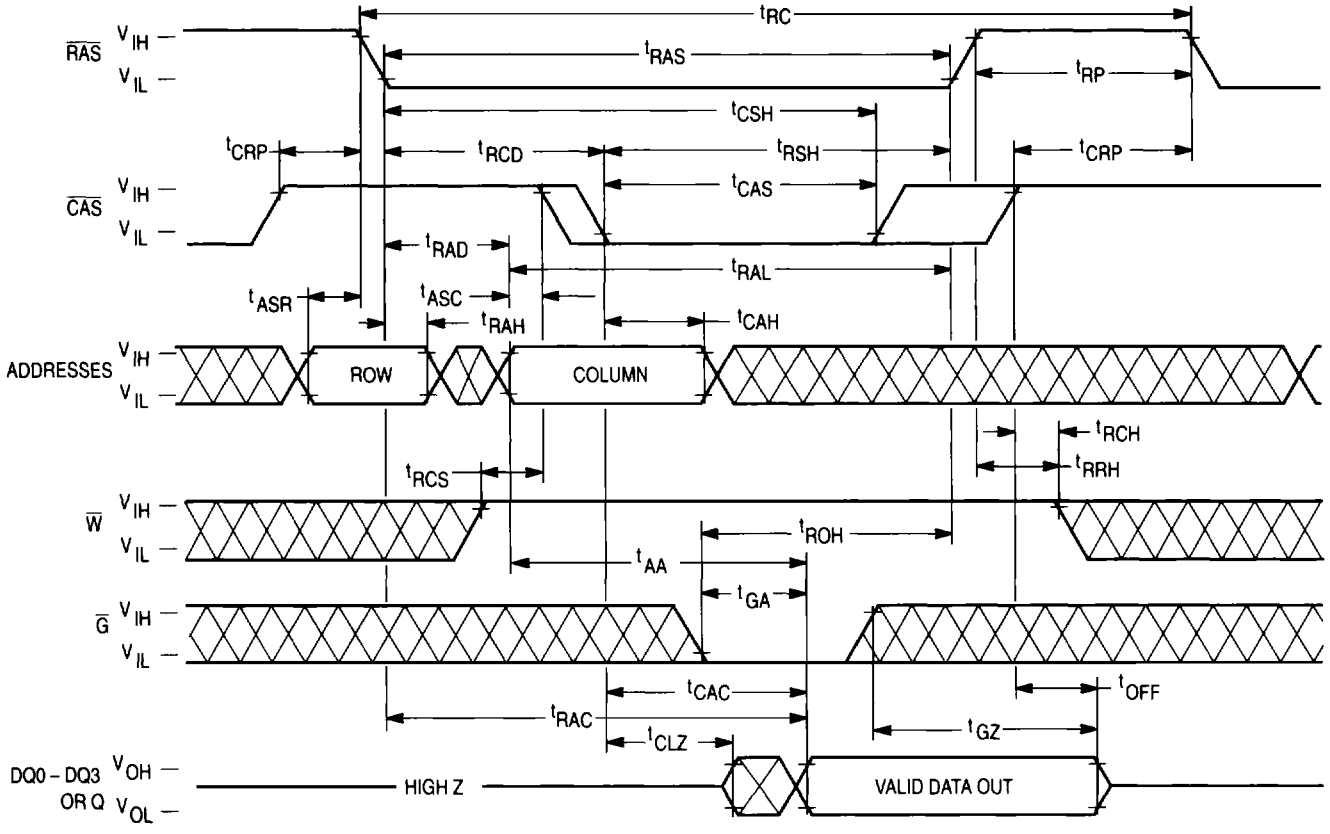
FAST PAGE MODE READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM317400C–60		MCM317400C–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time (Fast Page Mode)	t_{CEHREH}	t_{RHCP}	35	—	40	—	ns	
Fast Page Mode Read–Write Cycle Time	t_{CELCEL}	t_{PRWC}	85	—	95	—	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	100	125 k	115	125 k	ns	6
$\overline{CAS}$ Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	60	—	65	—	ns	5

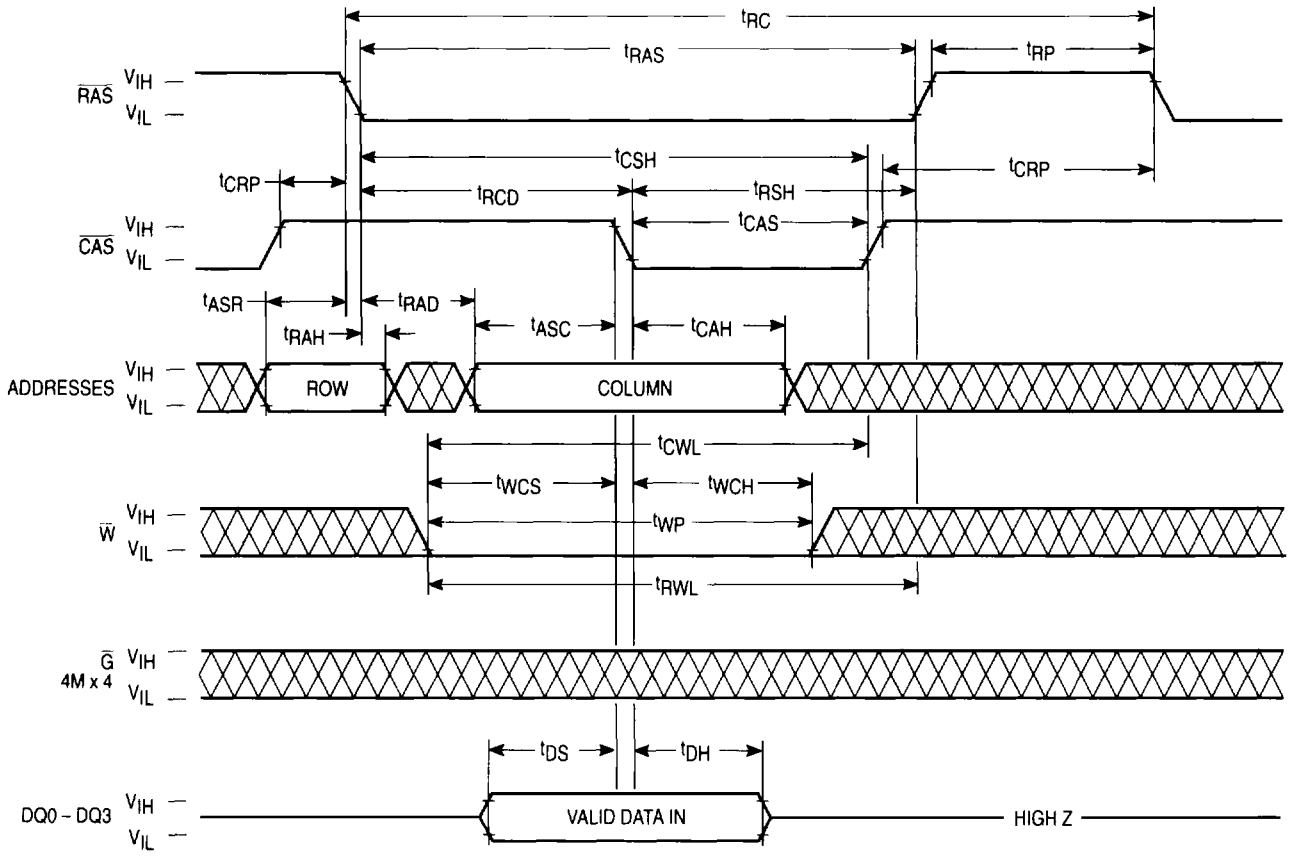
NOTES:
1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 500 µs is required after power–up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through–out the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read–write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
6. t_{RAS} (min) is specified as two cycles of $\overline{CAS}$ input are performed.

TIMING DIAGRAMS

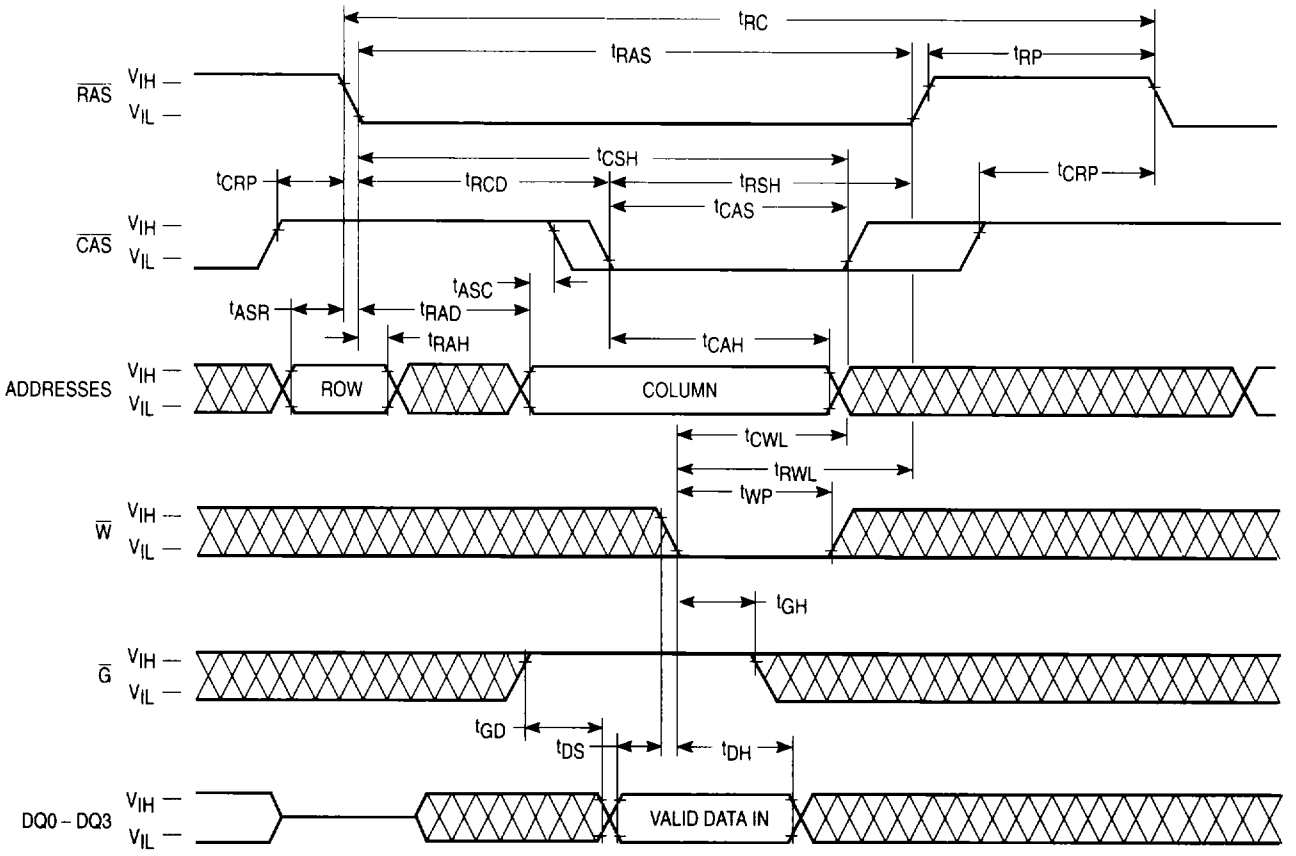
PAGE MODE READ CYCLE



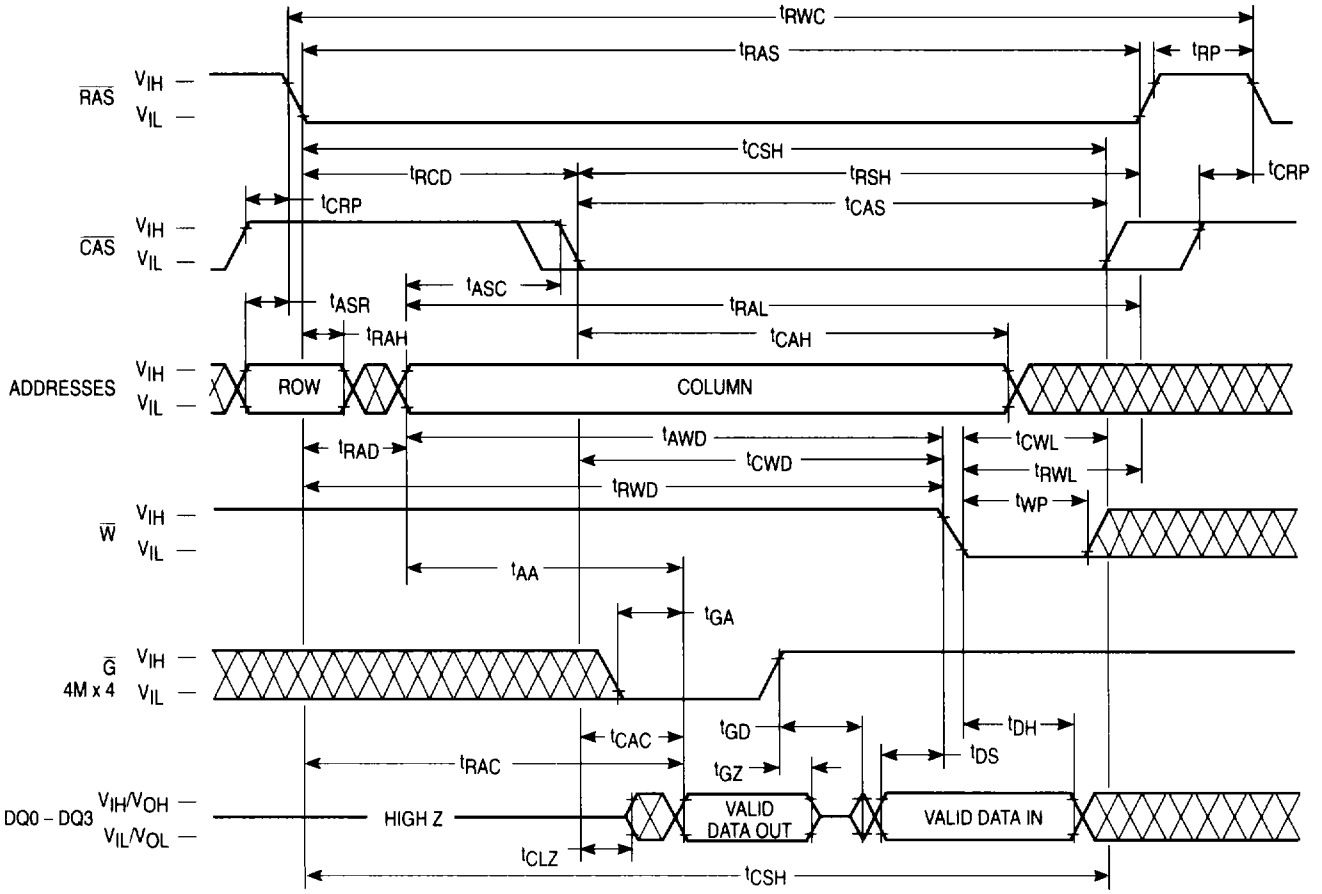
EARLY WRITE CYCLE



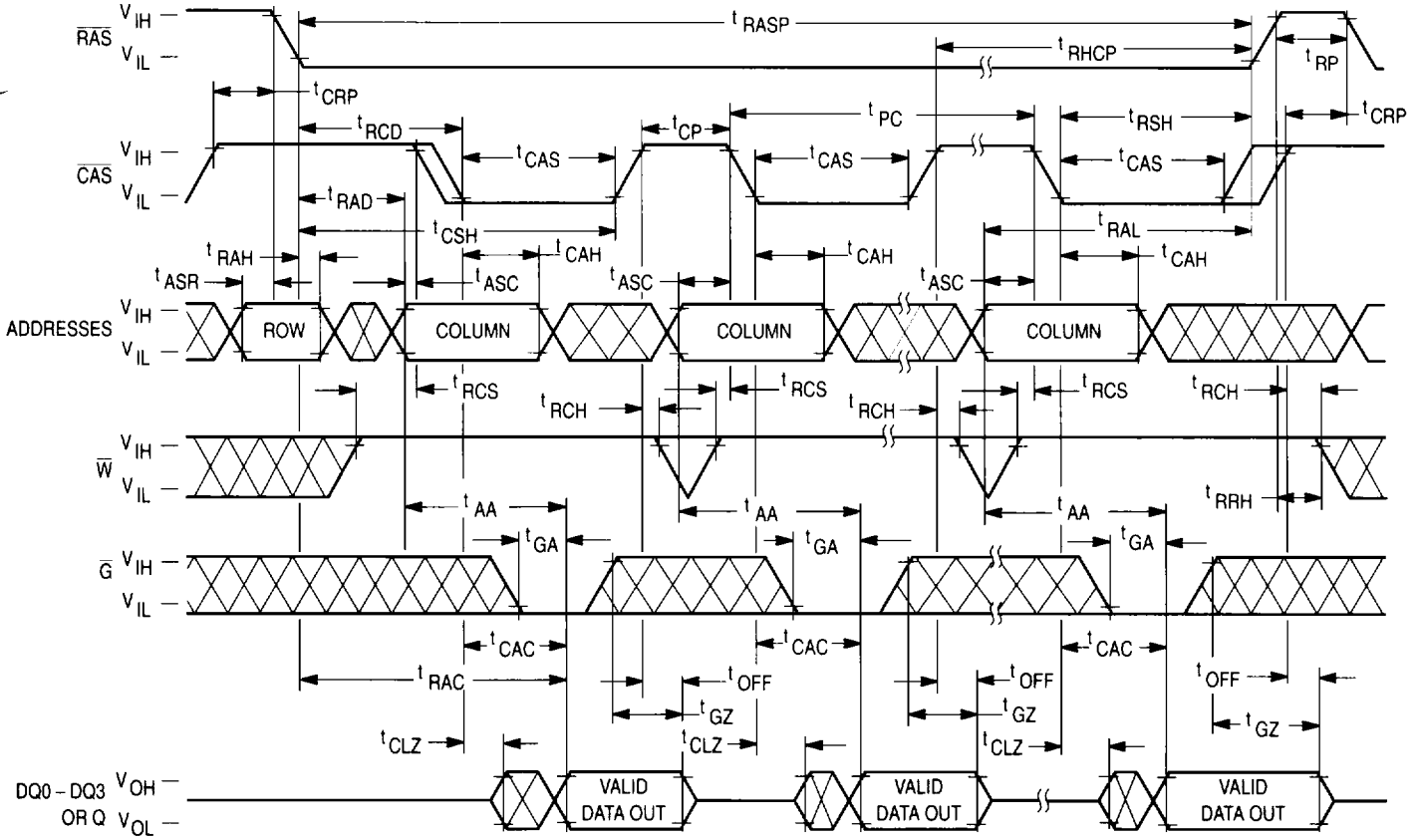
$\overline{G}$ CONTROLLED LATE WRITE CYCLE



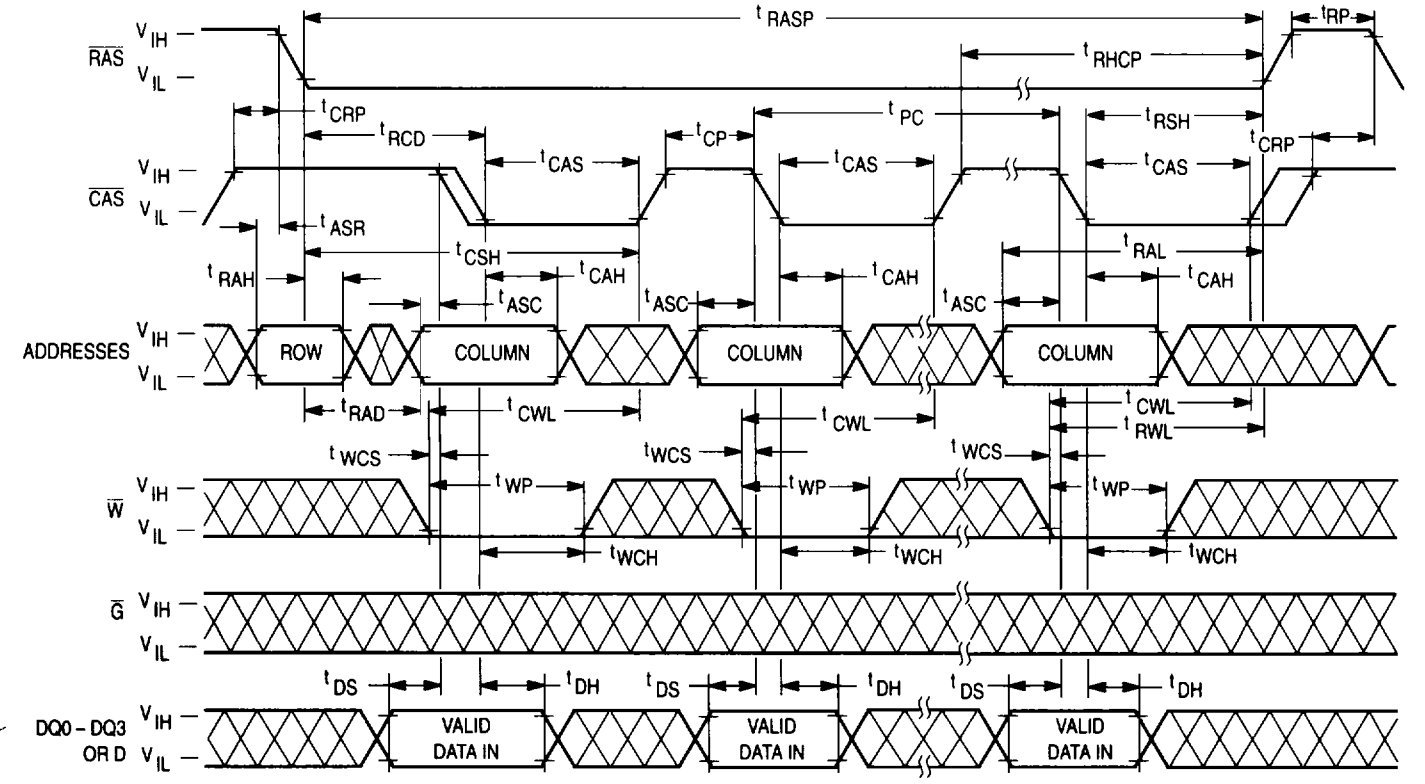
READ – WRITE CYCLE



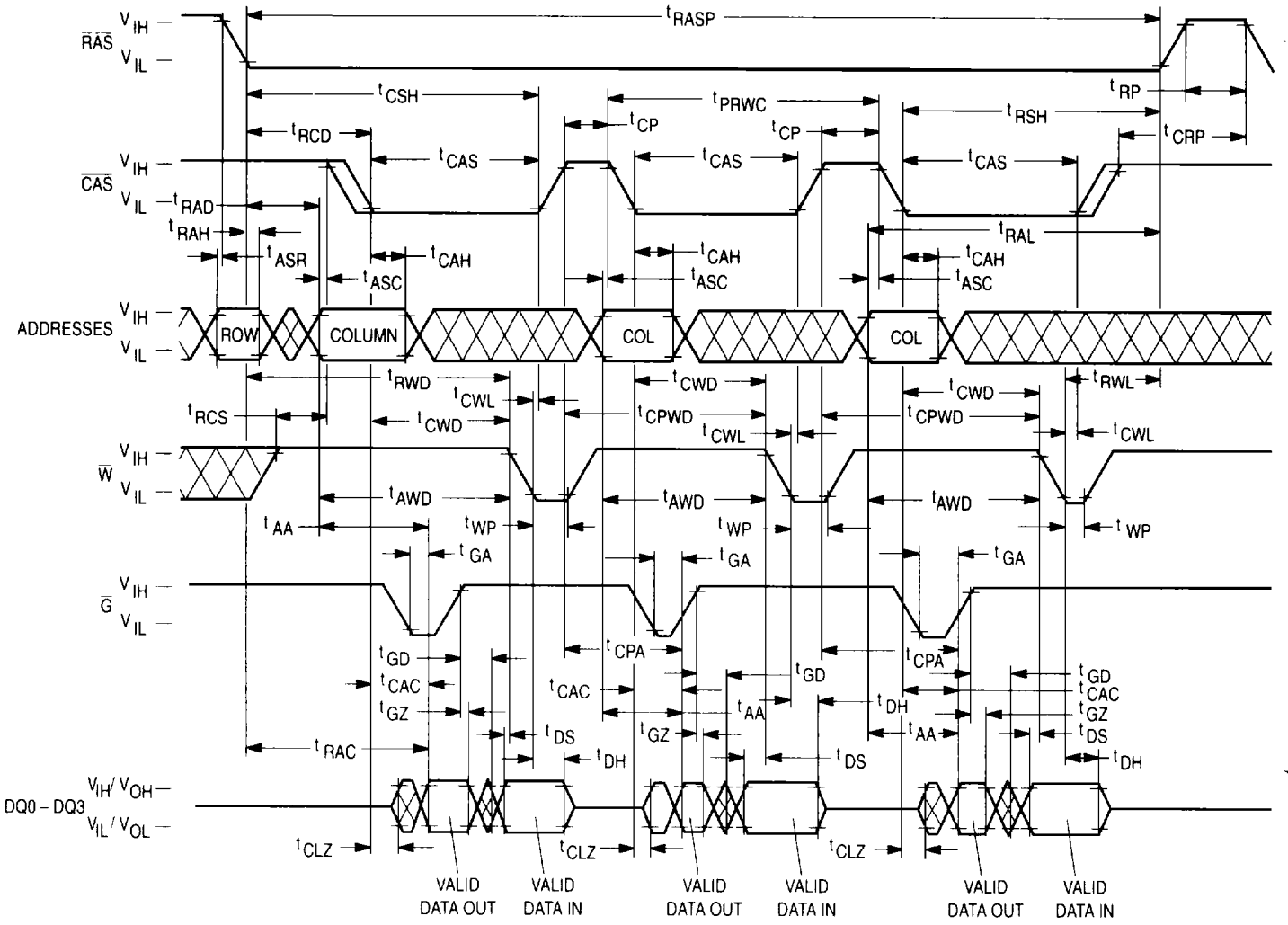
FAST PAGE MODE READ CYCLE



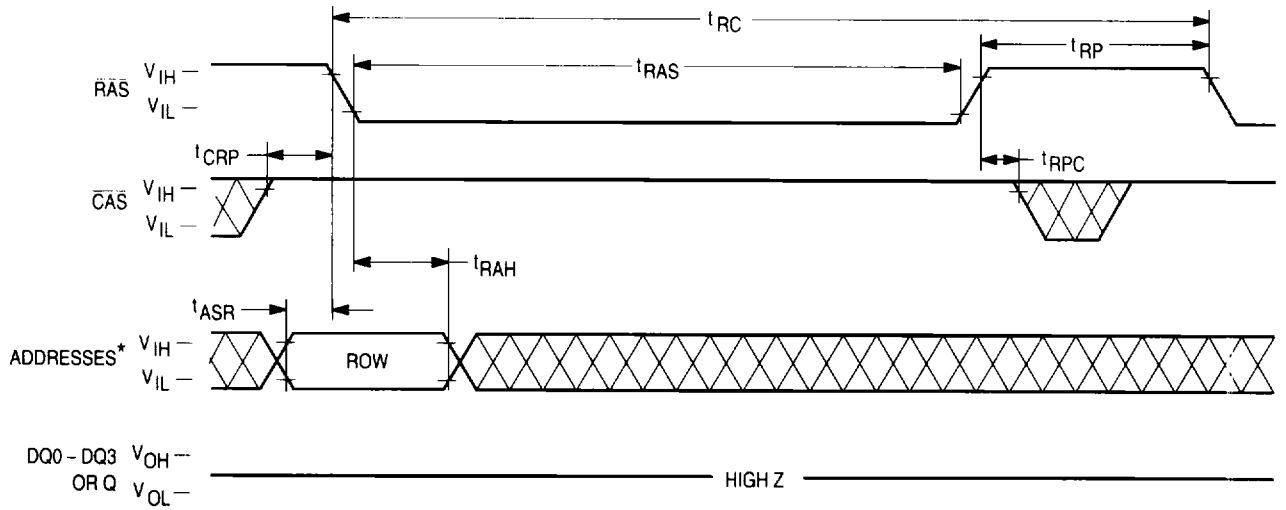
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ – WRITE CYCLE



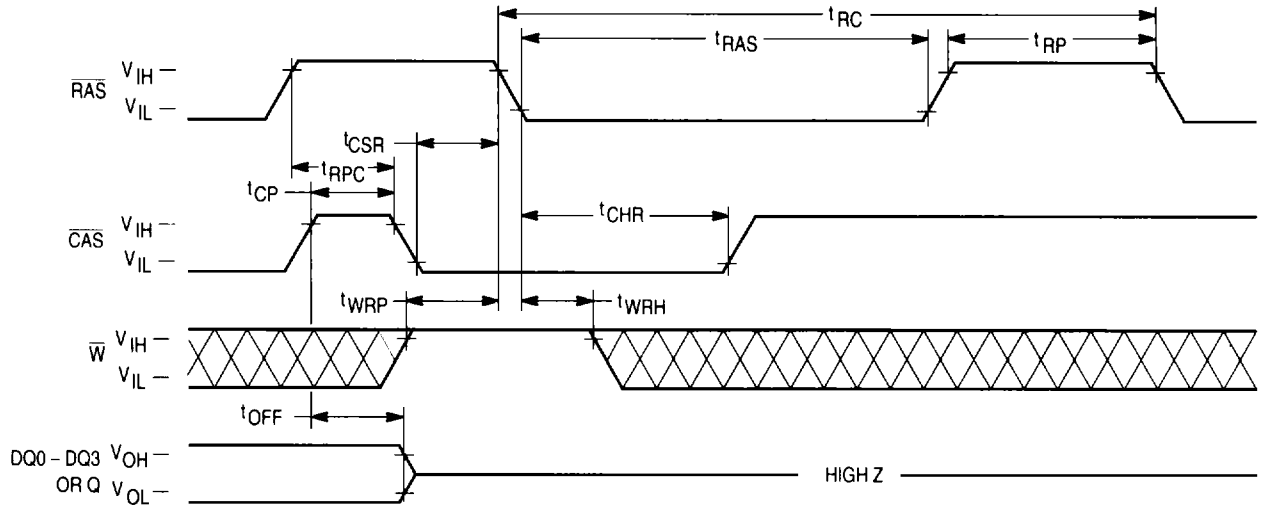
RAS ONLY REFRESH CYCLE
(W and G are Don't Care)



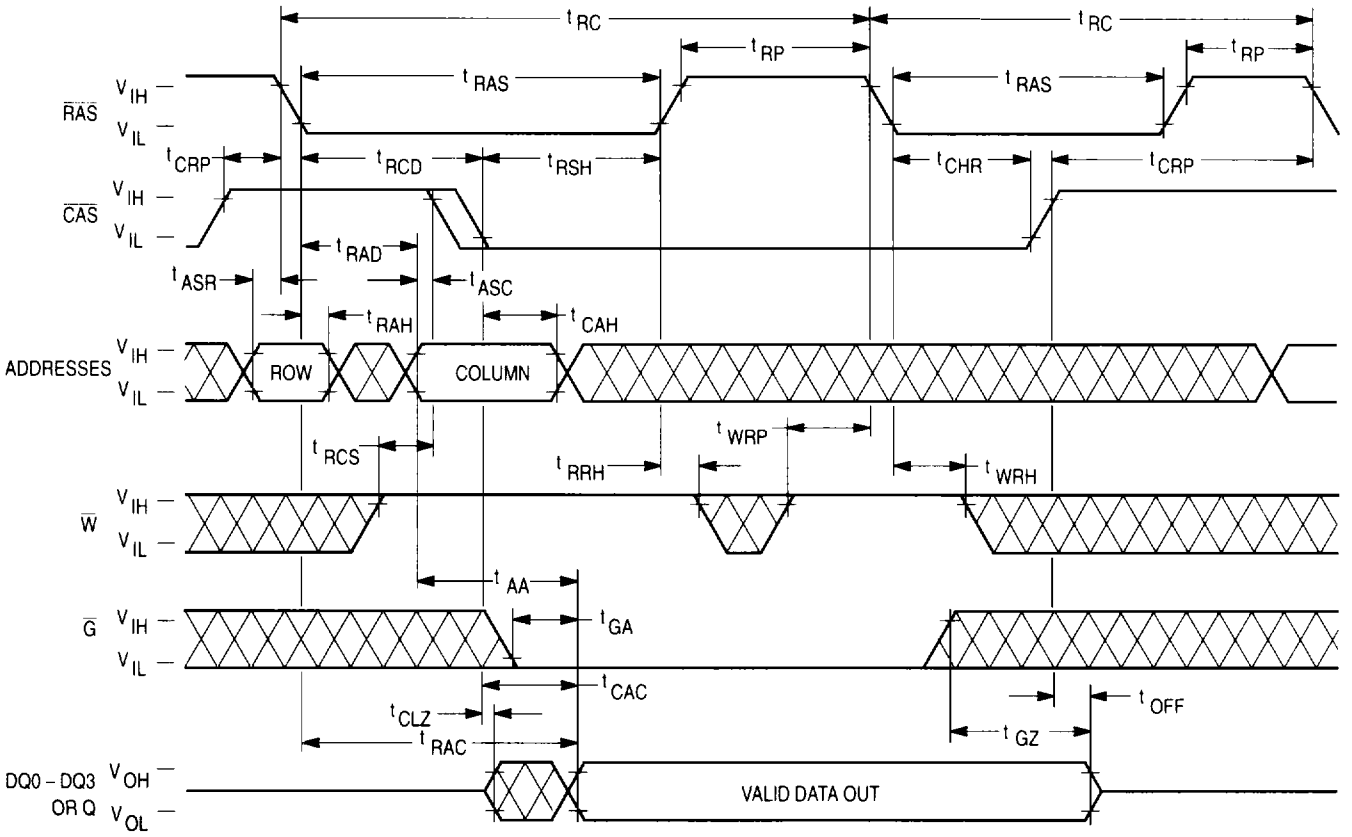
*MCM316xxxB – A0 – A11; MCM317400C – A0 – A10.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

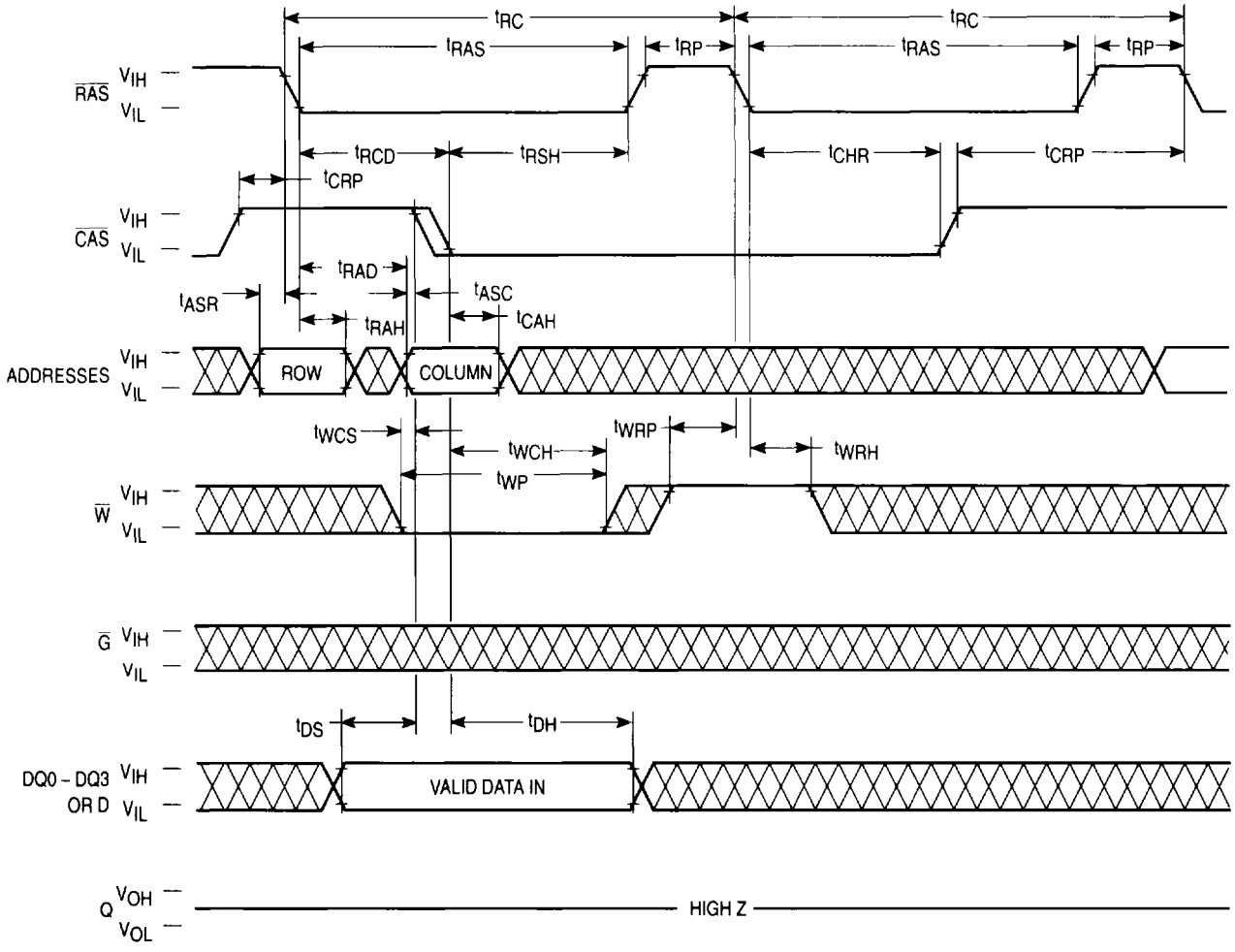
($\overline{G}$, D, and A0 – A10 or A11 are Don't Care)



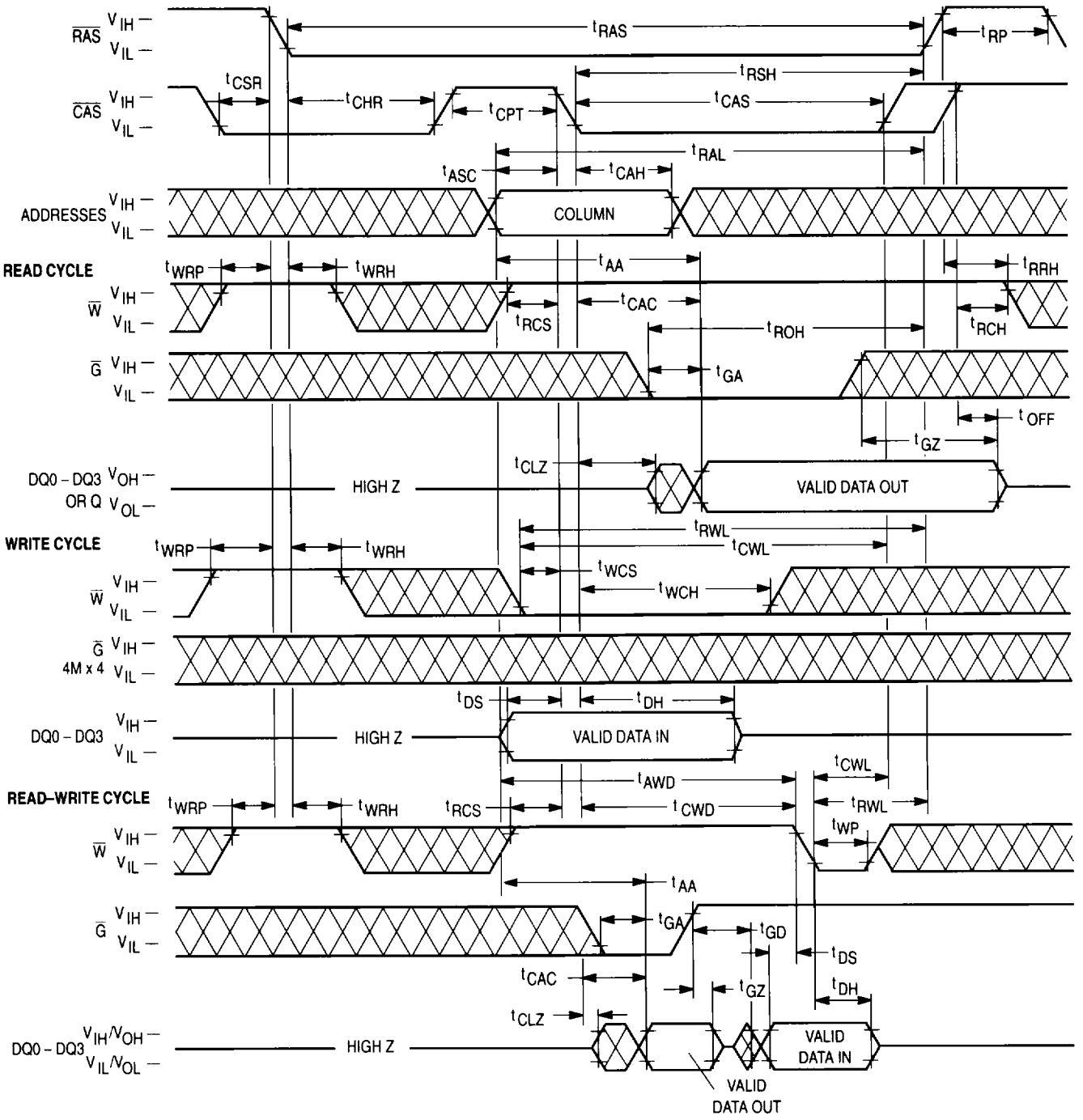
HIDDEN REFRESH CYCLE (READ)



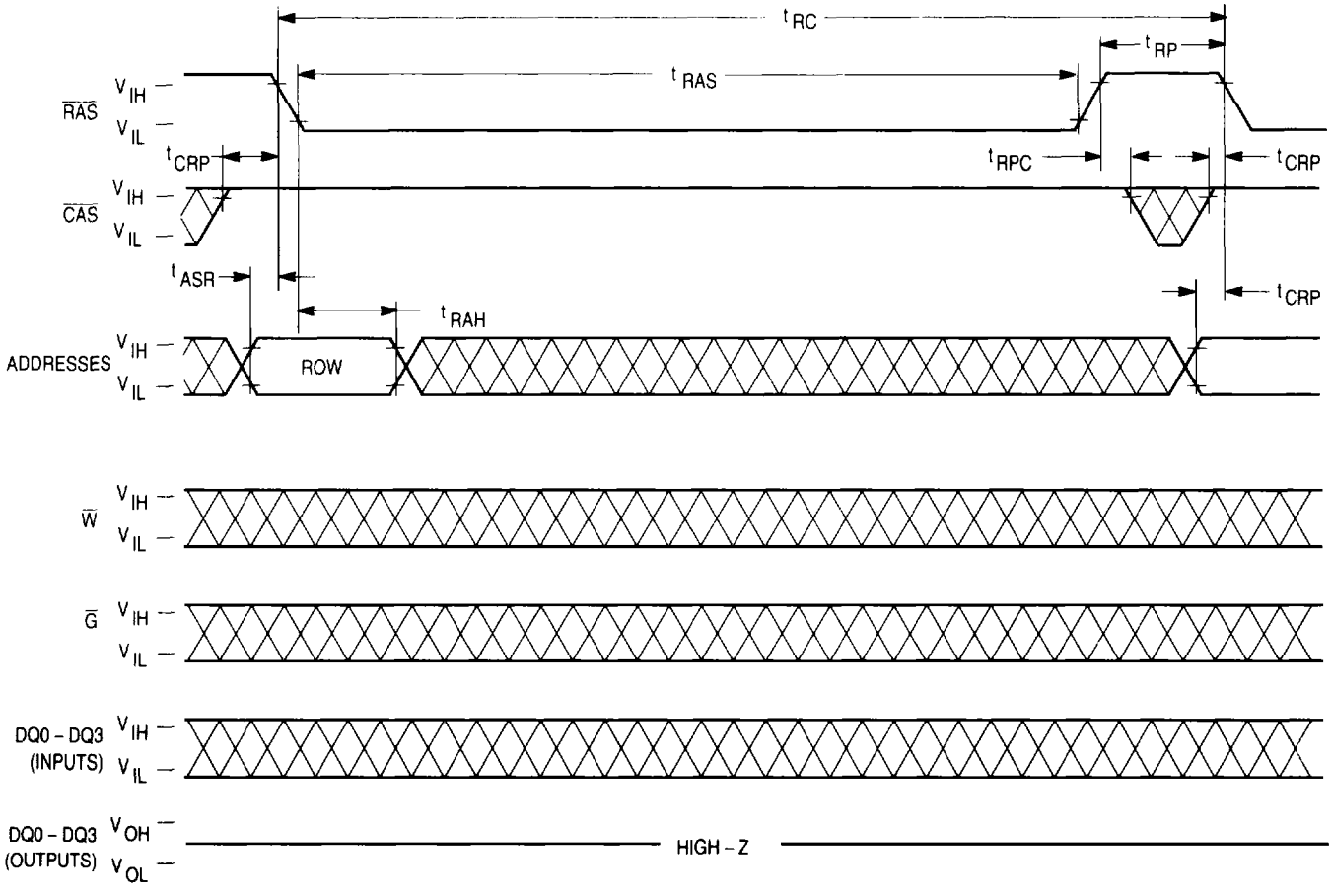
HIDDEN REFRESH CYCLE (EARLY WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE



DEVICE INITIALIZATION

On power–up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 32 milliseconds) a wakeup sequence of eight active cycles is necessary to ensure proper operation.

MCM317400C: The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 11–bit address fields. A total of twenty two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 four bit word locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for **all** read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the 16M DRAM Family per device: $\overline{RAS}$–only refresh cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, and page mode. All are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, fast page mode read cycle, read–write cycle, and fast page mode read–write cycle. The normal read cycle is outlined here,while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ or active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window.

For **MCM317400C**, both $\overline{CAS}$ and output enable ($\overline{G}$) control read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum and $\overline{G}$ must be active t_{RAC}–t_{GA} (both minimum) after $\overline{RAS}$ active transition to guarantee valid data out (Q) at t_{RAC}. If the t_{RCD} maximum is exceeded and/or $\overline{G}$ active transition does not occur in time, read access time is determined by either the $\overline{CAS}$ or $\overline{G}$ clock active transition (t_{CAC} or t_{GA}).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, fast page mode early write, and fast page mode read–write. Early and late write modes are discussed here, while fast page mode write operation is covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP}, apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Column address setup and hold times (t_{ASC}, t_{CAH}) and data in (D) setup and hold times (t_{DS}, t_{DH}) are referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

A late–write cycle (referred to as $\overline{G}$–controlled write) occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CAS}$ active transition, $(t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D timing parameters are referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition. 4M x 4 outputs are switched off by $\overline{G}$ inactive transition, which is required to write to the device. Q may be indeterminate (see note 15 of AC Operating Conditions table). $\overline{RAS}$ and $\overline{CAS}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{W}$ active transition to complete the write cycle. $\overline{G}$ (4M x 4) devices must remain inactive for t_{GH} after $\overline{W}$ active transition to complete the write cycle.

READ–WRITE CYCLE

A read–write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all column locations on a selected row of the 16M DRAM family. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read–write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read–write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Refresh time for the MCM317400C is 32 milliseconds.

This is accomplished by cycling through the 2048 row address within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the 16M DRAM device family. Burst refresh, a refresh of all rows consecutively, is performed every 32 milliseconds on the MCM317400C.

A normal read, write, or read–write operation to the RAM will refresh all the bits (2048) associated with the particular row decodes. Three other methods of refresh, **$\overline{RAS}$–only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$–Only Refresh

$\overline{RAS}$–only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CAS}$ remains high (V_{IH}) throughout the cycle. An external counter should be employed to ensure that all rows are refreshed within the specified limit.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CAS}$ active before $\overline{RAS}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{W}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{RAS}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CAS}$ active at the end of a read or write cycle while $\overline{RAS}$ cycles inactive for t_{RP} and back to active starts the hidden refresh. This is essentially the execution of a $\overline{CAS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1). $\overline{W}$ is subject to the same conditions with respect to $\overline{RAS}$ active transition (to prevent test mode entry) as in $\overline{CAS}$ before $\overline{RAS}$ refresh.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This test is performed with a read–write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after the 2048 cycle, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight **$\overline{CAS}$ before $\overline{RAS}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read–write cycle**. Repeat this operation 2048 times.
3. Read the "1"s that were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read–write cycle**. Repeat this operation 2048 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

TEST MODE

The internal organization of the MCM317400C allows the device to be tested as if it were a 1M x 16 DRAM. In **Test Mode** operation, column addresses A1 and A0 are ignored. A test mode cycle reads and/or writes data to a bit in each of the sixteen 1M blocks in parallel. During a write cycle, data is written using only DQ0, while during a read cycle, if all 16 bits are equal (all 0s or all 1s), DQ3 will indicate a '1'. Otherwise, DQ3 will indicate a '0'. DQ0, DQ1, and DQ2 always indicate a '1' during test mode read cycle. See "Test Mode" block diagram.

$\overline{W}$, $\overline{CAS}$ before $\overline{RAS}$ timing puts the device in **Test Mode**, as shown in the test mode timing diagram. A **$\overline{CAS}$ before $\overline{RAS}$** refresh cycle or a **$\overline{RAS}$ only** refresh cycle places the device back in normal mode. Refresh is performed in test mode by using a **$\overline{W}$, $\overline{CAS}$ before $\overline{RAS}$** refresh cycle which uses the internal refresh address counter.

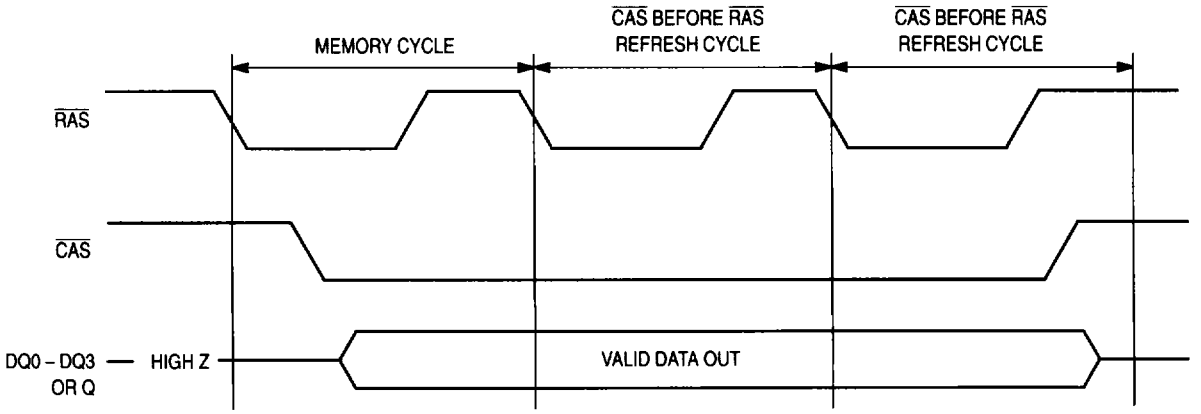


Figure 1. Hidden Refresh Cycle

TEST MODE SET CYCLE

$\overline{WRITE}$ OR $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE (TEST MODE ENTRY)
($\overline{G}$, D and A0 – A10)

4M x 4 CONFIGURATION–SPECIFIC READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM317400C–60		MCM317400C–70		Unit
	Std	Alt	Min	Max	Min	Max	
$\overline{W}$ Setup Time Before $\overline{RAS}$ low		t_{WTS}	10	—	10	—	ns
$\overline{W}$ Hold Time after $\overline{RAS}$ low		t_{WTH}	10	—	15	—	ns

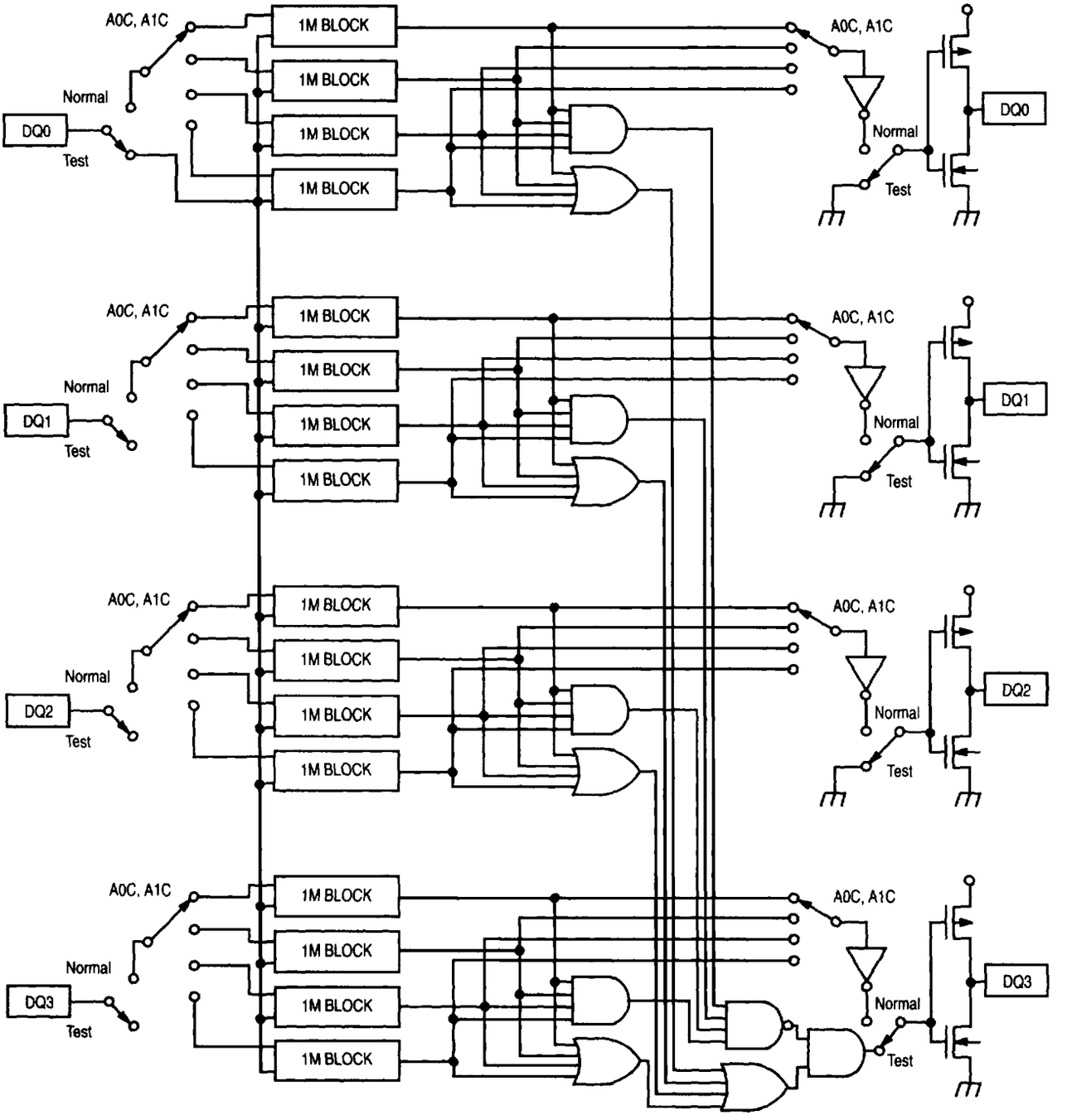
NOTE: The last mode function in initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram. The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle. During the test mode, the device is internally organized as 16 bits wide (1M bytes depth). No addressing of CA0, CA1 is required. During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4 bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4 bits, respectively. High state indicates they are the same. Low state indicates they are not same. During the test mode operation, WCBR cycle can be used to perform refresh.

MODE DEPENDENT ON $\overline{CAS}$ AND $\overline{W}$ WHEN $\overline{RAS}$ FALLS

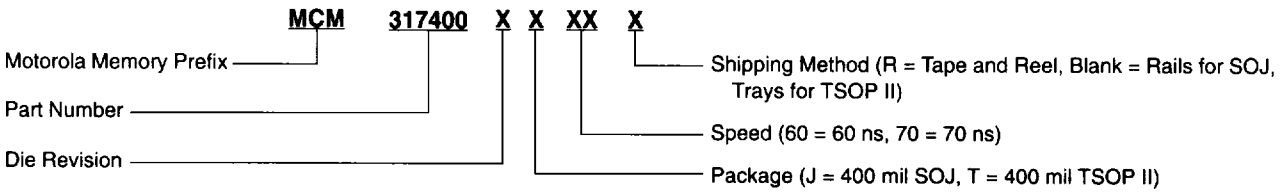
Mode	$\overline{CAS}$	$\overline{W}$*
Read, Write, RMW, FPM	1	0
CBR Refresh, Test Mode Exit	0	1
Test Mode Entry	0	0

*Logic state when $\overline{RAS}$ transitions low.

TEST MODE BLOCK DIAGRAM



ORDERING INFORMATION
(Order by Full Part Number)

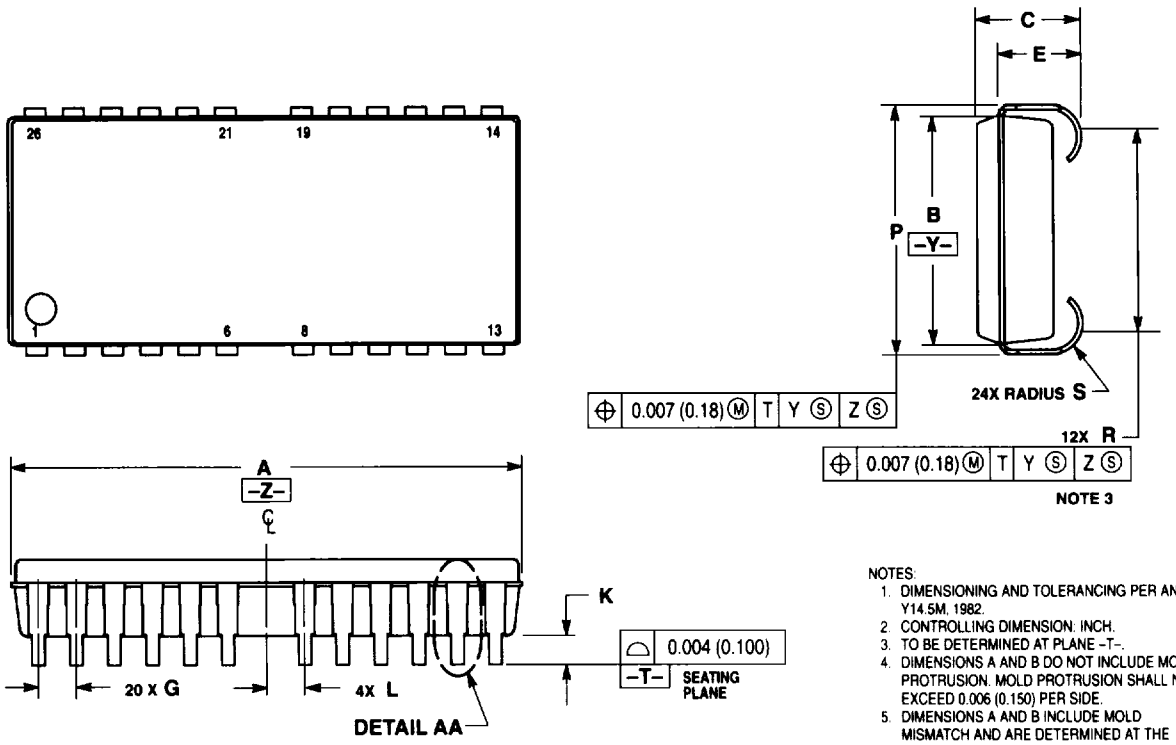


16M DEVICE NUMBERS

MCM317400CJ60	MCM317400CT60	MCM317400CJ60R	MCM317400CT60R
MCM317400CJ70	MCM317400CT70	MCM317400CJ70R	MCM317400CT70R

PACKAGE DIMENSIONS

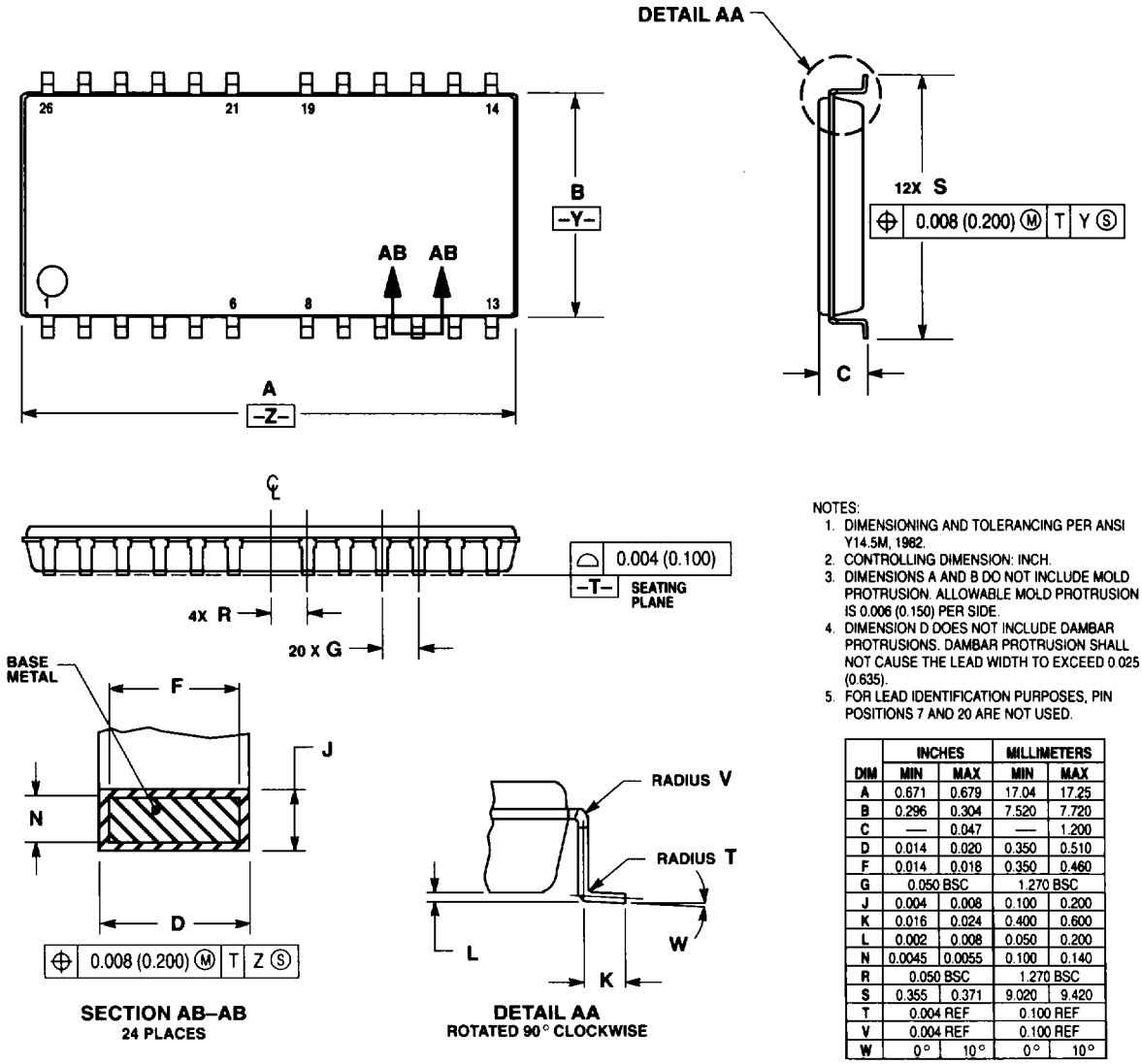
J PACKAGE
300 MIL SOJ
CASE 880A–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE -T-.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006 (0.150) PER SIDE.
5. DIMENSIONS A AND B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.
6. DIMENSION F DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE F DIMENSION TO EXCEED 0.037 (0.94).
7. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 7 AND 20 ARE NOT USED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.670	0.680	17.01	17.28
B	0.295	0.305	7.50	7.74
C	0.128	0.148	3.26	3.75
D	0.015	0.020	0.38	0.51
E	0.103	0.116	2.62	2.95
F	0.026	0.032	0.66	0.481
G	0.050 BSC		1.270 BSC	
K	0.031	0.045	0.80	1.14
L	0.050 BSC		1.270 BSC	
N	0.035	0.045	0.89	1.14
P	0.328	0.340	8.35	8.63
R	0.260	0.275	6.61	6.99
S	0.030	0.040	0.77	1.01

T PACKAGE
300 MIL TSOP II
CASE 892A–02



SECTION AB–AB
24 PLACES

DETAIL AA
ROTATED 90° CLOCKWISE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.006 (0.150) PER SIDE.
4. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.025 (0.635).
5. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 7 AND 20 ARE NOT USED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.671	0.679	17.04	17.25
B	0.296	0.304	7.520	7.720
C	—	0.047	—	1.200
D	0.014	0.020	0.350	0.510
F	0.014	0.018	0.350	0.460
G	0.050 BSC		1.270 BSC	
J	0.004	0.008	0.100	0.200
K	0.016	0.024	0.400	0.600
L	0.002	0.008	0.050	0.200
N	0.0045	0.0055	0.100	0.140
R	0.050 BSC		1.270 BSC	
S	0.355	0.371	9.020	9.420
T	0.004 REF		0.100 REF	
V	0.004 REF		0.100 REF	
W	0°	10°	0°	10°

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