# Intel® Pentium® 4 Processor 6x1$^{\Delta}$ Sequence

## Datasheet

***– On 65 nm Process in the 775-land LGA Package supporting Hyper-Threading Technology and Intel® 64 architecture***

*January 2007*

Document Number: 310308-002

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# Revision History

| Revision No. | Description | Date of Release |
|---|---|---|
| -001 | • Initial release | January 2006 |
| -002 | • Added Intel Pentium 4 processor 651, 641, and 631 at 65 W. | January 2007 |

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# Intel® Pentium® 4 Processor 6x1 Sequence

- Available at 3.6 GHz, 3.40 GHz, 3.20 GHz, and 3 GHz
- Supports Hyper-Threading Technology[1] (HT Technology) for all frequencies with 800 MHz front side bus (FSB)
- Supports Intel® 64 architecture
- Supports Execute Disable Bit capability
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Intel NetBurst® microarchitecture
- FSB frequency at 800 MHz
- Hyper-Pipelined Technology
- Advance Dynamic Execution
- Very deep out-of-order execution
- Enhanced branch prediction
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- 16-KB Level 1 data cache
- 2-MB Advanced Transfer Cache (on-die, full-speed Level 2 (L2) cache) with 8-way associativity and Error Correcting Code (ECC)
- 144 Streaming SIMD Extensions 2 (SSE2) instructions
- 13 Streaming SIMD Extensions 3 (SSE3) instructions
- Enhanced floating point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- Power Management capabilities
- System Management mode
- Multiple low-power states
- 8-way cache associativity provides improved cache hit rate on load/store operations
- 775-land Package

The Intel® Pentium® 4 processor family supporting Hyper-Threading Technology[1] (HT Technology) delivers Intel's advanced, powerful processors for desktop PCs and entry-level workstations that are based on the Intel NetBurst® microarchitecture. The Pentium 4 processor is designed to deliver performance across applications and usages where end-users can truly appreciate and experience the performance. These applications include Internet audio and streaming video, image processing, video content creation, speech, 3D, CAD, games, multimedia, and multitasking user environments. Intel® 64 architecture enables the Intel® Pentium® processor to execute operating systems and applications written to take advantage of the Intel 64 architecture.

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# 1 Introduction

The Intel® Pentium® 4 processors 6x1 sequence are the first single-core desktop processors on the 65 nm process. The Pentium 4 processor uses Flip-Chip Land Grid Array (FC-LGA6) package technology, and plugs into a 775-land surface mount, Land Grid Array (LGA) socket, referred to as the LGA775 socket.

***Note:*** In this document, unless otherwise specified, the Intel® Pentium® 4 processor 6x1 sequence refers to Intel Pentium 4 processors 661, 651, 641, 631.

***Note:*** In this document the Intel® Pentium® 4 processor 6x1 sequence on 65 nm process in the 775-land package will be referred to as the “Pentium 4 processor,” or simply “the processor.”

The Pentium 4 processor supports Intel® 64 architecture. This enhancement allows the processor to execute operating systems and applications written to take advantage of Intel 64 architecture. Further details on the 64-bit extension architecture and programming model are in the *Intel® Extended Memory 64 Technology Software Developer Guide* at http://developer.intel.com/technology/64bitextensions/.

The Pentium 4 processor supports Hyper-Threading Technology[1]. Hyper-Threading Technology allows a single, physical processor to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architecture state with its own set of general-purpose registers and control registers to provide increased system responsiveness in multitasking environments and headroom for next generation multithreaded applications. Intel recommends enabling Hyper-Threading Technology with Microsoft Windows* XP Professional or Windows* XP Home, and disabling Hyper-Threading Technology via the BIOS for all previous versions of Windows operating systems. For more information on Hyper-Threading Technology, see http://www.intel.com/products/ht/hyperthreading_more.htm. Refer to Section 6.1 for Hyper-Threading Technology configuration details.

The Pentium 4 processor’s Intel NetBurst® microarchitecture front side bus (FSB) uses a split-transaction, deferred reply protocol like previous Intel® Pentium® 4 processors. The Intel NetBurst microarchitecture FSB uses Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a “double-clocked” or 2X address bus. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 8.5 GB/s.

Intel will enable support components for the Pentium 4 processor including heatsink, heatsink retention mechanism, and socket. Manufacturability is a high priority; hence, mechanical assembly may be completed from the top of the baseboard and should not require any special tooling.

The Pentium 4 processor also include the Execute Disable Bit capability previously available in Intel® Itanium® processors. This feature, combined with a supported operating system, allows memory to be marked as executable or non-executable. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer over run vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architecture Software Developer’s Manual* for more detailed information.

The processor includes an address bus powerdown capability that removes power from the address and data signals when the FSB is not in use. This feature is always enabled on the processor.

Enhanced Intel® SpeedStep® technology allows trade-offs to be made between performance and power consumptions. This may lower average power consumption (in conjunction with OS support).

## 1.1 Terminology

A '#' symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

Front Side Bus refers to the interface between the processor and system core logic (a.k.a. the chipset components). The FSB is a multiprocessing interface to processors, memory, and I/O.

### 1.1.1 Processor Packaging Terminology

Commonly used terms are explained here for clarification:

- **Intel® Pentium® 4 processor on 65 nm process in the 775-land package** — Processor in the FC-LGA6 package with a 2 MB L2 cache.
- **Processor** — For this document, the term processor is the generic form of the Intel® Pentium® 4 processor 6x1 sequence on 65 nm process in the 775-land package.
- **Keep-out zone** — The area on or near the processor that system design can not utilize.
- **Intel® 945G/945GZ/945P/945PL Express chipsets** — Chipset that supports DDR and DDR2 memory technology for the Pentium 4 processor.
- **Processor core** — Processor core die with integrated L2 cache.
- **LGA775 socket** — The Pentium 4 processor mates with the system board through a surface mount, 775-land, LGA socket.
- **Integrated heat spreader (IHS)** —A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
- **Retention mechanism (RM)** — Since the LGA775 socket does not include any mechanical features for heatsink attach, a retention mechanism is required. Component thermal solutions should attach to the processor via a retention mechanism that is independent of the socket.
- **FSB (Front Side Bus)** — The electrical interface that connects the processor to the chipset. Also referred to as the processor system bus or the system bus. All memory and I/O transactions as well as interrupt messages pass between the processor and chipset over the FSB.
- **Storage conditions** — Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor lands should not be connected to any supply voltages, have any I/Os biased, or receive any clocks. Upon exposure to "free air"(i.e., unsealed packaging or a device removed from

packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.

- **Functional operation** — Refers to normal operating conditions in which all processor specifications, including DC, AC, system bus, signal quality, mechanical and thermal are satisfied.

## 1.2 References

Material and concepts available in the following documents may be beneficial when reading this document.

**Table 1. References**

| Document | Location |
|---|---|
| Intel® Pentium® 4 Processor 6x1 Sequence Specification Update | http://www.intel.com/design/pentium4/specupdt/310309.htm |
| *Intel® Pentium® D Processor, Intel® Pentium® Processor Extreme Edition, and Intel® Pentium® 4 Processor Thermal and Mechanical Design Guidelines*<br><br>**NOTE:** Refer to this document for 86 W processors. | http://www.intel.com/design/pentiumXE/designex/306830.htm |
| *Intel® Core™2 Duo Desktop Processor E6000 Sequence and Intel® Pentium® 4 Processor 6x1 Sequence Thermal and Mechanical Design Guidelines*<br><br>**NOTE:** Refer To this document for 65 W processors. | http://www.intel.com/design/processor/designex/313685.htm |
| *Voltage Regulator-Down (VRD) 11.0 Processor Power Delivery Design Guidelines For Desktop LGA775 Socket* | http://www.intel.com/design/Pentium4/guides/302356.htm |
| *LGA775 Socket Mechanical Design Guide* | http://www.intel.com/design/Pentium4/guides/302666.htm |
| *Balanced Technology Extended (BTX) System Design Guide* | http://www.formfactors.org |
| *Intel® 64 and IA-32 Architecture Software Developer's Manuals* | |
| *Volume 1: Basic Architecture* | http://www.intel.com/products/processor/manuals/ |
| *Volume 2A: Instruction Set Reference, A-M* | http://www.intel.com/products/processor/manuals/ |
| *Volume 2B: Instruction Set Reference, N-Z* | http://www.intel.com/products/processor/manuals/ |
| *Volume 3A: System Programming Guide* | http://www.intel.com/products/processor/manuals/ |
| *Volume 3B: System Programming Guide* | http://www.intel.com/products/processor/manuals/ |

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# 2 Electrical Specifications

This chapter describes the electrical characteristics of the processor interfaces and signals. DC electrical characteristics are provided.

## 2.1 Power and Ground Lands

The Pentium 4 processor has 226 VCC (power), 24 VTT and 273 VSS (ground) inputs for on-chip power distribution. All power lands must be connected to $V_{CC}$, while all VSS lands must be connected to a system ground plane. The processor VCC lands must be supplied the voltage determined by the **V**oltage **ID**entification (VID) lands.

Twenty-four (24) signals are denoted as VTT, that provide termination for the front side bus and power to the I/O buffers. A separate supply must be implemented for these lands, that meets the $V_{TT}$ specifications outlined in Table 4.

## 2.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings. This may cause voltages on power planes to sag below their minimum specified values if bulk decoupling is not adequate. Larger bulk storage ($C_{BULK}$), such as electrolytic or aluminum-polymer capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition. The motherboard must be designed to ensure that the voltage provided to the processor remains within the specifications listed in Table 4. Failure to do so can result in timing violations or reduced lifetime of the component.

### 2.2.1 $V_{CC}$ Decoupling

$V_{CC}$ regulator solutions need to provide sufficient decoupling capacitance to satisfy the processor voltage specifications. This includes bulk capacitance with low effective series resistance (ESR) to keep the voltage rail within specifications during large swings in load current. In addition, ceramic decoupling capacitors are required to filter high frequency content generated by the front side bus and processor activity. Consult the *Voltage Regulator-Down (VRD) 10.1 Design Guide For Desktop and Transportable LGA775 Socket* for further information.

### 2.2.2 $V_{TT}$ Decoupling

Decoupling must be provided on the motherboard. Decoupling solutions must be sized to meet the expected load. To insure compliance with the specifications, various factors associated with the power delivery solution must be considered including regulator type, power plane and trace sizing, and component placement. A conservative decoupling solution would consist of a combination of low ESR bulk capacitors and high frequency ceramic capacitors.

### 2.2.3 FSB Decoupling

The processor integrates signal termination on the die. In addition, some of the high frequency capacitance required for the FSB is included on the processor package. However, additional high frequency capacitance must be added to the motherboard to properly decouple the return currents from the front side bus. Bulk decoupling must also be provided by the motherboard for proper [A]GTL+ bus operation.

## 2.3 Voltage Identification

The Voltage Identification (VID) specification for the processor is defined by the *Voltage Regulator-Down (VRD) 10.1 Design Guide For Desktop and Transportable LGA775 Socket*. The voltage set by the VID signals is the reference VR output voltage to be delivered to the processor VCC lands (see Chapter 2.5.3 for $V_{CC}$ overshoot specifications). Refer to Table 14 for the DC specifications for these signals. A minimum voltage for each processor frequency is provided in Table 4.

Individual processor VID values may be calibrated during manufacturing such that two devices at the same core speed may have different default VID settings. This is reflected by the VID Range values provided in Table 4. Refer to the *Intel® Pentium® 4 Processor Specification Update* for further details on specific valid core frequency and VID values of the processor. Note that this differs from the VID employed by the processor during a power management event (Thermal Monitor 2, Enhanced Intel SpeedStep technology, or Enhanced HALT State).

The processor uses 6 voltage identification signals, VID[5:0], to support automatic selection of power supply voltages. Table 2 specifies the voltage level corresponding to the state of VID[5:0]. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. If the processor socket is empty (VID[5:0] = x11111), or the voltage regulation circuit cannot supply the voltage that is requested, it must disable itself. See the *Voltage Regulator-Down (VRD) 10.1 Design Guide For Desktop and Transportable LGA775 Socket* for further details.

The processor provides the ability to operate while transitioning to an adjacent VID and its associated processor core voltage ($V_{CC}$). This will represent a DC shift in the load line. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target core voltage. Transitions above the specified VID are not permitted. Table 4 includes VID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in Table 5 and Figure 1 as measured across the VCC_SENSE and VSS_SENSE lands.

The VRM or VRD used must be capable of regulating its output to the value defined by the new VID. DC specifications for dynamic VID transitions are included in Table 4 and Table 5. Refer to the *Voltage Regulator-Down (VRD) 10.1 Design Guide For Desktop and Transportable LGA775 Socket* for further details.

## Table 2. Voltage Identification Definition

| VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | VID | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | VID |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 0.8375 | 0 | 1 | 1 | 0 | 1 | 0 | 1.2125 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0.8500 | 1 | 1 | 1 | 0 | 0 | 1 | 1.2250 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0.8625 | 0 | 1 | 1 | 0 | 0 | 1 | 1.2375 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0.8750 | 1 | 1 | 1 | 0 | 0 | 0 | 1.2500 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0.8875 | 0 | 1 | 1 | 0 | 0 | 0 | 1.2625 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0.9000 | 1 | 1 | 0 | 1 | 1 | 1 | 1.2750 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0.9125 | 0 | 1 | 0 | 1 | 1 | 1 | 1.2875 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0.9250 | 1 | 1 | 0 | 1 | 1 | 0 | 1.3000 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0.9375 | 0 | 1 | 0 | 1 | 1 | 0 | 1.3125 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0.9500 | 1 | 1 | 0 | 1 | 0 | 1 | 1.3250 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0.9625 | 0 | 1 | 0 | 1 | 0 | 1 | 1.3375 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0.9750 | 1 | 1 | 0 | 1 | 0 | 0 | 1.3500 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0.9875 | 0 | 1 | 0 | 1 | 0 | 0 | 1.3625 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1.0000 | 1 | 1 | 0 | 0 | 1 | 1 | 1.3750 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1.0125 | 0 | 1 | 0 | 0 | 1 | 1 | 1.3875 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1.0250 | 1 | 1 | 0 | 0 | 1 | 0 | 1.4000 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1.0375 | 0 | 1 | 0 | 0 | 1 | 0 | 1.4125 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1.0500 | 1 | 1 | 0 | 0 | 0 | 1 | 1.4250 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1.0625 | 0 | 1 | 0 | 0 | 0 | 1 | 1.4375 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1.0750 | 1 | 1 | 0 | 0 | 0 | 0 | 1.4500 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1.0875 | 0 | 1 | 0 | 0 | 0 | 0 | 1.4625 |
| 1 | 1 | 1 | 1 | 1 | 1 | VR output off | 1 | 0 | 1 | 1 | 1 | 1 | 1.4750 |
| 0 | 1 | 1 | 1 | 1 | 1 | VR output off | 0 | 0 | 1 | 1 | 1 | 1 | 1.4875 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1.1000 | 1 | 0 | 1 | 1 | 1 | 0 | 1.5000 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1.1125 | 0 | 0 | 1 | 1 | 1 | 0 | 1.5125 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1.1250 | 1 | 0 | 1 | 1 | 0 | 1 | 1.5250 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1.1375 | 0 | 0 | 1 | 1 | 0 | 1 | 1.5375 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1.1500 | 1 | 0 | 1 | 1 | 0 | 0 | 1.5500 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1.1625 | 0 | 0 | 1 | 1 | 0 | 0 | 1.5625 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1.1750 | 1 | 0 | 1 | 0 | 1 | 1 | 1.5750 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1.1875 | 0 | 0 | 1 | 0 | 1 | 1 | 1.5875 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1.2000 | 1 | 0 | 1 | 0 | 1 | 0 | 1.6000 |

## 2.4 Reserved, Unused, and TESTHI Signals

All RESERVED lands must remain unconnected. Connection of these lands to $V_{CC}$, $V_{SS}$, $V_{TT}$, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Chapter 4 for a land listing of the processor and the location of all RESERVED lands.

In a system level design, on-die termination has been included by the processor to allow signals to be terminated within the processor silicon. Most unused GTL+ inputs should be left as no connects as GTL+ termination is provided on the processor silicon. However, see Table 7 for details on GTL+ signals that do not include on-die termination.

Unused active high inputs, should be connected through a resistor to ground ($V_{SS}$). Unused outputs can be left unconnected; however, this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within ± 20% of the impedance of the motherboard trace for front side bus signals. For unused GTL+ input or I/O signals, use pull-up resistors of the same value as the on-die termination resistors ($RT_T$). For details, see Table 16.

TAP, GTL+ Asynchronous inputs, and GTL+ Asynchronous outputs do not include on-die termination. Inputs and utilized outputs must be terminated on the motherboard. Unused outputs may be terminated on the motherboard or left unconnected. Note that leaving unused outputs unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing.

All TESTHI[13:0] lands should be individually connected to $V_{TT}$ via a pull-up resistor that matches the nominal trace impedance.

The TESTHI signals may use individual pull-up resistors or be grouped together as detailed below. A matched resistor must be used for each group:

- TESTHI[1:0]
- TESTHI[7:2]
- TESTHI8 – cannot be grouped with other TESTHI signals
- TESTHI9 – cannot be grouped with other TESTHI signals
- TESTHI10 – cannot be grouped with other TESTHI signals
- TESTHI11 – cannot be grouped with other TESTHI signals
- TESTHI12 – cannot be grouped with other TESTHI signals
- TESTHI13 – cannot be grouped with other TESTHI signals

However, using boundary scan test will not be functional if these lands are connected together. For optimum noise margin, all pull-up resistor values used for TESTHI[13:0] lands should have a resistance value within ± 20% of the impedance of the board transmission line traces. For example, if the nominal trace impedance is 50 Ω, then a value between 40 Ω and 60 Ω should be used.

## 2.5 Voltage and Current Specification

### 2.5.1 Absolute Maximum and Minimum Ratings

Table 3 specifies absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

**Table 3. Absolute Maximum and Minimum Ratings**

| Symbol | Parameter | Min | Max | Unit | Notes[1,2] |
|---|---|---|---|---|---|
| $V_{CC}$ | Core voltage with respect to $V_{SS}$ | –0.3 | 1.55 | V | |
| $V_{TT}$ | FSB termination voltage with respect to $V_{SS}$ | –0.3 | 1.55 | V | |
| $T_C$ | Processor case temperature | See Chapter 5 | See Chapter 5 | °C | |
| $T_{STORAGE}$ | Processor storage temperature | –40 | 85 | °C | 3, 4, 5 |

**NOTES:**
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, refer to the processor case temperature specifications.
4. This rating applies to the processor and does not include any tray or packaging.
5. Failure to adhere to this specification can affect the long term reliability of the processor.

## 2.5.2 DC Voltage and Current Specification

### Table 4. Voltage and Current Specification

| Symbol | Parameter | | Min | Typ | Max | Unit | Notes[1, 2] |
|---|---|---|---|---|---|---|---|
| VID Range | VID | | 1.200 | — | 1.3375 | V | 3 |
| $V_{CC}$ | Processor number | $V_{CC}$ for 775_VR_CONFIG_05A | Refer to Table 5 and Figure 1 | | | V | 4, 5, 6 |
| | 661 | 3.6 GHz | | | | | |
| | 651 | 3.4 GHz | | | | | |
| | 641 | 3.2 GHz | | | | | |
| | 631 | 3 GHz | | | | | |
| $I_{CC}$ | Processor number | $I_{CC}$ for 775_VR_CONFIG_05A | — | — | | A | 7 |
| | 661 | 3.6 GHz | | | 100 | | |
| | 651 | 3.4 GHz | | | 100 | | |
| | 641 | 3.2 GHz | | | 100 | | |
| | 631 | 3 GHz | | | 100 | | |
| | Processor number | $I_{CC}$ for 775_VR_CONFIG_06 | — | — | | | |
| | 651 | 3.4 GHz | | | 65 | | |
| | 641 | 3.2 GHz | | | 65 | | |
| | 631 | 3 GHz | | | 65 | | |
| $I_{SGNT}$ | Processor number | $I_{CC}$ Stop-Grant for 775_VR_CONFIG_05A | — | — | | A | 8,9,10,11 |
| | 661 | 3.6 GHz | | | 50 | | |
| | 651 | 3.4 GHz | | | 50 | | |
| | 641 | 3.2 GHz | | | 50 | | |
| | 631 | 3 GHz | | | 50 | | |
| | Processor number | $I_{CC}$ Stop-Grant for 775_VR_CONFIG_06 | | | | | |
| | 651 | 3.4 GHz | | | 40 | | |
| | 641 | 3.2 GHz | | | 40 | | |
| | 631 | 3 GHz | | | 40 | | |
| $I_{ENHANCED\_AUTO\_HALT}$ | Processor number | $I_{CC}$ Enhanced Halt for 775_VR_CONFIG_05A | | | | A | 8,10,11 |
| | 661 | 3.6 GHz | | | 40 | | |
| | 651 | 3.4 GHz | | | 40 | | |
| | 641 | 3.2 GHz | | | 40 | | |
| | 631 | 3 GHz | | | 40 | | |
| | Processor number | $I_{CC}$ Enhanced Auto HALT for 775_VR_CONFIG_06 | | | | | |
| | 651 | 3.4 GHz | | | 25 | | |
| | 641 | 3.2 GHz | | | 25 | | |
| | 631 | 3 GHz | | | 25 | | |
| $I_{TCC}$ | $I_{CC}$ TCC active | | — | — | $I_{CC}$ | A | 12 |
| $V_{TT}$ | FSB termination voltage (DC + AC specifications) | | 1.14 | 1.20 | 1.26 | V | 13, 14 |

## Table 4. Voltage and Current Specification

| Symbol | Parameter | Min | Typ | Max | Unit | Notes[1, 2] |
|---|---|---|---|---|---|---|
| VTT_OUT_LEFT and VTT_OUT_RIGHT $I_{CC}$ | DC Current that may be drawn from VTT_OUT_LEFT and VTT_OUT_RIGHT per pin | — | — | 580 | mA | |
| $I_{TT}$ | Steady-state FSB termination current | — | — | 3.5 | A | 15, 16 |
| $I_{TT\_POWER\text{-}UP}$ | Power-up FSB termination current | — | — | 4.5 | A | 15, 17 |
| $I_{CC\_VCCA}$ | $I_{CC}$ for PLL lands | — | — | 35 | mA | |
| $I_{CC\_VCCIOPLL}$ | $I_{CC}$ for I/O PLL land | — | — | 26 | mA | |
| $I_{CC\_GTLREF}$ | $I_{CC}$ for GTLREF | — | — | 200 | μA | |

**NOTES:**

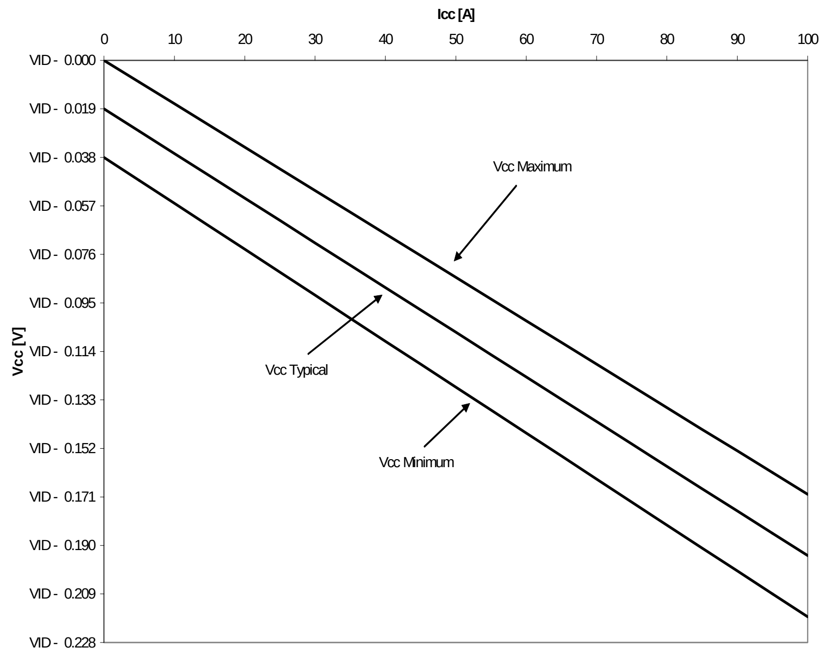
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Adherence to the voltage specifications for the processor are required to ensure reliable processor operation.
3. Each processor is programmed with a maximum valid voltage identification value (VID) that is set at manufacturing and can not be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Thermal Monitor 2, Enhanced Intel SpeedStep technology, or Enhanced HALT State).
4. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 2.3 and Table 2 for more information.
5. The voltage specification requirements are measured across VCC_SENSE and VSS_SENSE lands at the socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
6. Refer to Table 5 and Figure 1 for the minimum, typical, and maximum $V_{CC}$ allowed for a given current. The processor should not be subjected to any $V_{CC}$ and $I_{CC}$ combination wherein $V_{CC}$ exceeds $V_{CC\_MAX}$ for a given current.
7. $I_{CC\_MAX}$ is specified at $V_{CC\_MAX}$.
8. The current specified is also for AutoHALT State.
9. $I_{CC}$ Stop-Grant is specified at $V_{CC\_MAX}$.
10. $I_{SGNT}$ and $I_{ENHANCED\_AUTO\_HALT}$ are specified at $V_{CC\_TYP}$ and TC = 50 °C.
11. These parameters are based on design characterization and are not tested.
12. The maximum instantaneous current the processor will draw while the thermal control circuit is active (as indicated by the assertion of PROCHOT#) is the same as the maximum $I_{CC}$ for the processor.
13. $V_{TT}$ must be provided via a separate voltage source and not be connected to $V_{CC}$. This specification is measured at the land.
14. Baseboard bandwidth is limited to 20 MHz.
15. This is maximum total current drawn from $V_{TT}$ plane by only the processor. This specification does not include the current coming from $R_{TT}$ (through the signal line). Refer to the *Voltage Regulator-Down (VRD) 10.1 Design Guide For Desktop and Transportable LGA775 Socket* to determine the total $I_{TT}$ drawn by the system.
16. This is a steady-state $I_{TT}$ current specification, which is applicable when both $V_{TT}$ and $V_{CC}$ are high.
17. This is a power-up peak current specification that is applicable when $V_{TT}$ is high and $V_{CC}$ is low.

**Table 5. $V_{CC}$ Static and Transient Tolerance for 775_VR_CONFIG_05A (Mainstream) and for 775_VR_CONFIG_06 Processors**

| $I_{CC}$ (A) | Voltage Deviation from VID Setting (V)[1,2,3,4] | | |
|---|---|---|---|
| | Maximum Voltage 1.7 mΩ | Typical Voltage 1.75 mΩ | Minimum Voltage 1.8 mΩ |
| 0 | 0.000 | -0.019 | -0.038 |
| 5 | -0.009 | -0.028 | -0.047 |
| 10 | -0.017 | -0.037 | -0.056 |
| 15 | -0.026 | -0.045 | -0.065 |
| 20 | -0.034 | -0.054 | -0.074 |
| 25 | -0.043 | -0.063 | -0.083 |
| 30 | -0.051 | -0.072 | -0.092 |
| 35 | -0.060 | -0.080 | -0.101 |
| 40 | -0.068 | -0.089 | -0.110 |
| 45 | -0.077 | -0.098 | -0.119 |
| 50 | -0.085 | -0.107 | -0.128 |
| 55 | -0.094 | -0.115 | -0.137 |
| 60 | -0.102 | -0.124 | -0.146 |
| 65 | -0.111 | -0.133 | -0.155 |
| 70 | -0.119 | -0.142 | -0.164 |
| 75 | -0.128 | -0.150 | -0.173 |
| 80 | -0.133 | -0.156 | -0.178 |
| 85 | -0.145 | -0.168 | -0.191 |
| 90 | -0.153 | -0.177 | -0.200 |
| 95 | -0.162 | -0.185 | -0.209 |
| 100 | -0.170 | -0.194 | -0.218 |

**NOTES:**
1. The loadline specification includes both static and transient limits except for overshoot allowed as shown in Section 2.5.3.
2. This table is intended to aid in reading discrete points on Figure 1.
3. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE lands. Voltage regulation feedback for voltage regulator circuits must be taken from processor VCC and VSS lands. Refer to the *Voltage Regulator-Down (VRD) 10.1 Design Guide For Desktop and Transportable LGA775 Socket* for socket loadline guidelines and VR implementation details.
4. Adherence to this loadline specification for the Pentium 4 processor is required to ensure reliable processor operation.

**Figure 1. $V_{CC}$ Static and Transient Tolerance for 775_VR_CONFIG_05A (Mainstream) and for 775_VR_CONFIG_06 Processors**




**NOTES:**
1. The loadline specification includes both static and transient limits except for overshoot allowed as shown in Section 2.5.3.
2. This loadline specification shows the deviation from the VID set point.
3. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE lands. Voltage regulation feedback for voltage regulator circuits must be taken from processor VCC and VSS lands. Refer to the *Voltage Regulator-Down (VRD) 10.1 Design Guide For Desktop and Transportable LGA775 Socket* for socket loadline guidelines and VR implementation details.

## 2.5.3 $V_{CC}$ Overshoot

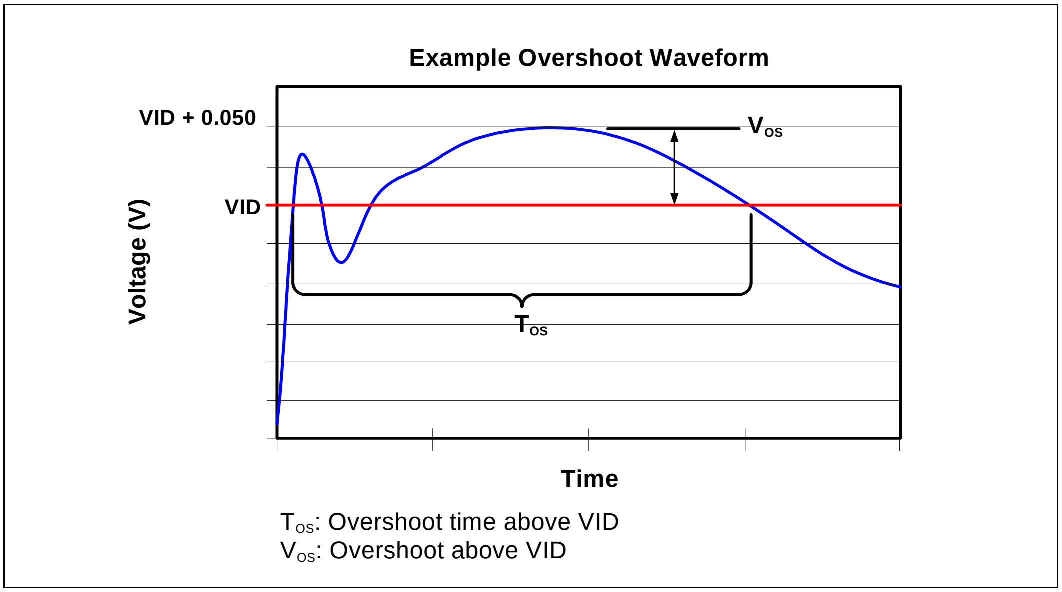
The processor can tolerate short transient overshoot events where $V_{CC}$ exceeds the VID voltage when transitioning from a high to low current load condition. This overshoot cannot exceed VID + $V_{OS\_MAX}$ ($V_{OS\_MAX}$ is the maximum allowable overshoot voltage). The time duration of the overshoot event must not exceed $T_{OS\_MAX}$ ($T_{OS\_MAX}$ is the maximum allowable time duration above VID). These specifications apply to the processor die voltage as measured across the VCC_SENSE and VSS_SENSE lands.

**Table 6. $V_{CC}$ Overshoot Specifications**

| Symbol | Parameter | Min | Max | Unit | Figure | Notes |
|---|---|---|---|---|---|---|
| $V_{OS\_MAX}$ | Magnitude of $V_{CC}$ overshoot above VID | — | 0.050 | V | 2 | 1 |
| $T_{OS\_MAX}$ | Time duration of $V_{CC}$ overshoot above VID | — | 25 | µs | 2 | 1 |

**NOTES:**
1. Adherence to these specifications for the Pentium 4 processor is required to ensure reliable processor operation.

**Figure 2. $V_{CC}$ Overshoot Example Waveform**




**NOTES:**
1. $V_{OS}$ is measured overshoot voltage.
2. $T_{OS}$ is measured time duration above VID.

### 2.5.4 Die Voltage Validation

Overshoot events on the processor must meet the specifications in Table 6 when measured across the VCC_SENSE and VSS_SENSE lands. Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot must be taken with a bandwidth limited oscilloscope set to a greater than or equal to 100 MHz bandwidth limit.

## 2.6 Signaling Specifications

Most processor front side bus signals use Gunning Transceiver Logic (GTL+) signaling technology. This technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. Platforms implement a termination voltage level for GTL+ signals defined as $V_{TT}$. Because platforms implement separate power planes for each processor (and chipset), separate $V_{CC}$ and $V_{TT}$ supplies are necessary. This configuration allows for improved noise tolerance as processor frequency increases. Speed enhancements to data and address busses have caused signal integrity considerations and platform design methods to become even more critical than with previous processor families.

The GTL+ inputs require a reference voltage (GTLREF) that is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the motherboard (see Table 16 for GTLREF specifications). Termination resistors ($R_{TT}$) for GTL+ signals are provided on the processor silicon and are terminated to $V_{TT}$. Intel chipsets will also provide on-die termination, thus eliminating the need to terminate the bus on the motherboard for most GTL+ signals.

## 2.6.1 FSB Signal Groups

The front side bus signals have been combined into groups by buffer type. GTL+ input signals have differential input buffers that use GTLREF[1:0] as a reference level. In this document, the term “GTL+ Input” refers to the GTL+ input group as well as the GTL+ I/O group when receiving. Similarly, “GTL+ Output” refers to the GTL+ output group as well as the GTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals that are dependent on the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals that are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asynchronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 7 identifies which signals are common clock, source synchronous, and asynchronous.

**Table 7. FSB Signal Groups (Sheet 1 of 2)**

<table>
<tr><th>Signal Group</th><th>Type</th><th>Signals[1]</th></tr>
<tr><td>GTL+ Common Clock Input</td><td>Synchronous to BCLK[1:0]</td><td>BPRI#, DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#</td></tr>
<tr><td>GTL+ Common Clock I/O</td><td>Synchronous to BCLK[1:0]</td><td>AP[1:0]#, ADS#, BINIT#, BNR#, BPM[5:0]#, BR0#, DBSY#, DP[3:0]#, DRDY#, HIT#, HITM#, LOCK#, MCERR#</td></tr>
<tr><td>GTL+ Source Synchronous I/O</td><td>Synchronous to assoc. strobe</td><td><table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>REQ[4:0]#, A[16:3]#[3]</td><td>ADSTB0#</td></tr>
<tr><td>A[35:17]#[3]</td><td>ADSTB1#</td></tr>
<tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#, DSTBN0#</td></tr>
<tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#, DSTBN1#</td></tr>
<tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#, DSTBN2#</td></tr>
<tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#, DSTBN3#</td></tr>
</table></td></tr>
<tr><td>GTL+ Strobes</td><td>Synchronous to BCLK[1:0]</td><td>ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#</td></tr>
<tr><td>GTL+ Asynchronous Input</td><td></td><td>A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI#, STPCLK#, PWRGOOD</td></tr>
<tr><td>GTL+ Asynchronous Output</td><td></td><td>FERR#/PBE#, IERR#, THERMTRIP#</td></tr>
<tr><td>GTL+ Asynchronous Input/Output</td><td></td><td>PROCHOT#</td></tr>
<tr><td>TAP Input</td><td>Synchronous to TCK</td><td>TCK, TDI, TMS, TRST#</td></tr>
</table>

## Table 7. FSB Signal Groups (Sheet 2 of 2)

| Signal Group | Type | Signals[1] |
|---|---|---|
| TAP Output | Synchronous to TCK | TDO |
| FSB Clock | Clock | BCLK[1:0], ITP_CLK[1:0][2] |
| Power/Other | | VCC, VTT, VCCA, VCCIOPLL, VID[5:0], VSS, VSSA, GTLREF[1:0], COMP[5:4,1:0], RESERVED, TESTHI[13:0], THERMDA, THERMDC, VCC_SENSE, VCC_MB_REGULATION, VSS_SENSE, VSS_MB_REGULATION, BSEL[2:0], SKTOCC#, DBR#[2], VTTPWRGD, BOOTSELECT, VTT_OUT_LEFT, VTT_OUT_RIGHT, VTT_SEL, LL_ID[1:0], MSID[1:0], FCx, IMPSEL |

**NOTES:**
1. Refer to Section 4.2 for signal descriptions.
2. In processor systems where no debug port is implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
3. The value of these signals during the active-to-inactive edge of RESET# defines the processor configuration options. See Section 6.1 for details.

## Table 8. Signal Characteristics

| Signals with $R_{TT}$ | Signals with No $R_{TT}$ |
|---|---|
| A[35:3]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BINIT#, BNR#, BOOTSELECT[1], BPRI#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, HIT#, HITM#, LOCK#, MCERR#, MSID[1:0][1], PROCHOT#, REQ[4:0]#, RS[2:0]#, RSP#, TRDY#, IMPSEL[1] | A20M#, BCLK[1:0], BPM[5:0]#, BSEL[2:0], COMP[5:4,1:0], FERR#/PBE#, IERR#, IGNNE#, INIT#, ITP_CLK[1:0], LINT0/INTR, LINT1/NMI, PWRGOOD, RESET#, SKTOCC#, SMI#, STPCLK#, TDO, TESTHI[13:0], THERMDA, THERMDC, THERMTRIP#, VID[5:0], VTTPWRGD, GTLREF[1:0], TCK, TDI, TMS, TRST#, VTT_SEL |
| **Open Drain Signals[2]** | |
| THERMTRIP#, FERR#/PBE#, IERR#, BPM[5:0]#, BR0#, TDO, LL_ID[1:0], FCx | |

**NOTES:**
1. These signals have a 500–5000 Ω pull-up to $V_{TT}$ rather than on-die termination.
2. Signals that do not have $R_{TT}$, nor are actively driven to their high-voltage level.

## Table 9. Signal Reference Voltages

| GTLREF | $V_{TT}$ / 2 |
|---|---|
| BPM[5:0]#, LINT0/INTR, LINT1/NMI, RESET#, BINIT#, BNR#, HIT#, HITM#, MCERR#, PROCHOT#, BR0#, A[35:0]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BPRI#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, LOCK#, REQ[4:0]#, RS[2:0]#, RSP#, TRDY# | BOOTSELECT, VTTPWRGD, A20M#, IGNNE#, INIT#, MSID[1:0], PWRGOOD[1], SMI#, STPCLK#, TCK[1], TDI[1], TMS[1], TRST#[1] |

**NOTES:**
1. These signals also have hysteresis added to the reference voltage. See Table 12 for more information.

## 2.6.2 GTL+ Asynchronous Signals

Legacy input signals such as A20M#, IGNNE#, INIT#, SMI#, and STPCLK# use CMOS input buffers. All of these signals follow the same DC requirements as GTL+ signals; however, the outputs are not actively driven high (during a logical 0-to-1 transition) by the processor. These signals do not have setup or hold time specifications in relation to BCLK[1:0].

All of the GTL+ Asynchronous signals are required to be asserted/deasserted for at least six BCLKs in order for the processor to recognize the proper signal state. See Section 2.6.3 for the DC specifications for the GTL+ Asynchronous signal groups. See Section 6.2 for additional timing requirements for entering and leaving the low power states.

## 2.6.3 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless otherwise stated. All specifications apply to all frequencies and cache sizes unless otherwise stated.

### Table 10. GTL+ Signal Group DC Specifications

| Symbol | Parameter | Min | Max | Unit | Notes[1] |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | 0.0 | GTLREF – (0.10 * $V_{TT}$) | V | 2, 3 |
| $V_{IH}$ | Input High Voltage | GTLREF + (0.10 * $V_{TT}$) | $V_{TT}$ | V | 3, 4, 5 |
| $V_{OH}$ | Output High Voltage | 0.90*$V_{TT}$ | $V_{TT}$ | V | 5, 6 |
| $I_{OL}$ | Output Low Current | N/A | $V_{TT\_MAX}$/ [(0.50*$R_{TT\_MIN}$)+($R_{ON\_MIN}$)] | A | |
| $I_{LI}$ | Input Leakage Current | N/A | ± 200 | µA | 6 |
| $I_{LO}$ | Output Leakage Current | N/A | ± 200 | µA | 7 |
| $R_{ON}$ | Buffer On Resistance | 6 | 12 | W | |

**NOTES:**
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. $V_{IL}$ is defined as the voltage range at a receiving agent that will be interpreted as a logical low value.
3. The $V_{TT}$ referred to in these specifications is the instantaneous $V_{TT}$.
4. $V_{IH}$ is defined as the voltage range at a receiving agent that will be interpreted as a logical high value.
5. $V_{IH}$ and $V_{OH}$ may experience excursions above $V_{TT}$. However, input signal drivers must comply with the signal quality specifications.
6. Leakage to $V_{SS}$ with land held at $V_{TT}$.
7. Leakage to $V_{TT}$ with land held at 300 mV.

### Table 11. GTL+ Asynchronous Signal Group DC Specifications

| Symbol | Parameter | Min | Max | Unit | Notes[1] |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | 0.0 | $V_{TT}$/2 – (0.10 * $V_{TT}$) | V | 2, 3 |
| $V_{IH}$ | Input High Voltage | $V_{TT}$/2 + (0.10 * $V_{TT}$) | $V_{TT}$ | V | 3, 4, 5, 6 |
| $V_{OH}$ | Output High Voltage | 0.90*$V_{TT}$ | $V_{TT}$ | V | 5, 6, 7 |
| $I_{OL}$ | Output Low Current | — | $V_{TT}$/ [(0.50*$R_{TT\_MIN}$)+($R_{ON\_MIN}$)] | A | 8 |

## Table 11. GTL+ Asynchronous Signal Group DC Specifications

| Symbol | Parameter | Min | Max | Unit | Notes[1] |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | N/A | ± 200 | µA | 9 |
| $I_{LO}$ | Output Leakage Current | N/A | ± 200 | µA | 10 |
| $R_{ON}$ | Buffer On Resistance | 6 | 12 | W | |

**NOTES:**
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. $V_{IL}$ is defined as the voltage range at a receiving agent that will be interpreted as a logical low value.
3. LINT0/INTR and LINT1/NMI use GTLREF as a reference voltage. For these two signals, $V_{IH}$ = GTLREF + (0.10 * $V_{TT}$) and $V_{IL}$= GTLREF – (0.10 * $V_{TT}$).
4. $V_{IH}$ is defined as the voltage range at a receiving agent that will be interpreted as a logical high value.
5. $V_{IH}$ and $V_{OH}$ may experience excursions above $V_{TT}$. However, input signal drivers must comply with the signal quality specifications.
6. The $V_{TT}$ referred to in these specifications refers to instantaneous $V_{TT}$.
7. All outputs are open drain.
8. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load.
9. Leakage to $V_{SS}$ with land held at $V_{TT}$.
10. Leakage to $V_{TT}$ with land held at 300 mV.

## Table 12. PWRGOOD and TAP Signal Group DC Specifications

| Symbol | Parameter | Min | Max | Unit | Notes[1, 2] |
|---|---|---|---|---|---|
| $V_{HYS}$ | Input Hysteresis | 120 | 396 | mV | 3 |
| $V_{T+}$ | PWRGOOD Input low-to-high threshold voltage | 0.5 * ($V_{TT}$ + $V_{HYS\_MIN}$ + 0.24) | 0.5 * ($V_{TT}$ + $V_{HYS\_MAX}$ + 0.24) | V | 4, 5 |
| | TAP Input low-to-high threshold voltage | 0.5 * ($V_{TT}$ + $V_{HYS\_MIN}$) | 0.5 * ($V_{TT}$ + $V_{HYS\_MAX}$) | V | 4 |
| $V_{T-}$ | PWRGOOD Input high-to-low threshold voltage | 0.4 * $V_{TT}$ | 0.6 * $V_{TT}$ | V | 4 |
| | TAP Input high-to-low threshold voltage | 0.5 * ($V_{TT}$ – $V_{HYS\_MAX}$) | 0.5 * ($V_{TT}$ – $V_{HYS\_MIN}$) | V | 4 |
| $V_{OH}$ | Output High Voltage | N/A | $V_{TT}$ | V | 4, 6 |
| $I_{OL}$ | Output Low Current | — | 22.2 | mA | 7 |
| $I_{LI}$ | Input Leakage Current | — | ± 200 | µA | 8 |
| $I_{LO}$ | Output Leakage Current | — | ± 200 | µA | 9 |
| $R_{ON}$ | Buffer On Resistance | 6 | 12 | W | |

**NOTES:**
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All outputs are open drain.
3. $V_{HYS}$ represents the amount of hysteresis, nominally centered about 0.5 * $V_{TT}$, for all TAP inputs.
4. The $V_{TT}$ referred to in these specifications refers to instantaneous $V_{TT}$.
5. 0.24 V is defined at 20% of nominal $V_{TT}$ of 1.2 V.
6. The TAP signal group must meet the signal quality specifications.
7. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load.
8. Leakage to Vss with land held at $V_{TT}$.
9. Leakage to $V_{TT}$ with land held at 300 mV.

## Table 13. VTTPWRGD DC Specifications

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | — | — | 0.3 | V |
| $V_{IH}$ | Input High Voltage | 0.9 | — | — | V |

## Table 14. BSEL[2:0] and VID[5:0] DC Specifications

| Symbol | Parameter | Max | Unit | Notes[1, 2] |
|---|---|---|---|---|
| $R_{ON}$ (BSEL) | Buffer On Resistance | 120 | Ω | |
| $R_{ON}$ (VID) | Buffer On Resistance | 120 | Ω | |
| $I_{OL}$ | Max Land Current | 2.4 | mA | |
| $I_{LO}$ | Output Leakage Current | 200 | µA | 3 |
| $V_{TOL}$ | Voltage Tolerance | $V_{TT}$(max) | V | |

**NOTES:**
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These parameters are not tested and are based on design simulations.
3. Leakage to $V_{SS}$ with land held at 2.5 V.

## Table 15. BOOTSELECT DC Specifications

| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | — | — | 0.24 | V | 1 |
| $V_{IH}$ | Input High Voltage | 0.96 | — | — | V | 1 |

**NOTES:**
1. These parameters are not tested and are based on design simulations.

### 2.6.3.1 GTL+ Front Side Bus Specifications

In most cases, termination resistors are not required as these are integrated into the processor silicon. See Table 8 for details on which GTL+ signals do not include on-die termination.

Valid high and low levels are determined by the input buffers by comparing with a reference voltage called GTLREF. Table 16 lists the GTLREF specifications. The GTL+ reference voltage (GTLREF) should be generated on the system board using high precision voltage divider circuits.

**Table 16. GTL+ Bus Voltage Definitions**

| Symbol | Parameter | Min | Typ | Max | Units | Notes[1] |
|---|---|---|---|---|---|---|
| GTLREF_PU | GTLREF pull up resistor | 124 * 0.99 | 124 | 124 * 1.01 | Ω | 2 |
| GTLREF_PD | GTLREF pull down resistor | 210 * 0.99 | 210 | 210 * 1.01 | Ω | 2 |
| $R_{PULLUP}$ | On die pull-up for BOOTSELECT signal | 500 | — | 5000 | Ω | 3 |
| $R_{TT}$ | 60 Ω Platform Termination Resistance | 51 | 60 | 66 | Ω | 4 |
| | 50 Ω Platform Termination Resistance | 39 | 50 | 55 | Ω | 4 |
| COMP[1:0] | 60 Ω Platform Termination COMP Resistance | 59.8 | 60.4 | 61 | Ω | 5 |
| | 50 Ω Platform Termination COMP Resistance | 49.9 * 0.99 | 49.9 | 49.9 * 1.01 | Ω | 5 |
| COMP[5:4] | 60 Ω Platform Termination COMP Resistance | 59.8 | 60.4 | 61 | Ω | 5 |
| | 50 Ω Platform Termination COMP Resistance | 49.9 * 0.99 | 49.9 | 49.9 * 1.01 | Ω | 5 |

**NOTES:**
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. GTLREF is to be generated from $V_{TT}$ by a voltage divider of 1% resistors (one divider for each GTLREF land).
3. These pull-ups are to $V_{TT}$.
4. $R_{TT}$ is the on-die termination resistance measured at $V_{TT}/2$ of the GTL+ output driver. The IMPSEL pin is used to select a 50 Ω or 60 Ω buffer and $R_{TT}$ value.
5. COMP resistance must be provided on the system board with 1% resistors. COMP[1:0] resistors are to $V_{SS}$. COMP[5:4] resistors are to $V_{TT}$.

# 2.7 Clock Specifications

## 2.7.1 Front Side Bus Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous generation processors, the Pentium 4 processor core frequency is a multiple of the BCLK[1:0] frequency. The processor bus ratio multiplier will be set at its default ratio during manufacturing. Refer to Table 17 for the processor supported ratios.

The processor uses a differential clocking implementation. For more information on processor clocking, contact your Intel representative.

**Table 17. Core Frequency to FSB Multiplier Configuration**

| Multiplication of System Core Frequency to FSB Frequency | Core Frequency (200 MHz BCLK / 800 MHz FSB) | Notes[1,2] |
|---|---|---|
| 1/12 | 2.40 GHz | |
| 1/13 | 2.60 GHz | |
| 1/14 | 2.80 GHz | |
| 1/15 | 3 GHz | |
| 1/16 | 3.20 GHz | |
| 1/17 | 3.40 GHz | |
| 1/18 | 3.60 GHz | |
| 1/19 | 3.80 GHz | |
| 1/20 | 4 GHz | |
| 1/21 | 4.20 GHz | |
| 1/22 | 4.40 GHz | |
| 1/23 | 4.60 GHz | |
| 1/24 | 4.80 GHz | |
| 1/25 | 5 GHz | |

**NOTES:**
1. Individual processors operate only at or below the rated frequency.
2. Listed frequencies are not necessarily committed production frequencies.

### 2.7.2 FSB Frequency Select Signals (BSEL[2:0])

The BSEL[2:0] signals are used to select the frequency of the processor input clock (BCLK[1:0]). Table 18 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset, and clock synthesizer. All agents must operate at the same frequency.

The Pentium 4 processor will operate at an 800 MHz FSB frequency (selected by a 200 MHz BCLK[1:0] frequency).

For more information about these signals, refer to Section 4.2.

**Table 18. BSEL[2:0] Frequency Table for BCLK[1:0]**

| BSEL2 | BSEL1 | BSEL0 | FSB Frequency |
|---|---|---|---|
| L | L | L | RESERVED |
| L | L | H | RESERVED |
| L | H | H | RESERVED |
| L | H | L | 200 MHz |
| H | H | L | RESERVED |
| H | H | H | RESERVED |
| H | L | H | RESERVED |
| H | L | L | RESERVED |

### 2.7.3 Phase Lock Loop (PLL) and Filter

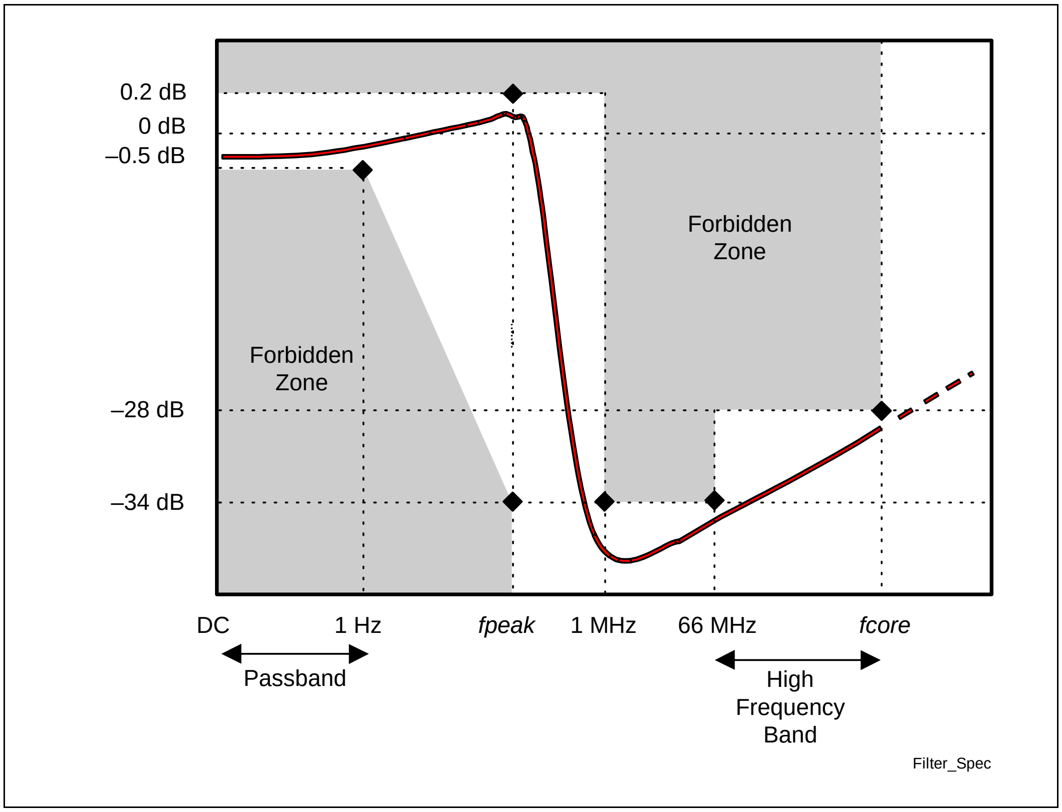
$V_{CCA}$ and $V_{CCIOPLL}$ are power sources required by the PLL clock generators for the Pentium 4 processor silicon. Since these PLLs are analog, they require low noise power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). To prevent this degradation, these supplies must be low pass filtered from $V_{TT}$.

The AC low-pass requirements, with input at $V_{TT}$ are as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter requirements are illustrated in Figure 3.

## Figure 3. Phase Lock Loop (PLL) Filter Requirements




**NOTES:**
1. Diagram not to scale.
2. No specification for frequencies beyond fcore (core frequency).
3. $f_{peak}$, if existent, should be less than 0.05 MHz.
4. $f_{core}$ represents the maximum core frequency supported by the platform.

## 2.7.4 BCLK[1:0] Specifications

### Table 19. Front Side Bus Differential BCLK Specifications

| Symbol | Parameter | Min | Typ | Max | Unit | Notes[1] |
|---|---|---|---|---|---|---|
| $V_L$ | Input Low Voltage | -0.150 | 0.000 | N/A | V | |
| $V_H$ | Input High Voltage | 0.660 | 0.700 | 0.850 | V | |
| $V_{CROSS(abs)}$ | Absolute Crossing Point | 0.250 | N/A | 0.550 | V | 2, 3 |
| $V_{CROSS(rel)}$ | Relative Crossing Point | 0.250 + 0.5($V_{Havg}$ – 0.700) | N/A | 0.550 + 0.5($V_{Havg}$ – 0.700) | V | 3, 4, 5 |
| $\Delta V_{CROSS}$ | Range of Crossing Points | N/A | N/A | 0.140 | V | |
| $V_{OS}$ | Overshoot | N/A | N/A | $V_H$ + 0.3 | V | 6 |
| $V_{US}$ | Undershoot | -0.300 | N/A | N/A | V | 7 |
| $V_{RBM}$ | Ringback Margin | 0.200 | N/A | N/A | V | 8 |
| $V_{TM}$ | Threshold Region | $V_{CROSS}$ – 0.100 | N/A | $V_{CROSS}$ + 0.100 | V | 9 |

**NOTES:**
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing voltage is defined as the instantaneous voltage value when the rising edge of BCLK0 equals the falling edge of BCLK1.
3. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
4. $V_{Havg}$ is the statistical average of the $V_H$ measured by the oscilloscope.
5. $V_{Havg}$ can be measured directly using “Vtop” on Agilent* oscilloscopes and “High” on Tektronix* oscilloscopes.
6. Overshoot is defined as the absolute value of the maximum voltage.
7. Undershoot is defined as the absolute value of the minimum voltage.
8. Ringback Margin is defined as the absolute voltage difference between the maximum Rising Edge Ringback and the maximum Falling Edge Ringback.
9. Threshold Region is defined as a region entered around the crossing point voltage in which the differential receiver switches. It includes input threshold hysteresis.

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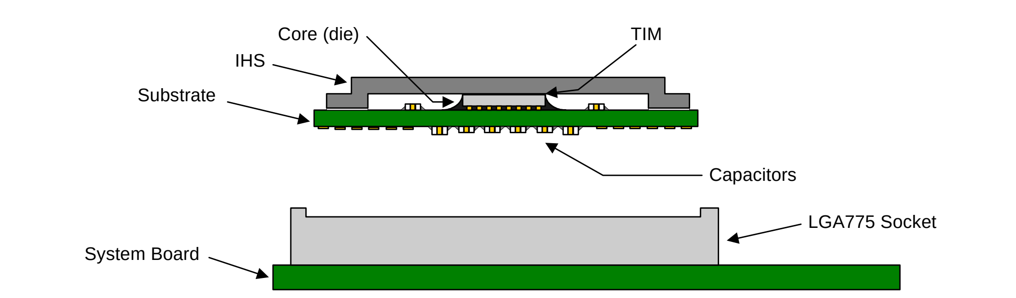
# 3 Package Mechanical Specifications

The Pentium 4 processor is packaged in a Flip-Chip Land Grid Array (FC-LGA6) package that interfaces with the motherboard via an LGA775 socket. The package consists of a processor core mounted on a substrate land-carrier. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the mating surface for processor component thermal solutions, such as a heatsink. Figure 4 shows a sketch of the processor package components and how they are assembled together. Refer to the *LGA775 Socket Mechanical Design Guide* for complete details on the LGA775 socket.

The package components shown in Figure 4 include the following:

- Integrated Heat Spreader (IHS)
- Thermal Interface Material (TIM)
- Processor core (die)
- Package substrate
- Capacitors

**Figure 4. Processor Package Assembly Sketch**



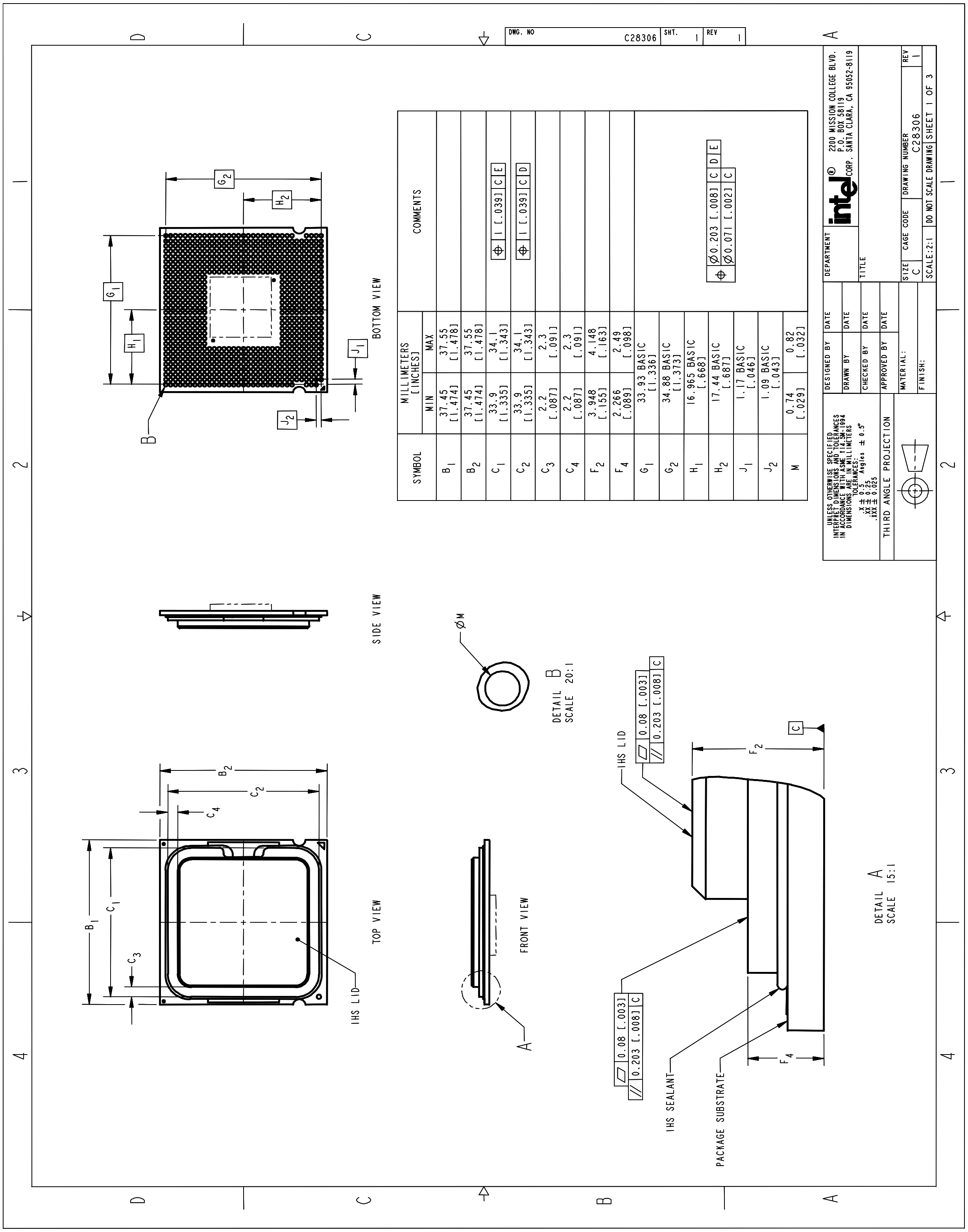

**NOTE:**
1. Socket and motherboard are included for reference and are not part of processor package.

## 3.1 Package Mechanical Drawing

The package mechanical drawings are shown in Figure 5 and Figure 6. The drawings include dimensions necessary to design a thermal solution for the processor. These dimensions include:

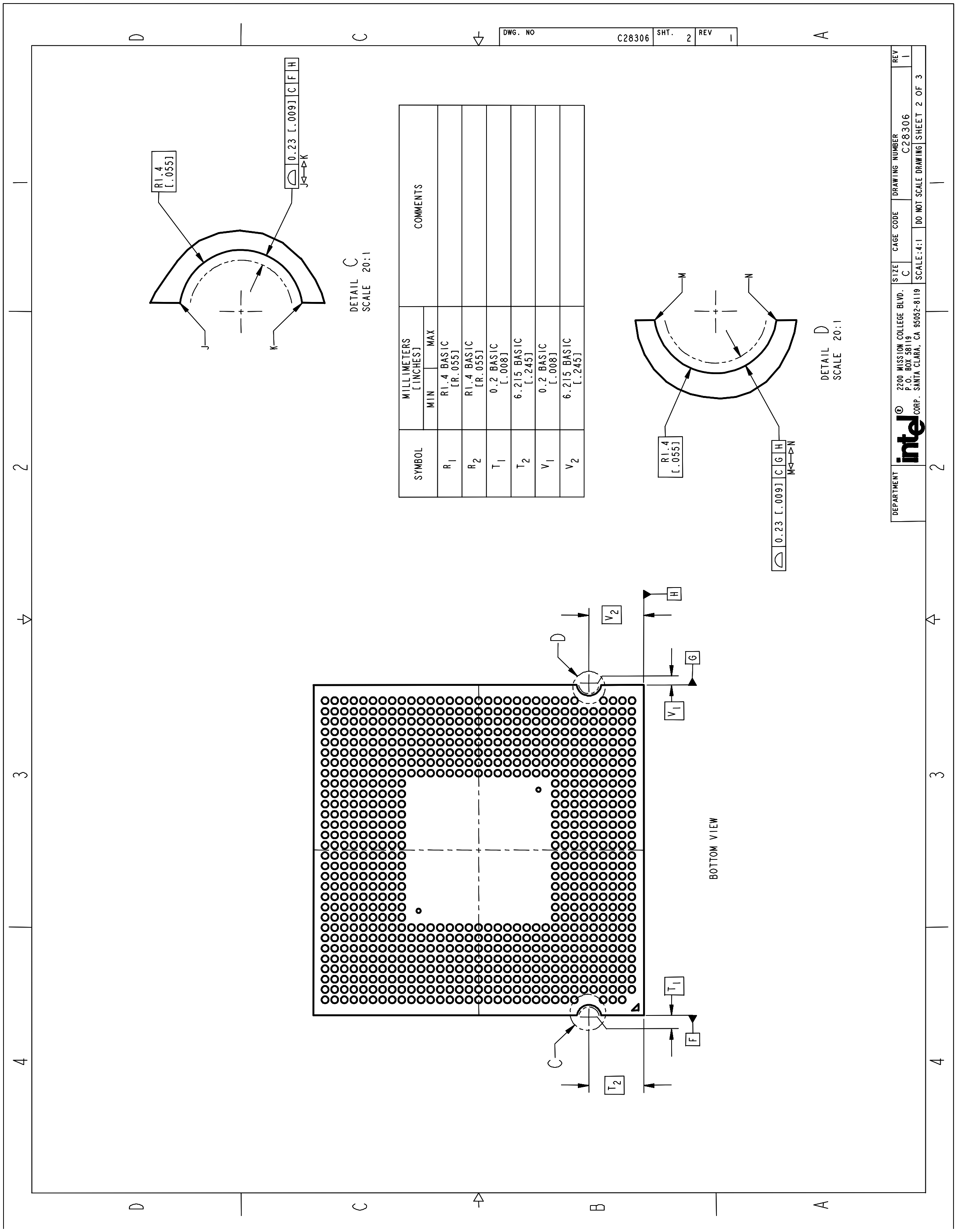
- Package reference with tolerances (total height, length, width, etc.)
- IHS parallelism and tilt
- Land dimensions
- Top-side and back-side component keep-out dimensions
- Reference datums
- All drawing dimensions are in mm [in].
- Guidelines on potential IHS flatness variation with socket load plate actuation and installation of the cooling solution is available in the processor Thermal and Mechanical Design Guidelines (see Section 1.2).

## Figure 5. Processor Package Drawing Sheet 1 of 3



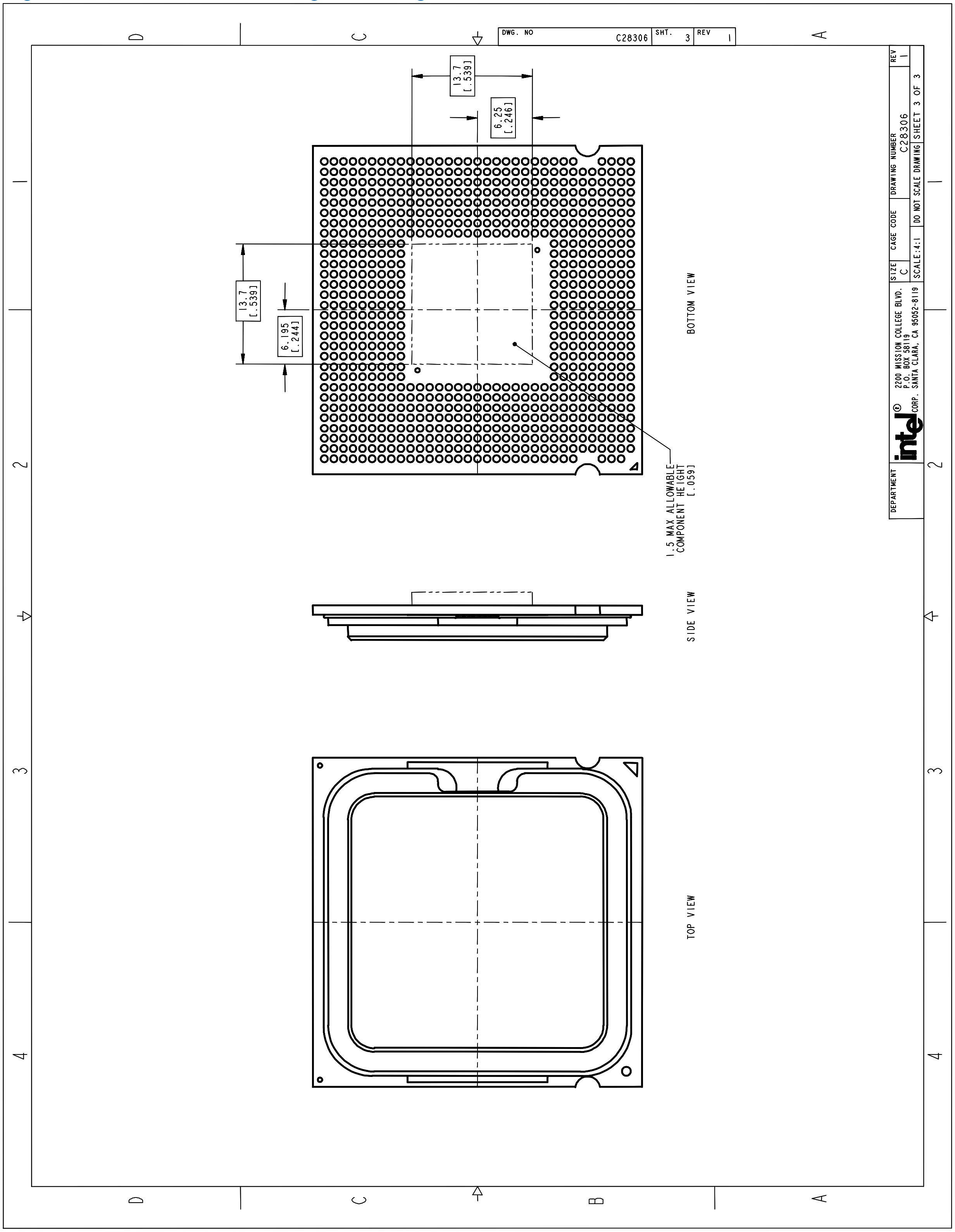

| SYMBOL | MILLIMETERS [INCHES] MIN | MAX | COMMENTS |
|---|---|---|---|
| $B_1$ | 37.45 [1.474] | 37.55 [1.478] | |
| $B_2$ | 37.45 [1.474] | 37.55 [1.478] | |
| $C_1$ | 33.9 [1.335] | 34.1 [1.343] | ⌖ 1 [.039] C E |
| $C_2$ | 33.9 [1.335] | 34.1 [1.343] | ⌖ 1 [.039] C D |
| $C_3$ | 2.2 [.087] | 2.3 [.091] | |
| $C_4$ | 2.2 [.087] | 2.3 [.091] | |
| $F_2$ | 3.948 [.155] | 4.148 [.163] | |
| $F_4$ | 2.266 [.089] | 2.49 [.098] | |
| $G_1$ | 33.93 BASIC [1.336] | | |
| $G_2$ | 34.88 BASIC [1.373] | | |
| $H_1$ | 16.965 BASIC [.668] | | ⌖ Ø0.203 [.008] C D E / Ø0.071 [.002] C |
| $H_2$ | 17.44 BASIC [.687] | | |
| $J_1$ | 1.17 BASIC [.046] | | |
| $J_2$ | 1.09 BASIC [.043] | | |
| M | 0.74 [.029] | 0.82 [.032] | |

## Figure 6. Processor Package Drawing Sheet 2 of 3




| SYMBOL | MILLIMETERS [INCHES] MIN | MAX | COMMENTS |
|---|---|---|---|
| $R_1$ | R1.4 BASIC [R.055] | | |
| $R_2$ | R1.4 BASIC [R.055] | | |
| $T_1$ | 0.2 BASIC [.008] | | |
| $T_2$ | 6.215 BASIC [.245] | | |
| $V_1$ | 0.2 BASIC [.008] | | |
| $V_2$ | 6.215 BASIC [.245] | | |

## Figure 7. Processor Package Drawing Sheet 3 of 3



## 3.2 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Decoupling capacitors are typically mounted to either the topside or land-side of the package substrate. See Figure 5 and Figure 6 for keep-out zones. The location and quantity of package capacitors may change due to manufacturing efficiencies but will remain within the component keep-in.

## 3.3 Package Loading Specifications

Table 20 provides dynamic and static load specifications for the processor package. These mechanical maximum load limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Also, any mechanical system or component testing should not exceed the maximum limits. The processor package substrate should not be used as a mechanical reference or load-bearing surface for thermal and mechanical solution. The minimum loading specification must be maintained by any thermal and mechanical solutions.

**Table 20. Processor Loading Specifications**

| Parameter | Minimum | Maximum | Notes |
|---|---|---|---|
| Static | 80 N [17 lbf] | 311 N [70 lbf] | 1, 2, 3 |
| Dynamic | — | 756 N [170 lbf] | 1, 3, 4 |

**NOTES:**
1. These specifications apply to uniform compressive loading in a direction normal to the processor IHS.
2. This is the maximum force that can be applied by a heatsink retention clip. The clip must also provide the minimum specified load on the processor package.
3. These specifications are based on limited testing for design characterization. Loading limits are for the package only and do not include the limits of the processor socket.
4. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.

## 3.4 Package Handling Guidelines

Table 21 includes a list of guidelines on package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

**Table 21. Package Handling Guidelines**

| Parameter | Maximum Recommended | Notes |
|---|---|---|
| Shear | 311 N [70 lbf] | 1, 2 |
| Tensile | 111 N [25 lbf] | 2, 3 |
| Torque | 3.95 N-m [35 lbf-in] | 2, 4 |

**NOTES:**
1. A shear load is defined as a load applied to the IHS in a direction parallel to the IHS top surface.
2. These guidelines are based on limited testing for design characterization.
3. A tensile load is defined as a pulling load applied to the IHS in a direction normal to the IHS surface.
4. A torque load is defined as a twisting load applied to the IHS in an axis of rotation normal to the IHS top surface.

## 3.5 Package Insertion Specifications

The Pentium 4 processor can be inserted into and removed from a LGA775 socket 15 times. The socket should meet the LGA775 requirements detailed in the *LGA775 Socket Mechanical Design Guide*.

## 3.6 Processor Mass Specification

The typical mass of the Pentium 4 processor is 21.5 g [0.76 oz]. This mass [weight] includes all the components that are included in the package.

## 3.7 Processor Materials

Table 22 lists some of the package components and associated materials.

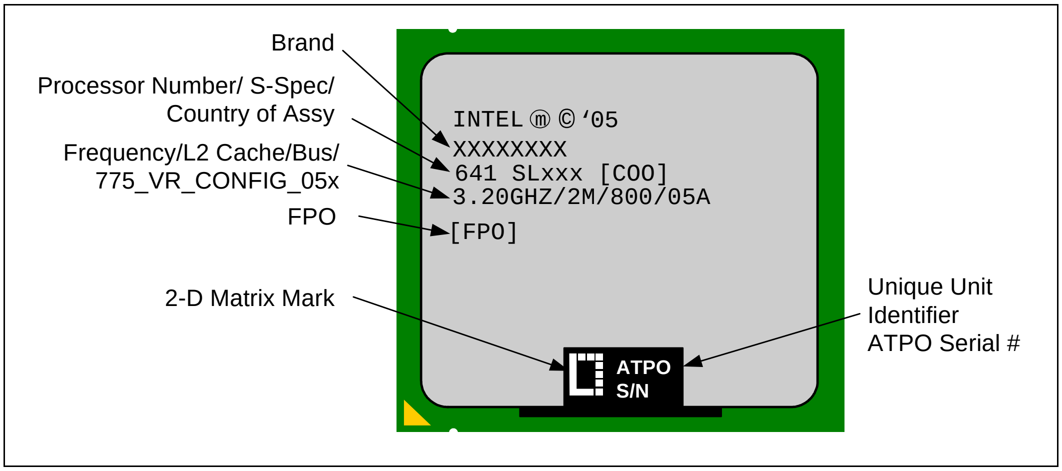
**Table 22. Processor Materials**

| Component | Material |
|---|---|
| Integrated Heat Spreader (IHS) | Nickel Plated Copper |
| Substrate | Fiber Reinforced Resin |
| Substrate Lands | Gold Plated Copper |

## 3.8 Processor Markings

Figure 8 shows the topside markings on the processor. This diagram is to aid in the identification of the Pentium 4 processor.

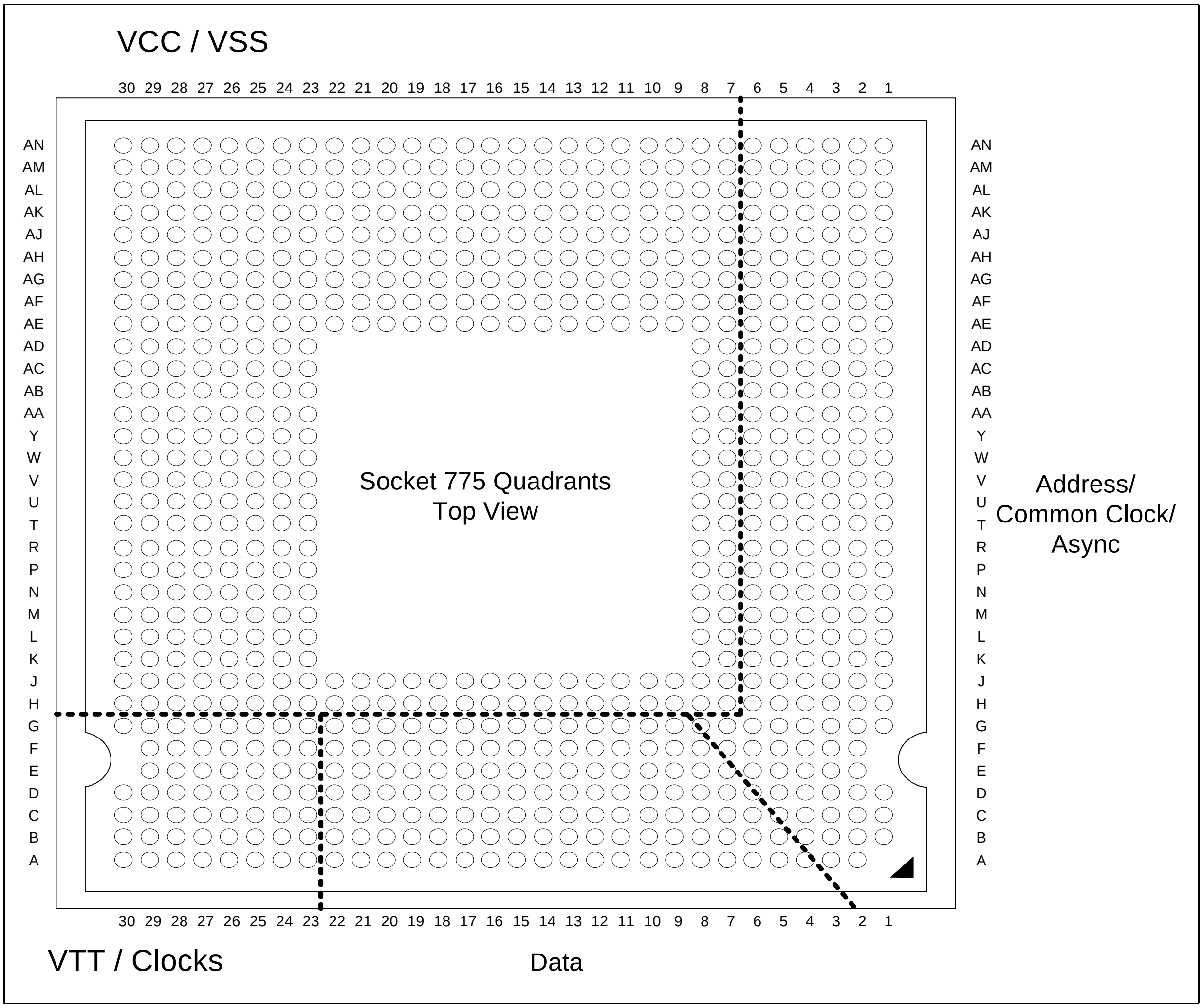
**Figure 8. Processor Top-Side Markings Example**



## 3.9 Processor Land Coordinates

Figure 9 shows the top view of the processor land coordinates. The coordinates are referred to throughout the document to identify processor lands.

**Figure 9. Processor Land Coordinates and Quadrants (Top View)**

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# 4 Land Listing and Signal Descriptions

This chapter provides the processor land assignment and signal descriptions.

## 4.1 Processor Land Assignments

This section contains the land listings for the processor. The land-out footprint is shown in Figure 10 and Figure 11. These figures represent the land-out arranged by land number and they show the physical location of each signal on the package land array (top view). Table 23 is a listing of all processor lands ordered alphabetically by land (signal) name. Table 24 is also a listing of all processor lands; the ordering is by land number.

## Figure 10.land-out Diagram (Top View – Left Side)

| | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AN | VCC | VCC | VSS | VSS | VCC | VCC | VSS | VSS | VCC | VCC | VSS | VCC | VCC | VSS | VSS | VCC |
| AM | VCC | VCC | VSS | VSS | VCC | VCC | VSS | VSS | VCC | VCC | VSS | VCC | VCC | VSS | VSS | VCC |
| AL | VCC | VCC | VSS | VSS | VCC | VCC | VSS | VSS | VCC | VCC | VSS | VCC | VCC | VSS | VSS | VCC |
| AK | VSS | VSS | VSS | VSS | VCC | VCC | VSS | VSS | VCC | VCC | VSS | VCC | VCC | VSS | VSS | VCC |
| AJ | VSS | VSS | VSS | VSS | VCC | VCC | VSS | VSS | VCC | VCC | VSS | VCC | VCC | VSS | VSS | VCC |
| AH | VCC | VCC | VCC | VCC | VCC | VCC | VSS | VSS | VCC | VCC | VSS | VCC | VCC | VSS | VSS | VCC |
| AG | VCC | VCC | VCC | VCC | VCC | VCC | VSS | VSS | VCC | VCC | VSS | VCC | VCC | VSS | VSS | VCC |
| AF | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VCC | VCC | VSS | VCC | VCC | VSS | VSS | VCC |
| AE | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VCC | VCC | VCC | VSS | VCC | VCC | VSS | VSS | VCC |
| AD | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | | | | | | | | |
| AC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | | | | | | | | |
| AB | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | | | |
| AA | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | | | |
| Y | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | | | | | | | | |
| W | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | | | | | | | | |
| V | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | | | |
| U | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | | | | | | | | |
| T | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | | | | | | | | |
| R | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | | | |
| P | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | | | |
| N | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | | | | | | | | |
| M | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | | | | | | | | |
| L | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | | | | | | | | |
| K | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | | | | | | | | |
| J | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | VCC | DP3# | DP0# | VCC |
| H | BSEL1 | FC15 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | DP2# | DP1# |
| G | BSEL2 | BSEL0 | BCLK1 | TESTHI4 | TESTHI5 | TESTHI3 | TESTHI6 | RESET# | D47# | D44# | DSTBN2# | DSTBP2# | D35# | D36# | D32# | D31# |
| F | | RSVD | BCLK0 | VTT_SEL | TESTHI0 | TESTHI2 | TESTHI7 | RSVD | VSS | D43# | D41# | VSS | D38# | D37# | VSS | D30# |
| E | | VSS | VSS | VSS | VSS | VSS | FC10 | RSVD | D45# | D42# | VSS | D40# | D39# | VSS | D34# | D33# |
| D | VTT | VTT | VTT | VTT | VTT | VTT | VSS | FC9 | D46# | VSS | D48# | DBI2# | VSS | D49# | RSVD | VSS |
| C | VTT | VTT | VTT | VTT | VTT | VTT | VSS | VCCIO PLL | VSS | D58# | DBI3# | VSS | D54# | DSTBP3# | VSS | D51# |
| B | VTT | VTT | VTT | VTT | VTT | VTT | VSS | VSSA | D63# | D59# | VSS | D60# | D57# | VSS | D55# | D53# |
| A | VTT | VTT | VTT | VTT | VTT | VTT | VSS | VCCA | D62# | VSS | RSVD | D61# | VSS | D56# | DSTBN3# | VSS |
| | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 |

## Figure 11.land-out Diagram (Top View – Right Side)

| 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VCC | VSS | VCC | VCC | VSS | VCC | VCC | FC16 | VSS_MB_ REGULATION | VCC_MB_ REGULATION | VSS_ SENSE | VCC_ SENSE | VSS | VSS | AN |
| VCC | VSS | VCC | VCC | VSS | VCC | VCC | FC12 | VTTPWRGD | FC11 | VSS | VID2 | VID0 | VSS | AM |
| VCC | VSS | VCC | VCC | VSS | VCC | VCC | VSS | VID3 | VID1 | VID5 | VSS | PROCHOT# | THERMDA | AL |
| VCC | VSS | VCC | VCC | VSS | VCC | VCC | VSS | FC8 | VSS | VID4 | ITP_CLK0 | VSS | THERMDC | AK |
| VCC | VSS | VCC | VCC | VSS | VCC | VCC | VSS | A35# | A34# | VSS | ITP_CLK1 | BPM0# | BPM1# | AJ |
| VCC | VSS | VCC | VCC | VSS | VCC | VCC | VSS | VSS | A33# | A32# | VSS | RSVD | VSS | AH |
| VCC | VSS | VCC | VCC | VSS | VCC | VCC | VSS | A29# | A31# | A30# | BPM5# | BPM3# | TRST# | AG |
| VCC | VSS | VCC | VCC | VSS | VCC | VCC | VSS | VSS | A27# | A28# | VSS | BPM4# | TDO | AF |
| VCC | VSS | VCC | VCC | VSS | VCC | SKTOCC# | VSS | RSVD | VSS | RSVD | FC18 | VSS | TCK | AE |
| | | | | | | VCC | VSS | A22# | ADSTB1# | VSS | BINIT# | BPM2# | TDI | AD |
| | | | | | | VCC | VSS | VSS | A25# | RSVD | VSS | DBR# | TMS | AC |
| | | | | | | VCC | VSS | A17# | A24# | A26# | MCERR# | IERR# | VSS | AB |
| | | | | | | VCC | VSS | VSS | A23# | A21# | VSS | LL_ID1 | VTT_OUT_ RIGHT | AA |
| | | | | | | VCC | VSS | A19# | VSS | A20# | FC17 | VSS | BOOT SELECT | Y |
| | | | | | | VCC | VSS | A18# | A16# | VSS | TESTHI1 | TESTHI12 | MSID0 | W |
| | | | | | | VCC | VSS | VSS | A14# | A15# | VSS | LL_ID0 | MSID1 | V |
| | | | | | | VCC | VSS | A10# | A12# | A13# | AP1# | AP0# | VSS | U |
| | | | | | | VCC | VSS | VSS | A9# | A11# | VSS | COMP5 | COMP1 | T |
| | | | | | | VCC | VSS | ADSTB0# | VSS | A8# | FERR#/ PBE# | VSS | FC2 | R |
| | | | | | | VCC | VSS | A4# | RSVD | VSS | INIT# | SMI# | TESTHI11 | P |
| | | | | | | VCC | VSS | VSS | RSVD | RSVD | VSS | IGNNE# | PWRGOOD | N |
| | | | | | | VCC | VSS | REQ2# | A5# | A7# | STPCLK# | THER- MTRIP# | VSS | M |
| | | | | | | VCC | VSS | VSS | A3# | A6# | VSS | TESTHI13 | LINT1 | L |
| | | | | | | VCC | VSS | REQ3# | VSS | REQ0# | A20M# | VSS | LINT0 | K |
| VCC | VCC | VCC | VCC | VCC | VCC | VCC | VSS | REQ4# | REQ1# | VSS | FC22 | COMP4 | VTT_OUT_ LEFT | J |
| VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | TESTHI10 | RSP# | VSS | GTLREF1 | GTLREF0 | H |
| D29# | D27# | DSTBN1# | DBI1# | RSVD | D16# | BPRI# | DEFER# | RSVD | FC7 | TESTHI9 | TESTHI8 | FC1 | VSS | G |
| D28# | VSS | D24# | D23# | VSS | D18# | D17# | VSS | IMPSEL | RS1# | VSS | BR0# | FC5 | | F |
| VSS | D26# | DSTBP1# | VSS | D21# | D19# | VSS | RSVD | RSVD | FC20 | HITM# | TRDY# | VSS | | E |
| RSVD | D25# | VSS | D15# | D22# | VSS | D12# | D20# | VSS | VSS | HIT# | VSS | ADS# | RSVD | D |
| D52# | VSS | D14# | D11# | VSS | RSVD | DSTBN0# | VSS | D3# | D1# | VSS | LOCK# | BNR# | DRDY# | C |
| VSS | FC19 | D13# | VSS | D10# | DSTBP0# | VSS | D6# | D5# | VSS | D0# | RS0# | DBSY# | VSS | B |
| D50# | COMP0 | VSS | D9# | D8# | VSS | DBI0# | D7# | VSS | D4# | D2# | RS2# | VSS | | A |
| 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |

**Table 23. Alphabetical Land Assignments**

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| A10# | U6 | Source Synch | Input/Output |
| A11# | T4 | Source Synch | Input/Output |
| A12# | U5 | Source Synch | Input/Output |
| A13# | U4 | Source Synch | Input/Output |
| A14# | V5 | Source Synch | Input/Output |
| A15# | V4 | Source Synch | Input/Output |
| A16# | W5 | Source Synch | Input/Output |
| A17# | AB6 | Source Synch | Input/Output |
| A18# | W6 | Source Synch | Input/Output |
| A19# | Y6 | Source Synch | Input/Output |
| A20# | Y4 | Source Synch | Input/Output |
| A20M# | K3 | Asynch GTL+ | Input |
| A21# | AA4 | Source Synch | Input/Output |
| A22# | AD6 | Source Synch | Input/Output |
| A23# | AA5 | Source Synch | Input/Output |
| A24# | AB5 | Source Synch | Input/Output |
| A25# | AC5 | Source Synch | Input/Output |
| A26# | AB4 | Source Synch | Input/Output |
| A27# | AF5 | Source Synch | Input/Output |
| A28# | AF4 | Source Synch | Input/Output |
| A29# | AG6 | Source Synch | Input/Output |
| A3# | L5 | Source Synch | Input/Output |
| A30# | AG4 | Source Synch | Input/Output |
| A31# | AG5 | Source Synch | Input/Output |
| A32# | AH4 | Source Synch | Input/Output |
| A33# | AH5 | Source Synch | Input/Output |
| A34# | AJ5 | Source Synch | Input/Output |
| A35# | AJ6 | Source Synch | Input/Output |
| A4# | P6 | Source Synch | Input/Output |
| A5# | M5 | Source Synch | Input/Output |
| A6# | L4 | Source Synch | Input/Output |
| A7# | M4 | Source Synch | Input/Output |
| A8# | R4 | Source Synch | Input/Output |
| A9# | T5 | Source Synch | Input/Output |
| ADS# | D2 | Common Clock | Input/Output |
| ADSTB0# | R6 | Source Synch | Input/Output |
| ADSTB1# | AD5 | Source Synch | Input/Output |
| AP0# | U2 | Common Clock | Input/Output |
| AP1# | U3 | Common Clock | Input/Output |

**Table 23. Alphabetical Land Assignments**

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| BCLK0 | F28 | Clock | Input |
| BCLK1 | G28 | Clock | Input |
| BINIT# | AD3 | Common Clock | Input/Output |
| BNR# | C2 | Common Clock | Input/Output |
| BOOTSELECT | Y1 | Power/Other | Input |
| BPM0# | AJ2 | Common Clock | Input/Output |
| BPM1# | AJ1 | Common Clock | Input/Output |
| BPM2# | AD2 | Common Clock | Input/Output |
| BPM3# | AG2 | Common Clock | Input/Output |
| BPM4# | AF2 | Common Clock | Input/Output |
| BPM5# | AG3 | Common Clock | Input/Output |
| BPRI# | G8 | Common Clock | Input |
| BR0# | F3 | Common Clock | Input/Output |
| BSEL0 | G29 | Power/Other | Output |
| BSEL1 | H30 | Power/Other | Output |
| BSEL2 | G30 | Power/Other | Output |
| COMP0 | A13 | Power/Other | Input |
| COMP1 | T1 | Power/Other | Input |
| COMP4 | J2 | Power/Other | Input |
| COMP5 | T2 | Power/Other | Input |
| D0# | B4 | Source Synch | Input/Output |
| D1# | C5 | Source Synch | Input/Output |
| D10# | B10 | Source Synch | Input/Output |
| D11# | C11 | Source Synch | Input/Output |
| D12# | D8 | Source Synch | Input/Output |
| D13# | B12 | Source Synch | Input/Output |
| D14# | C12 | Source Synch | Input/Output |
| D15# | D11 | Source Synch | Input/Output |
| D16# | G9 | Source Synch | Input/Output |
| D17# | F8 | Source Synch | Input/Output |
| D18# | F9 | Source Synch | Input/Output |
| D19# | E9 | Source Synch | Input/Output |
| D2# | A4 | Source Synch | Input/Output |
| D20# | D7 | Source Synch | Input/Output |
| D21# | E10 | Source Synch | Input/Output |
| D22# | D10 | Source Synch | Input/Output |
| D23# | F11 | Source Synch | Input/Output |
| D24# | F12 | Source Synch | Input/Output |
| D25# | D13 | Source Synch | Input/Output |

## Table 23. Alphabetical Land Assignments

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| D26# | E13 | Source Synch | Input/Output |
| D27# | G13 | Source Synch | Input/Output |
| D28# | F14 | Source Synch | Input/Output |
| D29# | G14 | Source Synch | Input/Output |
| D3# | C6 | Source Synch | Input/Output |
| D30# | F15 | Source Synch | Input/Output |
| D31# | G15 | Source Synch | Input/Output |
| D32# | G16 | Source Synch | Input/Output |
| D33# | E15 | Source Synch | Input/Output |
| D34# | E16 | Source Synch | Input/Output |
| D35# | G18 | Source Synch | Input/Output |
| D36# | G17 | Source Synch | Input/Output |
| D37# | F17 | Source Synch | Input/Output |
| D38# | F18 | Source Synch | Input/Output |
| D39# | E18 | Source Synch | Input/Output |
| D4# | A5 | Source Synch | Input/Output |
| D40# | E19 | Source Synch | Input/Output |
| D41# | F20 | Source Synch | Input/Output |
| D42# | E21 | Source Synch | Input/Output |
| D43# | F21 | Source Synch | Input/Output |
| D44# | G21 | Source Synch | Input/Output |
| D45# | E22 | Source Synch | Input/Output |
| D46# | D22 | Source Synch | Input/Output |
| D47# | G22 | Source Synch | Input/Output |
| D48# | D20 | Source Synch | Input/Output |
| D49# | D17 | Source Synch | Input/Output |
| D5# | B6 | Source Synch | Input/Output |
| D50# | A14 | Source Synch | Input/Output |
| D51# | C15 | Source Synch | Input/Output |
| D52# | C14 | Source Synch | Input/Output |
| D53# | B15 | Source Synch | Input/Output |
| D54# | C18 | Source Synch | Input/Output |
| D55# | B16 | Source Synch | Input/Output |
| D56# | A17 | Source Synch | Input/Output |
| D57# | B18 | Source Synch | Input/Output |
| D58# | C21 | Source Synch | Input/Output |
| D59# | B21 | Source Synch | Input/Output |
| D6# | B7 | Source Synch | Input/Output |
| D60# | B19 | Source Synch | Input/Output |

## Table 23. Alphabetical Land Assignments

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| D61# | A19 | Source Synch | Input/Output |
| D62# | A22 | Source Synch | Input/Output |
| D63# | B22 | Source Synch | Input/Output |
| D7# | A7 | Source Synch | Input/Output |
| D8# | A10 | Source Synch | Input/Output |
| D9# | A11 | Source Synch | Input/Output |
| DBI0# | A8 | Source Synch | Input/Output |
| DBI1# | G11 | Source Synch | Input/Output |
| DBI2# | D19 | Source Synch | Input/Output |
| DBI3# | C20 | Source Synch | Input/Output |
| DBR# | AC2 | Power/Other | Output |
| DBSY# | B2 | Common Clock | Input/Output |
| DEFER# | G7 | Common Clock | Input |
| DP0# | J16 | Common Clock | Input/Output |
| DP1# | H15 | Common Clock | Input/Output |
| DP2# | H16 | Common Clock | Input/Output |
| DP3# | J17 | Common Clock | Input/Output |
| DRDY# | C1 | Common Clock | Input/Output |
| DSTBN0# | C8 | Source Synch | Input/Output |
| DSTBN1# | G12 | Source Synch | Input/Output |
| DSTBN2# | G20 | Source Synch | Input/Output |
| DSTBN3# | A16 | Source Synch | Input/Output |
| DSTBP0# | B9 | Source Synch | Input/Output |
| DSTBP1# | E12 | Source Synch | Input/Output |
| DSTBP2# | G19 | Source Synch | Input/Output |
| DSTBP3# | C17 | Source Synch | Input/Output |
| FC1 | G2 | Power/Other | Input |
| FC11 | AM5 | Power/Other | Output |
| FC12 | AM7 | Power/Other | Output |
| FC15 | H29 | Power/Other | Output |
| FC16 | AN7 | Power/Other | Output |
| FC2 | R1 | Power/Other | Input |
| FC5 | F2 | Common Clock | Input |
| FC7 | G5 | Source Synch | Output |
| FC8 | AK6 | Power/Other | Output |
| FC10 | E24 | Power/Other | Output |
| FC17 | Y3 | Power/Other | Output |
| FC22 | J3 | Power/Other | Output |
| FC19 | B13 | Power/Other | Output |

**Table 23. Alphabetical Land Assignments**

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| FC18 | AE3 | Power/Other | Output |
| FC20 | E5 | Power/Other | Output |
| FC9 | D23 | Power/Other | Output |
| FERR#/PBE# | R3 | Asynch GTL+ | Output |
| GTLREF0 | H1 | Power/Other | Input |
| GTLREF1 | H2 | Power/Other | Input |
| HIT# | D4 | Common Clock | Input/Output |
| HITM# | E4 | Common Clock | Input/Output |
| IERR# | AB2 | Asynch GTL+ | Output |
| IGNNE# | N2 | Asynch GTL+ | Input |
| IMPSEL | F6 | Power/Other | Input |
| INIT# | P3 | Asynch GTL+ | Input |
| ITP_CLK0 | AK3 | TAP | Input |
| ITP_CLK1 | AJ3 | TAP | Input |
| LINT0 | K1 | Asynch GTL+ | Input |
| LINT1 | L1 | Asynch GTL+ | Input |
| LL_ID0 | V2 | Power/Other | Output |
| LL_ID1 | AA2 | Power/Other | Output |
| LOCK# | C3 | Common Clock | Input/Output |
| MCERR# | AB3 | Common Clock | Input/Output |
| MSID0 | W1 | Power/Other | Output |
| MSID1 | V1 | Power/Other | Output |
| PROCHOT# | AL2 | Asynch GTL+ | Input/Output |
| PWRGOOD | N1 | Power/Other | Input |
| REQ0# | K4 | Source Synch | Input/Output |
| REQ1# | J5 | Source Synch | Input/Output |
| REQ2# | M6 | Source Synch | Input/Output |
| REQ3# | K6 | Source Synch | Input/Output |
| REQ4# | J6 | Source Synch | Input/Output |
| RESERVED | A20 | | |
| RESERVED | AC4 | | |
| RESERVED | AE4 | | |
| RESERVED | AE6 | | |
| RESERVED | AH2 | | |
| RESERVED | C9 | | |
| RESERVED | D1 | | |
| RESERVED | D14 | | |
| RESERVED | D16 | | |
| RESERVED | E23 | | |

**Table 23. Alphabetical Land Assignments**

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| RESERVED | E6 | | |
| RESERVED | E7 | | |
| RESERVED | F23 | | |
| RESERVED | F29 | | |
| RESERVED | G10 | | |
| RESERVED | G6 | | |
| RESERVED | N4 | | |
| RESERVED | N5 | | |
| RESERVED | P5 | | |
| RESET# | G23 | Common Clock | Input |
| RS0# | B3 | Common Clock | Input |
| RS1# | F5 | Common Clock | Input |
| RS2# | A3 | Common Clock | Input |
| RSP# | H4 | Common Clock | Input |
| SKTOCC# | AE8 | Power/Other | Output |
| SMI# | P2 | Asynch GTL+ | Input |
| STPCLK# | M3 | Asynch GTL+ | Input |
| TCK | AE1 | TAP | Input |
| TDI | AD1 | TAP | Input |
| TDO | AF1 | TAP | Output |
| TESTHI0 | F26 | Power/Other | Input |
| TESTHI1 | W3 | Power/Other | Input |
| TESTHI10 | H5 | Power/Other | Input |
| TESTHI11 | P1 | Power/Other | Input |
| TESTHI12 | W2 | Power/Other | Input |
| TESTHI13 | L2 | Asynch GTL+ | Input |
| TESTHI2 | F25 | Power/Other | Input |
| TESTHI3 | G25 | Power/Other | Input |
| TESTHI4 | G27 | Power/Other | Input |
| TESTHI5 | G26 | Power/Other | Input |
| TESTHI6 | G24 | Power/Other | Input |
| TESTHI7 | F24 | Power/Other | Input |
| TESTHI8 | G3 | Power/Other | Input |
| TESTHI9 | G4 | Power/Other | Input |
| THERMDA | AL1 | Power/Other | |
| THERMDC | AK1 | Power/Other | |
| THERMTRIP# | M2 | Asynch GTL+ | Output |
| TMS | AC1 | TAP | Input |
| TRDY# | E3 | Common Clock | Input |

**Table 23. Alphabetical Land Assignments**

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| TRST# | AG1 | TAP | Input |
| VCC | AA8 | Power/Other | |
| VCC | AB8 | Power/Other | |
| VCC | AC23 | Power/Other | |
| VCC | AC24 | Power/Other | |
| VCC | AC25 | Power/Other | |
| VCC | AC26 | Power/Other | |
| VCC | AC27 | Power/Other | |
| VCC | AC28 | Power/Other | |
| VCC | AC29 | Power/Other | |
| VCC | AC30 | Power/Other | |
| VCC | AC8 | Power/Other | |
| VCC | AD23 | Power/Other | |
| VCC | AD24 | Power/Other | |
| VCC | AD25 | Power/Other | |
| VCC | AD26 | Power/Other | |
| VCC | AD27 | Power/Other | |
| VCC | AD28 | Power/Other | |
| VCC | AD29 | Power/Other | |
| VCC | AD30 | Power/Other | |
| VCC | AD8 | Power/Other | |
| VCC | AE11 | Power/Other | |
| VCC | AE12 | Power/Other | |
| VCC | AE14 | Power/Other | |
| VCC | AE15 | Power/Other | |
| VCC | AE18 | Power/Other | |
| VCC | AE19 | Power/Other | |
| VCC | AE21 | Power/Other | |
| VCC | AE22 | Power/Other | |
| VCC | AE23 | Power/Other | |
| VCC | AE9 | Power/Other | |
| VCC | AF11 | Power/Other | |
| VCC | AF12 | Power/Other | |
| VCC | AF14 | Power/Other | |
| VCC | AF15 | Power/Other | |
| VCC | AF18 | Power/Other | |
| VCC | AF19 | Power/Other | |
| VCC | AF21 | Power/Other | |
| VCC | AF22 | Power/Other | |

**Table 23. Alphabetical Land Assignments**

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| VCC | AF8 | Power/Other | |
| VCC | AF9 | Power/Other | |
| VCC | AG11 | Power/Other | |
| VCC | AG12 | Power/Other | |
| VCC | AG14 | Power/Other | |
| VCC | AG15 | Power/Other | |
| VCC | AG18 | Power/Other | |
| VCC | AG19 | Power/Other | |
| VCC | AG21 | Power/Other | |
| VCC | AG22 | Power/Other | |
| VCC | AG25 | Power/Other | |
| VCC | AG26 | Power/Other | |
| VCC | AG27 | Power/Other | |
| VCC | AG28 | Power/Other | |
| VCC | AG29 | Power/Other | |
| VCC | AG30 | Power/Other | |
| VCC | AG8 | Power/Other | |
| VCC | AG9 | Power/Other | |
| VCC | AH11 | Power/Other | |
| VCC | AH12 | Power/Other | |
| VCC | AH14 | Power/Other | |
| VCC | AH15 | Power/Other | |
| VCC | AH18 | Power/Other | |
| VCC | AH19 | Power/Other | |
| VCC | AH21 | Power/Other | |
| VCC | AH22 | Power/Other | |
| VCC | AH25 | Power/Other | |
| VCC | AH26 | Power/Other | |
| VCC | AH27 | Power/Other | |
| VCC | AH28 | Power/Other | |
| VCC | AH29 | Power/Other | |
| VCC | AH30 | Power/Other | |
| VCC | AH8 | Power/Other | |
| VCC | AH9 | Power/Other | |
| VCC | AJ11 | Power/Other | |
| VCC | AJ12 | Power/Other | |
| VCC | AJ14 | Power/Other | |
| VCC | AJ15 | Power/Other | |
| VCC | AJ18 | Power/Other | |

**Table 23. Alphabetical Land Assignments**

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| VCC | AJ19 | Power/Other | |
| VCC | AJ21 | Power/Other | |
| VCC | AJ22 | Power/Other | |
| VCC | AJ25 | Power/Other | |
| VCC | AJ26 | Power/Other | |
| VCC | AJ8 | Power/Other | |
| VCC | AJ9 | Power/Other | |
| VCC | AK11 | Power/Other | |
| VCC | AK12 | Power/Other | |
| VCC | AK14 | Power/Other | |
| VCC | AK15 | Power/Other | |
| VCC | AK18 | Power/Other | |
| VCC | AK19 | Power/Other | |
| VCC | AK21 | Power/Other | |
| VCC | AK22 | Power/Other | |
| VCC | AK25 | Power/Other | |
| VCC | AK26 | Power/Other | |
| VCC | AK8 | Power/Other | |
| VCC | AK9 | Power/Other | |
| VCC | AL11 | Power/Other | |
| VCC | AL12 | Power/Other | |
| VCC | AL14 | Power/Other | |
| VCC | AL15 | Power/Other | |
| VCC | AL18 | Power/Other | |
| VCC | AL19 | Power/Other | |
| VCC | AL21 | Power/Other | |
| VCC | AL22 | Power/Other | |
| VCC | AL25 | Power/Other | |
| VCC | AL26 | Power/Other | |
| VCC | AL29 | Power/Other | |
| VCC | AL30 | Power/Other | |
| VCC | AL8 | Power/Other | |
| VCC | AL9 | Power/Other | |
| VCC | AM11 | Power/Other | |
| VCC | AM12 | Power/Other | |
| VCC | AM14 | Power/Other | |
| VCC | AM15 | Power/Other | |
| VCC | AM18 | Power/Other | |
| VCC | AM19 | Power/Other | |

**Table 23. Alphabetical Land Assignments**

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| VCC | AM21 | Power/Other | |
| VCC | AM22 | Power/Other | |
| VCC | AM25 | Power/Other | |
| VCC | AM26 | Power/Other | |
| VCC | AM29 | Power/Other | |
| VCC | AM30 | Power/Other | |
| VCC | AM8 | Power/Other | |
| VCC | AM9 | Power/Other | |
| VCC | AN11 | Power/Other | |
| VCC | AN12 | Power/Other | |
| VCC | AN14 | Power/Other | |
| VCC | AN15 | Power/Other | |
| VCC | AN18 | Power/Other | |
| VCC | AN19 | Power/Other | |
| VCC | AN21 | Power/Other | |
| VCC | AN22 | Power/Other | |
| VCC | AN25 | Power/Other | |
| VCC | AN26 | Power/Other | |
| VCC | AN29 | Power/Other | |
| VCC | AN30 | Power/Other | |
| VCC | AN8 | Power/Other | |
| VCC | AN9 | Power/Other | |
| VCC | J10 | Power/Other | |
| VCC | J11 | Power/Other | |
| VCC | J12 | Power/Other | |
| VCC | J13 | Power/Other | |
| VCC | J14 | Power/Other | |
| VCC | J15 | Power/Other | |
| VCC | J18 | Power/Other | |
| VCC | J19 | Power/Other | |
| VCC | J20 | Power/Other | |
| VCC | J21 | Power/Other | |
| VCC | J22 | Power/Other | |
| VCC | J23 | Power/Other | |
| VCC | J24 | Power/Other | |
| VCC | J25 | Power/Other | |
| VCC | J26 | Power/Other | |
| VCC | J27 | Power/Other | |
| VCC | J28 | Power/Other | |

**Table 23. Alphabetical Land Assignments**

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| VCC | J29 | Power/Other | |
| VCC | J30 | Power/Other | |
| VCC | J8 | Power/Other | |
| VCC | J9 | Power/Other | |
| VCC | K23 | Power/Other | |
| VCC | K24 | Power/Other | |
| VCC | K25 | Power/Other | |
| VCC | K26 | Power/Other | |
| VCC | K27 | Power/Other | |
| VCC | K28 | Power/Other | |
| VCC | K29 | Power/Other | |
| VCC | K30 | Power/Other | |
| VCC | K8 | Power/Other | |
| VCC | L8 | Power/Other | |
| VCC | M23 | Power/Other | |
| VCC | M24 | Power/Other | |
| VCC | M25 | Power/Other | |
| VCC | M26 | Power/Other | |
| VCC | M27 | Power/Other | |
| VCC | M28 | Power/Other | |
| VCC | M29 | Power/Other | |
| VCC | M30 | Power/Other | |
| VCC | M8 | Power/Other | |
| VCC | N23 | Power/Other | |
| VCC | N24 | Power/Other | |
| VCC | N25 | Power/Other | |
| VCC | N26 | Power/Other | |
| VCC | N27 | Power/Other | |
| VCC | N28 | Power/Other | |
| VCC | N29 | Power/Other | |
| VCC | N30 | Power/Other | |
| VCC | N8 | Power/Other | |
| VCC | P8 | Power/Other | |
| VCC | R8 | Power/Other | |
| VCC | T23 | Power/Other | |
| VCC | T24 | Power/Other | |
| VCC | T25 | Power/Other | |
| VCC | T26 | Power/Other | |
| VCC | T27 | Power/Other | |

**Table 23. Alphabetical Land Assignments**

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| VCC | T28 | Power/Other | |
| VCC | T29 | Power/Other | |
| VCC | T30 | Power/Other | |
| VCC | T8 | Power/Other | |
| VCC | U23 | Power/Other | |
| VCC | U24 | Power/Other | |
| VCC | U25 | Power/Other | |
| VCC | U26 | Power/Other | |
| VCC | U27 | Power/Other | |
| VCC | U28 | Power/Other | |
| VCC | U29 | Power/Other | |
| VCC | U30 | Power/Other | |
| VCC | U8 | Power/Other | |
| VCC | V8 | Power/Other | |
| VCC | W23 | Power/Other | |
| VCC | W24 | Power/Other | |
| VCC | W25 | Power/Other | |
| VCC | W26 | Power/Other | |
| VCC | W27 | Power/Other | |
| VCC | W28 | Power/Other | |
| VCC | W29 | Power/Other | |
| VCC | W30 | Power/Other | |
| VCC | W8 | Power/Other | |
| VCC | Y23 | Power/Other | |
| VCC | Y24 | Power/Other | |
| VCC | Y25 | Power/Other | |
| VCC | Y26 | Power/Other | |
| VCC | Y27 | Power/Other | |
| VCC | Y28 | Power/Other | |
| VCC | Y29 | Power/Other | |
| VCC | Y30 | Power/Other | |
| VCC | Y8 | Power/Other | |
| VCC_MB_REGULATION | AN5 | Power/Other | Output |
| VCC_SENSE | AN3 | Power/Other | Output |
| VCCA | A23 | Power/Other | |
| VCCIOPLL | C23 | Power/Other | |
| VID0 | AM2 | Power/Other | Output |
| VID1 | AL5 | Power/Other | Output |
| VID2 | AM3 | Power/Other | Output |

## Table 23. Alphabetical Land Assignments

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| VID3 | AL6 | Power/Other | Output |
| VID4 | AK4 | Power/Other | Output |
| VID5 | AL4 | Power/Other | Output |
| VSS | B1 | Power/Other | |
| VSS | B11 | Power/Other | |
| VSS | B14 | Power/Other | |
| VSS | B17 | Power/Other | |
| VSS | B20 | Power/Other | |
| VSS | B24 | Power/Other | |
| VSS | B5 | Power/Other | |
| VSS | B8 | Power/Other | |
| VSS | A12 | Power/Other | |
| VSS | A15 | Power/Other | |
| VSS | A18 | Power/Other | |
| VSS | A2 | Power/Other | |
| VSS | A21 | Power/Other | |
| VSS | A24 | Power/Other | |
| VSS | A6 | Power/Other | |
| VSS | A9 | Power/Other | |
| VSS | AA23 | Power/Other | |
| VSS | AA24 | Power/Other | |
| VSS | AA25 | Power/Other | |
| VSS | AA26 | Power/Other | |
| VSS | AA27 | Power/Other | |
| VSS | AA28 | Power/Other | |
| VSS | AA29 | Power/Other | |
| VSS | AA3 | Power/Other | |
| VSS | AA30 | Power/Other | |
| VSS | AA6 | Power/Other | |
| VSS | AA7 | Power/Other | |
| VSS | AB1 | Power/Other | |
| VSS | AB23 | Power/Other | |
| VSS | AB24 | Power/Other | |
| VSS | AB25 | Power/Other | |
| VSS | AB26 | Power/Other | |
| VSS | AB27 | Power/Other | |
| VSS | AB28 | Power/Other | |
| VSS | AB29 | Power/Other | |
| VSS | AB30 | Power/Other | |

## Table 23. Alphabetical Land Assignments

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | AB7 | Power/Other | |
| VSS | AC3 | Power/Other | |
| VSS | AC6 | Power/Other | |
| VSS | AC7 | Power/Other | |
| VSS | AD4 | Power/Other | |
| VSS | AD7 | Power/Other | |
| VSS | AE10 | Power/Other | |
| VSS | AE13 | Power/Other | |
| VSS | AE16 | Power/Other | |
| VSS | AE17 | Power/Other | |
| VSS | AE2 | Power/Other | |
| VSS | AE20 | Power/Other | |
| VSS | AE24 | Power/Other | |
| VSS | AE25 | Power/Other | |
| VSS | AE26 | Power/Other | |
| VSS | AE27 | Power/Other | |
| VSS | AE28 | Power/Other | |
| VSS | AE29 | Power/Other | |
| VSS | AE30 | Power/Other | |
| VSS | AE5 | Power/Other | |
| VSS | AE7 | Power/Other | |
| VSS | AF10 | Power/Other | |
| VSS | AF13 | Power/Other | |
| VSS | AF16 | Power/Other | |
| VSS | AF17 | Power/Other | |
| VSS | AF20 | Power/Other | |
| VSS | AF23 | Power/Other | |
| VSS | AF24 | Power/Other | |
| VSS | AF25 | Power/Other | |
| VSS | AF26 | Power/Other | |
| VSS | AF27 | Power/Other | |
| VSS | AF28 | Power/Other | |
| VSS | AF29 | Power/Other | |
| VSS | AF3 | Power/Other | |
| VSS | AF30 | Power/Other | |
| VSS | AF6 | Power/Other | |
| VSS | AF7 | Power/Other | |
| VSS | AG10 | Power/Other | |
| VSS | AG13 | Power/Other | |

## Table 23. Alphabetical Land Assignments

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | AG16 | Power/Other | |
| VSS | AG17 | Power/Other | |
| VSS | AG20 | Power/Other | |
| VSS | AG23 | Power/Other | |
| VSS | AG24 | Power/Other | |
| VSS | AG7 | Power/Other | |
| VSS | AH1 | Power/Other | |
| VSS | AH10 | Power/Other | |
| VSS | AH13 | Power/Other | |
| VSS | AH16 | Power/Other | |
| VSS | AH17 | Power/Other | |
| VSS | AH20 | Power/Other | |
| VSS | AH23 | Power/Other | |
| VSS | AH24 | Power/Other | |
| VSS | AH3 | Power/Other | |
| VSS | AH6 | Power/Other | |
| VSS | AH7 | Power/Other | |
| VSS | AJ10 | Power/Other | |
| VSS | AJ13 | Power/Other | |
| VSS | AJ16 | Power/Other | |
| VSS | AJ17 | Power/Other | |
| VSS | AJ20 | Power/Other | |
| VSS | AJ23 | Power/Other | |
| VSS | AJ24 | Power/Other | |
| VSS | AJ27 | Power/Other | |
| VSS | AJ28 | Power/Other | |
| VSS | AJ29 | Power/Other | |
| VSS | AJ30 | Power/Other | |
| VSS | AJ4 | Power/Other | |
| VSS | AJ7 | Power/Other | |
| VSS | AK10 | Power/Other | |
| VSS | AK13 | Power/Other | |
| VSS | AK16 | Power/Other | |
| VSS | AK17 | Power/Other | |
| VSS | AK2 | Power/Other | |
| VSS | AK20 | Power/Other | |
| VSS | AK23 | Power/Other | |
| VSS | AK24 | Power/Other | |
| VSS | AK27 | Power/Other | |

## Table 23. Alphabetical Land Assignments

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | AK28 | Power/Other | |
| VSS | AK29 | Power/Other | |
| VSS | AK30 | Power/Other | |
| VSS | AK5 | Power/Other | |
| VSS | AK7 | Power/Other | |
| VSS | AL10 | Power/Other | |
| VSS | AL13 | Power/Other | |
| VSS | AL16 | Power/Other | |
| VSS | AL17 | Power/Other | |
| VSS | AL20 | Power/Other | |
| VSS | AL23 | Power/Other | |
| VSS | AL24 | Power/Other | |
| VSS | AL27 | Power/Other | |
| VSS | AL28 | Power/Other | |
| VSS | AL3 | Power/Other | |
| VSS | AL7 | Power/Other | |
| VSS | AM1 | Power/Other | |
| VSS | AM10 | Power/Other | |
| VSS | AM13 | Power/Other | |
| VSS | AM16 | Power/Other | |
| VSS | AM17 | Power/Other | |
| VSS | AM20 | Power/Other | |
| VSS | AM23 | Power/Other | |
| VSS | AM24 | Power/Other | |
| VSS | AM27 | Power/Other | |
| VSS | AM28 | Power/Other | |
| VSS | AM4 | Power/Other | |
| VSS | AN1 | Power/Other | |
| VSS | AN10 | Power/Other | |
| VSS | AN13 | Power/Other | |
| VSS | AN16 | Power/Other | |
| VSS | AN17 | Power/Other | |
| VSS | AN2 | Power/Other | |
| VSS | AN20 | Power/Other | |
| VSS | AN23 | Power/Other | |
| VSS | AN24 | Power/Other | |
| VSS | AN27 | Power/Other | |
| VSS | AN28 | Power/Other | |
| VSS | C10 | Power/Other | |

## Table 23. Alphabetical Land Assignments

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | C13 | Power/Other | |
| VSS | C16 | Power/Other | |
| VSS | C19 | Power/Other | |
| VSS | C22 | Power/Other | |
| VSS | C24 | Power/Other | |
| VSS | C4 | Power/Other | |
| VSS | C7 | Power/Other | |
| VSS | D12 | Power/Other | |
| VSS | D15 | Power/Other | |
| VSS | D18 | Power/Other | |
| VSS | D21 | Power/Other | |
| VSS | D24 | Power/Other | |
| VSS | D3 | Power/Other | |
| VSS | D5 | Power/Other | |
| VSS | D6 | Power/Other | |
| VSS | D9 | Power/Other | |
| VSS | E11 | Power/Other | |
| VSS | E14 | Power/Other | |
| VSS | E17 | Power/Other | |
| VSS | E2 | Power/Other | |
| VSS | E20 | Power/Other | |
| VSS | E25 | Power/Other | |
| VSS | E26 | Power/Other | |
| VSS | E27 | Power/Other | |
| VSS | E28 | Power/Other | |
| VSS | E29 | Power/Other | |
| VSS | E8 | Power/Other | |
| VSS | F10 | Power/Other | |
| VSS | F13 | Power/Other | |
| VSS | F16 | Power/Other | |
| VSS | F19 | Power/Other | |
| VSS | F22 | Power/Other | |
| VSS | F4 | Power/Other | |
| VSS | F7 | Power/Other | |
| VSS | G1 | Power/Other | |
| VSS | H10 | Power/Other | |
| VSS | H11 | Power/Other | |
| VSS | H12 | Power/Other | |
| VSS | H13 | Power/Other | |

## Table 23. Alphabetical Land Assignments

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | H14 | Power/Other | |
| VSS | H17 | Power/Other | |
| VSS | H18 | Power/Other | |
| VSS | H19 | Power/Other | |
| VSS | H20 | Power/Other | |
| VSS | H21 | Power/Other | |
| VSS | H22 | Power/Other | |
| VSS | H23 | Power/Other | |
| VSS | H24 | Power/Other | |
| VSS | H25 | Power/Other | |
| VSS | H26 | Power/Other | |
| VSS | H27 | Power/Other | |
| VSS | H28 | Power/Other | |
| VSS | H3 | Power/Other | |
| VSS | H6 | Power/Other | |
| VSS | H7 | Power/Other | |
| VSS | H8 | Power/Other | |
| VSS | H9 | Power/Other | |
| VSS | J4 | Power/Other | |
| VSS | J7 | Power/Other | |
| VSS | K2 | Power/Other | |
| VSS | K5 | Power/Other | |
| VSS | K7 | Power/Other | |
| VSS | L23 | Power/Other | |
| VSS | L24 | Power/Other | |
| VSS | L25 | Power/Other | |
| VSS | L26 | Power/Other | |
| VSS | L27 | Power/Other | |
| VSS | L28 | Power/Other | |
| VSS | L29 | Power/Other | |
| VSS | L3 | Power/Other | |
| VSS | L30 | Power/Other | |
| VSS | L6 | Power/Other | |
| VSS | L7 | Power/Other | |
| VSS | M1 | Power/Other | |
| VSS | M7 | Power/Other | |
| VSS | N3 | Power/Other | |
| VSS | N6 | Power/Other | |
| VSS | N7 | Power/Other | |

## Table 23. Alphabetical Land Assignments

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | P23 | Power/Other | |
| VSS | P24 | Power/Other | |
| VSS | P25 | Power/Other | |
| VSS | P26 | Power/Other | |
| VSS | P27 | Power/Other | |
| VSS | P28 | Power/Other | |
| VSS | P29 | Power/Other | |
| VSS | P30 | Power/Other | |
| VSS | P4 | Power/Other | |
| VSS | P7 | Power/Other | |
| VSS | R2 | Power/Other | |
| VSS | R23 | Power/Other | |
| VSS | R24 | Power/Other | |
| VSS | R25 | Power/Other | |
| VSS | R26 | Power/Other | |
| VSS | R27 | Power/Other | |
| VSS | R28 | Power/Other | |
| VSS | R29 | Power/Other | |
| VSS | R30 | Power/Other | |
| VSS | R5 | Power/Other | |
| VSS | R7 | Power/Other | |
| VSS | T3 | Power/Other | |
| VSS | T6 | Power/Other | |
| VSS | T7 | Power/Other | |
| VSS | U1 | Power/Other | |
| VSS | U7 | Power/Other | |
| VSS | V23 | Power/Other | |
| VSS | V24 | Power/Other | |
| VSS | V25 | Power/Other | |
| VSS | V26 | Power/Other | |
| VSS | V27 | Power/Other | |
| VSS | V28 | Power/Other | |
| VSS | V29 | Power/Other | |
| VSS | V3 | Power/Other | |
| VSS | V30 | Power/Other | |
| VSS | V6 | Power/Other | |
| VSS | V7 | Power/Other | |
| VSS | W4 | Power/Other | |
| VSS | W7 | Power/Other | |

## Table 23. Alphabetical Land Assignments

| Land Name | Land # | Signal Buffer Type | Direction |
|---|---|---|---|
| VSS | Y2 | Power/Other | |
| VSS | Y5 | Power/Other | |
| VSS | Y7 | Power/Other | |
| VSS_MB_REGULATION | AN6 | Power/Other | Output |
| VSS_SENSE | AN4 | Power/Other | Output |
| VSSA | B23 | Power/Other | |
| VTT | B25 | Power/Other | |
| VTT | B26 | Power/Other | |
| VTT | B27 | Power/Other | |
| VTT | B28 | Power/Other | |
| VTT | B29 | Power/Other | |
| VTT | B30 | Power/Other | |
| VTT | A25 | Power/Other | |
| VTT | A26 | Power/Other | |
| VTT | A27 | Power/Other | |
| VTT | A28 | Power/Other | |
| VTT | A29 | Power/Other | |
| VTT | A30 | Power/Other | |
| VTT | C25 | Power/Other | |
| VTT | C26 | Power/Other | |
| VTT | C27 | Power/Other | |
| VTT | C28 | Power/Other | |
| VTT | C29 | Power/Other | |
| VTT | C30 | Power/Other | |
| VTT | D25 | Power/Other | |
| VTT | D26 | Power/Other | |
| VTT | D27 | Power/Other | |
| VTT | D28 | Power/Other | |
| VTT | D29 | Power/Other | |
| VTT | D30 | Power/Other | |
| VTT_OUT_LEFT | J1 | Power/Other | Output |
| VTT_OUT_RIGHT | AA1 | Power/Other | Output |
| VTT_SEL | F27 | Power/Other | Output |
| VTTPWRGD | AM6 | Power/Other | Input |

**Table 24.Numerical Land Assignment**

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| A10 | D08# | Source Synch | Input/Output |
| A11 | D09# | Source Synch | Input/Output |
| A12 | VSS | Power/Other | |
| A13 | COMP0 | Power/Other | Input |
| A14 | D50# | Source Synch | Input/Output |
| A15 | VSS | Power/Other | |
| A16 | DSTBN3# | Source Synch | Input/Output |
| A17 | D56# | Source Synch | Input/Output |
| A18 | VSS | Power/Other | |
| A19 | D61# | Source Synch | Input/Output |
| A2 | VSS | Power/Other | |
| A20 | RESERVED | | |
| A21 | VSS | Power/Other | |
| A22 | D62# | Source Synch | Input/Output |
| A23 | VCCA | Power/Other | |
| A24 | VSS | Power/Other | |
| A25 | VTT | Power/Other | |
| A26 | VTT | Power/Other | |
| A27 | VTT | Power/Other | |
| A28 | VTT | Power/Other | |
| A29 | VTT | Power/Other | |
| A3 | RS2# | Common Clock | Input |
| A30 | VTT | Power/Other | |
| A4 | D02# | Source Synch | Input/Output |
| A5 | D04# | Source Synch | Input/Output |
| A6 | VSS | Power/Other | |
| A7 | D07# | Source Synch | Input/Output |
| A8 | DBI0# | Source Synch | Input/Output |
| A9 | VSS | Power/Other | |
| AA1 | VTT_OUT_RIGHT | Power/Other | Output |
| AA2 | LL_ID1 | Power/Other | Output |
| AA23 | VSS | Power/Other | |
| AA24 | VSS | Power/Other | |
| AA25 | VSS | Power/Other | |
| AA26 | VSS | Power/Other | |
| AA27 | VSS | Power/Other | |
| AA28 | VSS | Power/Other | |
| AA29 | VSS | Power/Other | |
| AA3 | VSS | Power/Other | |
| AA30 | VSS | Power/Other | |

**Table 24.Numerical Land Assignment**

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| AA4 | A21# | Source Synch | Input/Output |
| AA5 | A23# | Source Synch | Input/Output |
| AA6 | VSS | Power/Other | |
| AA7 | VSS | Power/Other | |
| AA8 | VCC | Power/Other | |
| AB1 | VSS | Power/Other | |
| AB2 | IERR# | Asynch GTL+ | Output |
| AB23 | VSS | Power/Other | |
| AB24 | VSS | Power/Other | |
| AB25 | VSS | Power/Other | |
| AB26 | VSS | Power/Other | |
| AB27 | VSS | Power/Other | |
| AB28 | VSS | Power/Other | |
| AB29 | VSS | Power/Other | |
| AB3 | MCERR# | Common Clock | Input/Output |
| AB30 | VSS | Power/Other | |
| AB4 | A26# | Source Synch | Input/Output |
| AB5 | A24# | Source Synch | Input/Output |
| AB6 | A17# | Source Synch | Input/Output |
| AB7 | VSS | Power/Other | |
| AB8 | VCC | Power/Other | |
| AC1 | TMS | TAP | Input |
| AC2 | DBR# | Power/Other | Output |
| AC23 | VCC | Power/Other | |
| AC24 | VCC | Power/Other | |
| AC25 | VCC | Power/Other | |
| AC26 | VCC | Power/Other | |
| AC27 | VCC | Power/Other | |
| AC28 | VCC | Power/Other | |
| AC29 | VCC | Power/Other | |
| AC3 | VSS | Power/Other | |
| AC30 | VCC | Power/Other | |
| AC4 | RESERVED | | |
| AC5 | A25# | Source Synch | Input/Output |
| AC6 | VSS | Power/Other | |
| AC7 | VSS | Power/Other | |
| AC8 | VCC | Power/Other | |
| AD1 | TDI | TAP | Input |
| AD2 | BPM2# | Common Clock | Input/Output |
| AD23 | VCC | Power/Other | |

**Table 24. Numerical Land Assignment**

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| AD24 | VCC | Power/Other | |
| AD25 | VCC | Power/Other | |
| AD26 | VCC | Power/Other | |
| AD27 | VCC | Power/Other | |
| AD28 | VCC | Power/Other | |
| AD29 | VCC | Power/Other | |
| AD3 | BINIT# | Common Clock | Input/Output |
| AD30 | VCC | Power/Other | |
| AD4 | VSS | Power/Other | |
| AD5 | ADSTB1# | Source Synch | Input/Output |
| AD6 | A22# | Source Synch | Input/Output |
| AD7 | VSS | Power/Other | |
| AD8 | VCC | Power/Other | |
| AE1 | TCK | TAP | Input |
| AE10 | VSS | Power/Other | |
| AE11 | VCC | Power/Other | |
| AE12 | VCC | Power/Other | |
| AE13 | VSS | Power/Other | |
| AE14 | VCC | Power/Other | |
| AE15 | VCC | Power/Other | |
| AE16 | VSS | Power/Other | |
| AE17 | VSS | Power/Other | |
| AE18 | VCC | Power/Other | |
| AE19 | VCC | Power/Other | |
| AE2 | VSS | Power/Other | |
| AE20 | VSS | Power/Other | |
| AE21 | VCC | Power/Other | |
| AE22 | VCC | Power/Other | |
| AE23 | VCC | Power/Other | |
| AE24 | VSS | Power/Other | |
| AE25 | VSS | Power/Other | |
| AE26 | VSS | Power/Other | |
| AE27 | VSS | Power/Other | |
| AE28 | VSS | Power/Other | |
| AE29 | VSS | Power/Other | |
| AE3 | FC18 | Power/Other | Output |
| AE30 | VSS | Power/Other | |
| AE4 | RESERVED | | |
| AE5 | VSS | Power/Other | |
| AE6 | RESERVED | | |

**Table 24. Numerical Land Assignment**

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| AE7 | VSS | Power/Other | |
| AE8 | SKTOCC# | Power/Other | Output |
| AE9 | VCC | Power/Other | |
| AF1 | TDO | TAP | Output |
| AF10 | VSS | Power/Other | |
| AF11 | VCC | Power/Other | |
| AF12 | VCC | Power/Other | |
| AF13 | VSS | Power/Other | |
| AF14 | VCC | Power/Other | |
| AF15 | VCC | Power/Other | |
| AF16 | VSS | Power/Other | |
| AF17 | VSS | Power/Other | |
| AF18 | VCC | Power/Other | |
| AF19 | VCC | Power/Other | |
| AF2 | BPM4# | Common Clock | Input/Output |
| AF20 | VSS | Power/Other | |
| AF21 | VCC | Power/Other | |
| AF22 | VCC | Power/Other | |
| AF23 | VSS | Power/Other | |
| AF24 | VSS | Power/Other | |
| AF25 | VSS | Power/Other | |
| AF26 | VSS | Power/Other | |
| AF27 | VSS | Power/Other | |
| AF28 | VSS | Power/Other | |
| AF29 | VSS | Power/Other | |
| AF3 | VSS | Power/Other | |
| AF30 | VSS | Power/Other | |
| AF4 | A28# | Source Synch | Input/Output |
| AF5 | A27# | Source Synch | Input/Output |
| AF6 | VSS | Power/Other | |
| AF7 | VSS | Power/Other | |
| AF8 | VCC | Power/Other | |
| AF9 | VCC | Power/Other | |
| AG1 | TRST# | TAP | Input |
| AG10 | VSS | Power/Other | |
| AG11 | VCC | Power/Other | |
| AG12 | VCC | Power/Other | |
| AG13 | VSS | Power/Other | |
| AG14 | VCC | Power/Other | |
| AG15 | VCC | Power/Other | |

### Table 24. Numerical Land Assignment

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| AG16 | VSS | Power/Other | |
| AG17 | VSS | Power/Other | |
| AG18 | VCC | Power/Other | |
| AG19 | VCC | Power/Other | |
| AG2 | BPM3# | Common Clock | Input/Output |
| AG20 | VSS | Power/Other | |
| AG21 | VCC | Power/Other | |
| AG22 | VCC | Power/Other | |
| AG23 | VSS | Power/Other | |
| AG24 | VSS | Power/Other | |
| AG25 | VCC | Power/Other | |
| AG26 | VCC | Power/Other | |
| AG27 | VCC | Power/Other | |
| AG28 | VCC | Power/Other | |
| AG29 | VCC | Power/Other | |
| AG3 | BPM5# | Common Clock | Input/Output |
| AG30 | VCC | Power/Other | |
| AG4 | A30# | Source Synch | Input/Output |
| AG5 | A31# | Source Synch | Input/Output |
| AG6 | A29# | Source Synch | Input/Output |
| AG7 | VSS | Power/Other | |
| AG8 | VCC | Power/Other | |
| AG9 | VCC | Power/Other | |
| AH1 | VSS | Power/Other | |
| AH10 | VSS | Power/Other | |
| AH11 | VCC | Power/Other | |
| AH12 | VCC | Power/Other | |
| AH13 | VSS | Power/Other | |
| AH14 | VCC | Power/Other | |
| AH15 | VCC | Power/Other | |
| AH16 | VSS | Power/Other | |
| AH17 | VSS | Power/Other | |
| AH18 | VCC | Power/Other | |
| AH19 | VCC | Power/Other | |
| AH2 | RESERVED | | |
| AH20 | VSS | Power/Other | |
| AH21 | VCC | Power/Other | |
| AH22 | VCC | Power/Other | |
| AH23 | VSS | Power/Other | |
| AH24 | VSS | Power/Other | |

### Table 24. Numerical Land Assignment

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| AH25 | VCC | Power/Other | |
| AH26 | VCC | Power/Other | |
| AH27 | VCC | Power/Other | |
| AH28 | VCC | Power/Other | |
| AH29 | VCC | Power/Other | |
| AH3 | VSS | Power/Other | |
| AH30 | VCC | Power/Other | |
| AH4 | A32# | Source Synch | Input/Output |
| AH5 | A33# | Source Synch | Input/Output |
| AH6 | VSS | Power/Other | |
| AH7 | VSS | Power/Other | |
| AH8 | VCC | Power/Other | |
| AH9 | VCC | Power/Other | |
| AJ1 | BPM1# | Common Clock | Input/Output |
| AJ10 | VSS | Power/Other | |
| AJ11 | VCC | Power/Other | |
| AJ12 | VCC | Power/Other | |
| AJ13 | VSS | Power/Other | |
| AJ14 | VCC | Power/Other | |
| AJ15 | VCC | Power/Other | |
| AJ16 | VSS | Power/Other | |
| AJ17 | VSS | Power/Other | |
| AJ18 | VCC | Power/Other | |
| AJ19 | VCC | Power/Other | |
| AJ2 | BPM0# | Common Clock | Input/Output |
| AJ20 | VSS | Power/Other | |
| AJ21 | VCC | Power/Other | |
| AJ22 | VCC | Power/Other | |
| AJ23 | VSS | Power/Other | |
| AJ24 | VSS | Power/Other | |
| AJ25 | VCC | Power/Other | |
| AJ26 | VCC | Power/Other | |
| AJ27 | VSS | Power/Other | |
| AJ28 | VSS | Power/Other | |
| AJ29 | VSS | Power/Other | |
| AJ3 | ITP_CLK1 | TAP | Input |
| AJ30 | VSS | Power/Other | |
| AJ4 | VSS | Power/Other | |
| AJ5 | A34# | Source Synch | Input/Output |
| AJ6 | A35# | Source Synch | Input/Output |

## Table 24. Numerical Land Assignment

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| AJ7 | VSS | Power/Other | |
| AJ8 | VCC | Power/Other | |
| AJ9 | VCC | Power/Other | |
| AK1 | THERMDC | Power/Other | |
| AK10 | VSS | Power/Other | |
| AK11 | VCC | Power/Other | |
| AK12 | VCC | Power/Other | |
| AK13 | VSS | Power/Other | |
| AK14 | VCC | Power/Other | |
| AK15 | VCC | Power/Other | |
| AK16 | VSS | Power/Other | |
| AK17 | VSS | Power/Other | |
| AK18 | VCC | Power/Other | |
| AK19 | VCC | Power/Other | |
| AK2 | VSS | Power/Other | |
| AK20 | VSS | Power/Other | |
| AK21 | VCC | Power/Other | |
| AK22 | VCC | Power/Other | |
| AK23 | VSS | Power/Other | |
| AK24 | VSS | Power/Other | |
| AK25 | VCC | Power/Other | |
| AK26 | VCC | Power/Other | |
| AK27 | VSS | Power/Other | |
| AK28 | VSS | Power/Other | |
| AK29 | VSS | Power/Other | |
| AK3 | ITP_CLK0 | TAP | Input |
| AK30 | VSS | Power/Other | |
| AK4 | VID4 | Power/Other | Output |
| AK5 | VSS | Power/Other | |
| AK6 | FC8 | | |
| AK7 | VSS | Power/Other | |
| AK8 | VCC | Power/Other | |
| AK9 | VCC | Power/Other | |
| AL1 | THERMDA | Power/Other | |
| AL10 | VSS | Power/Other | |
| AL11 | VCC | Power/Other | |
| AL12 | VCC | Power/Other | |
| AL13 | VSS | Power/Other | |
| AL14 | VCC | Power/Other | |
| AL15 | VCC | Power/Other | |

## Table 24. Numerical Land Assignment

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| AL16 | VSS | Power/Other | |
| AL17 | VSS | Power/Other | |
| AL18 | VCC | Power/Other | |
| AL19 | VCC | Power/Other | |
| AL2 | PROCHOT# | Asynch GTL+ | Input/Output |
| AL20 | VSS | Power/Other | |
| AL21 | VCC | Power/Other | |
| AL22 | VCC | Power/Other | |
| AL23 | VSS | Power/Other | |
| AL24 | VSS | Power/Other | |
| AL25 | VCC | Power/Other | |
| AL26 | VCC | Power/Other | |
| AL27 | VSS | Power/Other | |
| AL28 | VSS | Power/Other | |
| AL29 | VCC | Power/Other | |
| AL3 | VSS | Power/Other | |
| AL30 | VCC | Power/Other | |
| AL4 | VID5 | Power/Other | Output |
| AL5 | VID1 | Power/Other | Output |
| AL6 | VID3 | Power/Other | Output |
| AL7 | VSS | Power/Other | |
| AL8 | VCC | Power/Other | |
| AL9 | VCC | Power/Other | |
| AM1 | VSS | Power/Other | |
| AM10 | VSS | Power/Other | |
| AM11 | VCC | Power/Other | |
| AM12 | VCC | Power/Other | |
| AM13 | VSS | Power/Other | |
| AM14 | VCC | Power/Other | |
| AM15 | VCC | Power/Other | |
| AM16 | VSS | Power/Other | |
| AM17 | VSS | Power/Other | |
| AM18 | VCC | Power/Other | |
| AM19 | VCC | Power/Other | |
| AM2 | VID0 | Power/Other | Output |
| AM20 | VSS | Power/Other | |
| AM21 | VCC | Power/Other | |
| AM22 | VCC | Power/Other | |
| AM23 | VSS | Power/Other | |
| AM24 | VSS | Power/Other | |

**Table 24. Numerical Land Assignment**

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| AM25 | VCC | Power/Other | |
| AM26 | VCC | Power/Other | |
| AM27 | VSS | Power/Other | |
| AM28 | VSS | Power/Other | |
| AM29 | VCC | Power/Other | |
| AM3 | VID2 | Power/Other | Output |
| AM30 | VCC | Power/Other | |
| AM4 | VSS | Power/Other | |
| AM5 | FC11 | Power/Other | Output |
| AM6 | VTTPWRGD | Power/Other | Input |
| AM7 | FC12 | Power/Other | Output |
| AM8 | VCC | Power/Other | |
| AM9 | VCC | Power/Other | |
| AN1 | VSS | Power/Other | |
| AN10 | VSS | Power/Other | |
| AN11 | VCC | Power/Other | |
| AN12 | VCC | Power/Other | |
| AN13 | VSS | Power/Other | |
| AN14 | VCC | Power/Other | |
| AN15 | VCC | Power/Other | |
| AN16 | VSS | Power/Other | |
| AN17 | VSS | Power/Other | |
| AN18 | VCC | Power/Other | |
| AN19 | VCC | Power/Other | |
| AN2 | VSS | Power/Other | |
| AN20 | VSS | Power/Other | |
| AN21 | VCC | Power/Other | |
| AN22 | VCC | Power/Other | |
| AN23 | VSS | Power/Other | |
| AN24 | VSS | Power/Other | |
| AN25 | VCC | Power/Other | |
| AN26 | VCC | Power/Other | |
| AN27 | VSS | Power/Other | |
| AN28 | VSS | Power/Other | |
| AN29 | VCC | Power/Other | |
| AN3 | VCC_SENSE | Power/Other | Output |
| AN30 | VCC | Power/Other | |
| AN4 | VSS_SENSE | Power/Other | Output |
| AN5 | VCC_MB_ REGULATION | Power/Other | Output |

**Table 24. Numerical Land Assignment**

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| AN6 | VSS_MB_ REGULATION | Power/Other | Output |
| AN7 | FC16 | Power/Other | Output |
| AN8 | VCC | Power/Other | |
| AN9 | VCC | Power/Other | |
| B1 | VSS | Power/Other | |
| B10 | D10# | Source Synch | Input/Output |
| B11 | VSS | Power/Other | |
| B12 | D13# | Source Synch | Input/Output |
| B13 | FC19 | Power/Other | Output |
| B14 | VSS | Power/Other | |
| B15 | D53# | Source Synch | Input/Output |
| B16 | D55# | Source Synch | Input/Output |
| B17 | VSS | Power/Other | |
| B18 | D57# | Source Synch | Input/Output |
| B19 | D60# | Source Synch | Input/Output |
| B2 | DBSY# | Common Clock | Input/Output |
| B20 | VSS | Power/Other | |
| B21 | D59# | Source Synch | Input/Output |
| B22 | D63# | Source Synch | Input/Output |
| B23 | VSSA | Power/Other | |
| B24 | VSS | Power/Other | |
| B25 | VTT | Power/Other | |
| B26 | VTT | Power/Other | |
| B27 | VTT | Power/Other | |
| B28 | VTT | Power/Other | |
| B29 | VTT | Power/Other | |
| B3 | RS0# | Common Clock | Input |
| B30 | VTT | Power/Other | |
| B4 | D00# | Source Synch | Input/Output |
| B5 | VSS | Power/Other | |
| B6 | D05# | Source Synch | Input/Output |
| B7 | D06# | Source Synch | Input/Output |
| B8 | VSS | Power/Other | |
| B9 | DSTBP0# | Source Synch | Input/Output |
| C1 | DRDY# | Common Clock | Input/Output |
| C10 | VSS | Power/Other | |
| C11 | D11# | Source Synch | Input/Output |
| C12 | D14# | Source Synch | Input/Output |
| C13 | VSS | Power/Other | |
| C14 | D52# | Source Synch | Input/Output |

**Table 24. Numerical Land Assignment**

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| C15 | D51# | Source Synch | Input/Output |
| C16 | VSS | Power/Other | |
| C17 | DSTBP3# | Source Synch | Input/Output |
| C18 | D54# | Source Synch | Input/Output |
| C19 | VSS | Power/Other | |
| C2 | BNR# | Common Clock | Input/Output |
| C20 | DBI3# | Source Synch | Input/Output |
| C21 | D58# | Source Synch | Input/Output |
| C22 | VSS | Power/Other | |
| C23 | VCCIOPLL | Power/Other | |
| C24 | VSS | Power/Other | |
| C25 | VTT | Power/Other | |
| C26 | VTT | Power/Other | |
| C27 | VTT | Power/Other | |
| C28 | VTT | Power/Other | |
| C29 | VTT | Power/Other | |
| C3 | LOCK# | Common Clock | Input/Output |
| C30 | VTT | Power/Other | |
| C4 | VSS | Power/Other | |
| C5 | D01# | Source Synch | Input/Output |
| C6 | D03# | Source Synch | Input/Output |
| C7 | VSS | Power/Other | |
| C8 | DSTBN0# | Source Synch | Input/Output |
| C9 | RESERVED | | |
| D1 | RESERVED | | |
| D10 | D22# | Source Synch | Input/Output |
| D11 | D15# | Source Synch | Input/Output |
| D12 | VSS | Power/Other | |
| D13 | D25# | Source Synch | Input/Output |
| D14 | RESERVED | | |
| D15 | VSS | Power/Other | |
| D16 | RESERVED | | |
| D17 | D49# | Source Synch | Input/Output |
| D18 | VSS | Power/Other | |
| D19 | DBI2# | Source Synch | Input/Output |
| D2 | ADS# | Common Clock | Input/Output |
| D20 | D48# | Source Synch | Input/Output |
| D21 | VSS | Power/Other | |
| D22 | D46# | Source Synch | Input/Output |
| D23 | FC9 | Power/Other | Output |

**Table 24. Numerical Land Assignment**

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| D24 | VSS | Power/Other | |
| D25 | VTT | Power/Other | |
| D26 | VTT | Power/Other | |
| D27 | VTT | Power/Other | |
| D28 | VTT | Power/Other | |
| D29 | VTT | Power/Other | |
| D3 | VSS | Power/Other | |
| D30 | VTT | Power/Other | |
| D4 | HIT# | Common Clock | Input/Output |
| D5 | VSS | Power/Other | |
| D6 | VSS | Power/Other | |
| D7 | D20# | Source Synch | Input/Output |
| D8 | D12# | Source Synch | Input/Output |
| D9 | VSS | Power/Other | |
| E10 | D21# | Source Synch | Input/Output |
| E11 | VSS | Power/Other | |
| E12 | DSTBP1# | Source Synch | Input/Output |
| E13 | D26# | Source Synch | Input/Output |
| E14 | VSS | Power/Other | |
| E15 | D33# | Source Synch | Input/Output |
| E16 | D34# | Source Synch | Input/Output |
| E17 | VSS | Power/Other | |
| E18 | D39# | Source Synch | Input/Output |
| E19 | D40# | Source Synch | Input/Output |
| E2 | VSS | Power/Other | |
| E20 | VSS | Power/Other | |
| E21 | D42# | Source Synch | Input/Output |
| E22 | D45# | Source Synch | Input/Output |
| E23 | RESERVED | | |
| E24 | FC10 | Power/Other | Output |
| E25 | VSS | Power/Other | |
| E26 | VSS | Power/Other | |
| E27 | VSS | Power/Other | |
| E28 | VSS | Power/Other | |
| E29 | VSS | Power/Other | |
| E3 | TRDY# | Common Clock | Input |
| E4 | HITM# | Common Clock | Input/Output |
| E5 | FC20 | Power/Other | Output |
| E6 | RESERVED | | |
| E7 | RESERVED | | |

## Table 24. Numerical Land Assignment

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| E8 | VSS | Power/Other | |
| E9 | D19# | Source Synch | Input/Output |
| F10 | VSS | Power/Other | |
| F11 | D23# | Source Synch | Input/Output |
| F12 | D24# | Source Synch | Input/Output |
| F13 | VSS | Power/Other | |
| F14 | D28# | Source Synch | Input/Output |
| F15 | D30# | Source Synch | Input/Output |
| F16 | VSS | Power/Other | |
| F17 | D37# | Source Synch | Input/Output |
| F18 | D38# | Source Synch | Input/Output |
| F19 | VSS | Power/Other | |
| F2 | FC5 | Common Clock | Input |
| F20 | D41# | Source Synch | Input/Output |
| F21 | D43# | Source Synch | Input/Output |
| F22 | VSS | Power/Other | |
| F23 | RESERVED | | |
| F24 | TESTHI7 | Power/Other | Input |
| F25 | TESTHI2 | Power/Other | Input |
| F26 | TESTHI0 | Power/Other | Input |
| F27 | VTT_SEL | Power/Other | Output |
| F28 | BCLK0 | Clock | Input |
| F29 | RESERVED | | |
| F3 | BR0# | Common Clock | Input/Output |
| F4 | VSS | Power/Other | |
| F5 | RS1# | Common Clock | Input |
| F6 | IMPSEL | Power/Other | Input |
| F7 | VSS | Power/Other | |
| F8 | D17# | Source Synch | Input/Output |
| F9 | D18# | Source Synch | Input/Output |
| G1 | VSS | Power/Other | |
| G10 | RESERVED | | |
| G11 | DBI1# | Source Synch | Input/Output |
| G12 | DSTBN1# | Source Synch | Input/Output |
| G13 | D27# | Source Synch | Input/Output |
| G14 | D29# | Source Synch | Input/Output |
| G15 | D31# | Source Synch | Input/Output |
| G16 | D32# | Source Synch | Input/Output |
| G17 | D36# | Source Synch | Input/Output |
| G18 | D35# | Source Synch | Input/Output |

## Table 24. Numerical Land Assignment

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| G19 | DSTBP2# | Source Synch | Input/Output |
| G2 | FC1 | Power/Other | Input |
| G20 | DSTBN2# | Source Synch | Input/Output |
| G21 | D44# | Source Synch | Input/Output |
| G22 | D47# | Source Synch | Input/Output |
| G23 | RESET# | Common Clock | Input |
| G24 | TESTHI6 | Power/Other | Input |
| G25 | TESTHI3 | Power/Other | Input |
| G26 | TESTHI5 | Power/Other | Input |
| G27 | TESTHI4 | Power/Other | Input |
| G28 | BCLK1 | Clock | Input |
| G29 | BSEL0 | Power/Other | Output |
| G3 | TESTHI8 | Power/Other | Input |
| G30 | BSEL2 | Power/Other | Output |
| G4 | TESTHI9 | Power/Other | Input |
| G5 | FC7 | Source Synch | Output |
| G6 | RESERVED | | |
| G7 | DEFER# | Common Clock | Input |
| G8 | BPRI# | Common Clock | Input |
| G9 | D16# | Source Synch | Input/Output |
| H1 | GTLREF0 | Power/Other | Input |
| H10 | VSS | Power/Other | |
| H11 | VSS | Power/Other | |
| H12 | VSS | Power/Other | |
| H13 | VSS | Power/Other | |
| H14 | VSS | Power/Other | |
| H15 | DP1# | Common Clock | Input/Output |
| H16 | DP2# | Common Clock | Input/Output |
| H17 | VSS | Power/Other | |
| H18 | VSS | Power/Other | |
| H19 | VSS | Power/Other | |
| H2 | GTLREF1 | Power/Other | Input |
| H20 | VSS | Power/Other | |
| H21 | VSS | Power/Other | |
| H22 | VSS | Power/Other | |
| H23 | VSS | Power/Other | |
| H24 | VSS | Power/Other | |
| H25 | VSS | Power/Other | |
| H26 | VSS | Power/Other | |
| H27 | VSS | Power/Other | |

**Table 24. Numerical Land Assignment**

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| H28 | VSS | Power/Other | |
| H29 | FC15 | Power/Other | Output |
| H3 | VSS | Power/Other | |
| H30 | BSEL1 | Power/Other | Output |
| H4 | RSP# | Common Clock | Input |
| H5 | TESTHI10 | Power/Other | Input |
| H6 | VSS | Power/Other | |
| H7 | VSS | Power/Other | |
| H8 | VSS | Power/Other | |
| H9 | VSS | Power/Other | |
| J1 | VTT_OUT_LEFT | Power/Other | Output |
| J10 | VCC | Power/Other | |
| J11 | VCC | Power/Other | |
| J12 | VCC | Power/Other | |
| J13 | VCC | Power/Other | |
| J14 | VCC | Power/Other | |
| J15 | VCC | Power/Other | |
| J16 | DP0# | Common Clock | Input/Output |
| J17 | DP3# | Common Clock | Input/Output |
| J18 | VCC | Power/Other | |
| J19 | VCC | Power/Other | |
| J2 | COMP4 | Power/Other | Input |
| J20 | VCC | Power/Other | |
| J21 | VCC | Power/Other | |
| J22 | VCC | Power/Other | |
| J23 | VCC | Power/Other | |
| J24 | VCC | Power/Other | |
| J25 | VCC | Power/Other | |
| J26 | VCC | Power/Other | |
| J27 | VCC | Power/Other | |
| J28 | VCC | Power/Other | |
| J29 | VCC | Power/Other | |
| J3 | FC22 | Power/Other | Output |
| J30 | VCC | Power/Other | |
| J4 | VSS | Power/Other | |
| J5 | REQ1# | Source Synch | Input/Output |
| J6 | REQ4# | Source Synch | Input/Output |
| J7 | VSS | Power/Other | |
| J8 | VCC | Power/Other | |
| J9 | VCC | Power/Other | |

**Table 24. Numerical Land Assignment**

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| K1 | LINT0 | Asynch GTL+ | Input |
| K2 | VSS | Power/Other | |
| K23 | VCC | Power/Other | |
| K24 | VCC | Power/Other | |
| K25 | VCC | Power/Other | |
| K26 | VCC | Power/Other | |
| K27 | VCC | Power/Other | |
| K28 | VCC | Power/Other | |
| K29 | VCC | Power/Other | |
| K3 | A20M# | Asynch GTL+ | Input |
| K30 | VCC | Power/Other | |
| K4 | REQ0# | Source Synch | Input/Output |
| K5 | VSS | Power/Other | |
| K6 | REQ3# | Source Synch | Input/Output |
| K7 | VSS | Power/Other | |
| K8 | VCC | Power/Other | |
| L1 | LINT1 | Asynch GTL+ | Input |
| L2 | TESTHI13 | Asynch GTL+ | Input |
| L23 | VSS | Power/Other | |
| L24 | VSS | Power/Other | |
| L25 | VSS | Power/Other | |
| L26 | VSS | Power/Other | |
| L27 | VSS | Power/Other | |
| L28 | VSS | Power/Other | |
| L29 | VSS | Power/Other | |
| L3 | VSS | Power/Other | |
| L30 | VSS | Power/Other | |
| L4 | A06# | Source Synch | Input/Output |
| L5 | A03# | Source Synch | Input/Output |
| L6 | VSS | Power/Other | |
| L7 | VSS | Power/Other | |
| L8 | VCC | Power/Other | |
| M1 | VSS | Power/Other | |
| M2 | THERMTRIP# | Asynch GTL+ | Output |
| M23 | VCC | Power/Other | |
| M24 | VCC | Power/Other | |
| M25 | VCC | Power/Other | |
| M26 | VCC | Power/Other | |
| M27 | VCC | Power/Other | |
| M28 | VCC | Power/Other | |

**Table 24. Numerical Land Assignment**

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| M29 | VCC | Power/Other | |
| M3 | STPCLK# | Asynch GTL+ | Input |
| M30 | VCC | Power/Other | |
| M4 | A07# | Source Synch | Input/Output |
| M5 | A05# | Source Synch | Input/Output |
| M6 | REQ2# | Source Synch | Input/Output |
| M7 | VSS | Power/Other | |
| M8 | VCC | Power/Other | |
| N1 | PWRGOOD | Power/Other | Input |
| N2 | IGNNE# | Asynch GTL+ | Input |
| N23 | VCC | Power/Other | |
| N24 | VCC | Power/Other | |
| N25 | VCC | Power/Other | |
| N26 | VCC | Power/Other | |
| N27 | VCC | Power/Other | |
| N28 | VCC | Power/Other | |
| N29 | VCC | Power/Other | |
| N3 | VSS | Power/Other | |
| N30 | VCC | Power/Other | |
| N4 | RESERVED | | |
| N5 | RESERVED | | |
| N6 | VSS | Power/Other | |
| N7 | VSS | Power/Other | |
| N8 | VCC | Power/Other | |
| P1 | TESTHI11 | Power/Other | Input |
| P2 | SMI# | Asynch GTL+ | Input |
| P23 | VSS | Power/Other | |
| P24 | VSS | Power/Other | |
| P25 | VSS | Power/Other | |
| P26 | VSS | Power/Other | |
| P27 | VSS | Power/Other | |
| P28 | VSS | Power/Other | |
| P29 | VSS | Power/Other | |
| P3 | INIT# | Asynch GTL+ | Input |
| P30 | VSS | Power/Other | |
| P4 | VSS | Power/Other | |
| P5 | RESERVED | | |
| P6 | A04# | Source Synch | Input/Output |
| P7 | VSS | Power/Other | |
| P8 | VCC | Power/Other | |

**Table 24. Numerical Land Assignment**

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| R1 | FC2 | Power/Other | Input |
| R2 | VSS | Power/Other | |
| R23 | VSS | Power/Other | |
| R24 | VSS | Power/Other | |
| R25 | VSS | Power/Other | |
| R26 | VSS | Power/Other | |
| R27 | VSS | Power/Other | |
| R28 | VSS | Power/Other | |
| R29 | VSS | Power/Other | |
| R3 | FERR#/PBE# | Asynch GTL+ | Output |
| R30 | VSS | Power/Other | |
| R4 | A08# | Source Synch | Input/Output |
| R5 | VSS | Power/Other | |
| R6 | ADSTB0# | Source Synch | Input/Output |
| R7 | VSS | Power/Other | |
| R8 | VCC | Power/Other | |
| T1 | COMP1 | Power/Other | Input |
| T2 | COMP5 | Power/Other | Input |
| T23 | VCC | Power/Other | |
| T24 | VCC | Power/Other | |
| T25 | VCC | Power/Other | |
| T26 | VCC | Power/Other | |
| T27 | VCC | Power/Other | |
| T28 | VCC | Power/Other | |
| T29 | VCC | Power/Other | |
| T3 | VSS | Power/Other | |
| T30 | VCC | Power/Other | |
| T4 | A11# | Source Synch | Input/Output |
| T5 | A09# | Source Synch | Input/Output |
| T6 | VSS | Power/Other | |
| T7 | VSS | Power/Other | |
| T8 | VCC | Power/Other | |
| U1 | VSS | Power/Other | |
| U2 | AP0# | Common Clock | Input/Output |
| U23 | VCC | Power/Other | |
| U24 | VCC | Power/Other | |
| U25 | VCC | Power/Other | |
| U26 | VCC | Power/Other | |
| U27 | VCC | Power/Other | |
| U28 | VCC | Power/Other | |

## Table 24. Numerical Land Assignment

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| U29 | VCC | Power/Other | |
| U3 | AP1# | Common Clock | Input/Output |
| U30 | VCC | Power/Other | |
| U4 | A13# | Source Synch | Input/Output |
| U5 | A12# | Source Synch | Input/Output |
| U6 | A10# | Source Synch | Input/Output |
| U7 | VSS | Power/Other | |
| U8 | VCC | Power/Other | |
| V1 | MSID1 | Power/Other | Output |
| V2 | LL_ID0 | Power/Other | Output |
| V23 | VSS | Power/Other | |
| V24 | VSS | Power/Other | |
| V25 | VSS | Power/Other | |
| V26 | VSS | Power/Other | |
| V27 | VSS | Power/Other | |
| V28 | VSS | Power/Other | |
| V29 | VSS | Power/Other | |
| V3 | VSS | Power/Other | |
| V30 | VSS | Power/Other | |
| V4 | A15# | Source Synch | Input/Output |
| V5 | A14# | Source Synch | Input/Output |
| V6 | VSS | Power/Other | |
| V7 | VSS | Power/Other | |
| V8 | VCC | Power/Other | |
| W1 | MSID0 | Power/Other | Output |
| W2 | TESTHI12 | Power/Other | Input |
| W23 | VCC | Power/Other | |
| W24 | VCC | Power/Other | |
| W25 | VCC | Power/Other | |
| W26 | VCC | Power/Other | |
| W27 | VCC | Power/Other | |
| W28 | VCC | Power/Other | |
| W29 | VCC | Power/Other | |
| W3 | TESTHI1 | Power/Other | Input |
| W30 | VCC | Power/Other | |
| W4 | VSS | Power/Other | |
| W5 | A16# | Source Synch | Input/Output |

## Table 24. Numerical Land Assignment

| Land # | Land Name | Signal Buffer Type | Direction |
|---|---|---|---|
| W6 | A18# | Source Synch | Input/Output |
| W7 | VSS | Power/Other | |
| W8 | VCC | Power/Other | |
| Y1 | BOOTSELECT | Power/Other | Input |
| Y2 | VSS | Power/Other | |
| Y23 | VCC | Power/Other | |
| Y24 | VCC | Power/Other | |
| Y25 | VCC | Power/Other | |
| Y26 | VCC | Power/Other | |
| Y27 | VCC | Power/Other | |
| Y28 | VCC | Power/Other | |
| Y29 | VCC | Power/Other | |
| Y3 | FC17 | Power/Other | |
| Y30 | VCC | Power/Other | |
| Y4 | A20# | Source Synch | Input/Output |
| Y5 | VSS | Power/Other | |
| Y6 | A19# | Source Synch | Input/Output |
| Y7 | VSS | Power/Other | |
| Y8 | VCC | Power/Other | |

## 4.2 Alphabetical Signals Reference

**Table 25. Signal Description (Sheet 1 of 9)**

| Name | Type | Description |
|---|---|---|
| A[35:3]# | Input/ Output | A[35:3]# (Address) define a $2^{36}$-byte physical memory address space. In sub-phase 1 of the address phase, these signals transmit the address of a transaction. In sub-phase 2, these signals transmit transaction type information. These signals must connect the appropriate pins/lands of all agents on the processor FSB. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#.<br>On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# signals to determine power-on configuration. See Section 6.1 for more details. |
| A20M# | Input | If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-MB boundary. Assertion of A20M# is only supported in real mode.<br>A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/ Output Write bus transaction. |
| ADS# | Input/ Output | ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# signals. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. |
| ADSTB[1:0]# | Input/ Output | Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below.<br>**Signals** — **Associated Strobe**<br>REQ[4:0]#, A[16:3]# — ADSTB0#<br>A[35:17]# — ADSTB1# |
| AP[1:0]# | Input/ Output | AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#, A[35:3]#, and the transaction type on the REQ[4:0]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins/lands of all processor FSB agents. The following table defines the coverage model of these signals.<br>**Request Signals** — **Subphase 1** — **Subphase 2**<br>A[35:24]# — AP0# — AP1#<br>A[23:3]# — AP1# — AP0#<br>REQ[4:0]# — AP1# — AP0# |

## Table 25. Signal Description (Sheet 1 of 9)

| Name | Type | Description |
|---|---|---|
| BCLK[1:0] | Input | The differential pair BCLK (Bus Clock) determines the FSB frequency. All processor FSB agents must receive these signals to drive their outputs and latch their inputs.<br>All external timing parameters are specified with respect to the rising edge of BCLK0 crossing $V_{CROSS}$. |
| BINIT# | Input/ Output | BINIT# (Bus Initialization) may be observed and driven by all processor FSB agents and if used, must connect the appropriate pins/lands of all such agents. If the BINIT# driver is enabled during power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation.<br>If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their IOQ and transaction tracking state machines upon observation of BINIT# activation. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the FSB and attempt completion of their bus queue and IOQ entries.<br>If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system. |
| BNR# | Input/ Output | BNR# (Block Next Request) is used to assert a bus stall by any bus agent unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. |
| BOOTSELECT | Input | This input is required to determine whether the processor is installed in a platform that supports the Pentium 4 processor. The processor will not operate if this signal is low. This input has a weak internal pull-up to $V_{CC}$. |
| BPM[5:0]# | Input/ Output | BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins/lands of all processor FSB agents.<br>BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness.<br>BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processor.<br>These signals do not have on-die termination. Refer to Section 2.5.2 for termination requirements. |
| BPRI# | Input | BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor FSB. It must connect the appropriate pins/lands of all processor FSB agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by de-asserting BPRI#. |

## Table 25. Signal Description (Sheet 1 of 9)

| Name | Type | Description |
|---|---|---|
| BR0# | Input/ Output | BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. During power-on configuration this signal is sampled to determine the agent ID = 0.<br>This signal does not have on-die termination and must be terminated. |
| BSEL[2:0] | Output | The BCLK[1:0] frequency select signals BSEL[2:0] are used to select the processor input clock frequency. Table 18 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. For more information about these signals, including termination recommendations, refer to Chapter 2. |
| COMP[5:4,1:0] | Analog | COMP[1:0] must be terminated to $V_{SS}$ on the system board using precision resistors. COMP[5:4] must be terminated to $V_{TT}$ on the system board using precision resistors. |
| D[63:0]# | Input/ Output | D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor FSB agents, and must connect the appropriate pins/lands on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.<br>D[63:0]# are quad-pumped signals and will, thus, be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DBI#.<br>**Quad-Pumped Signal Groups**<br>**Data Group** / **DSTBN# / DSTBP#** / **DBI#**<br>D[15:0]# / 0 / 0<br>D[31:16]# / 1 / 1<br>D[47:32]# / 2 / 2<br>D[63:48]# / 3 / 3<br>Furthermore, the DBI# signals determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high. |

## Table 25. Signal Description (Sheet 1 of 9)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DBI[3:0]#</td><td>Input/ Output</td><td>DBI[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals.The DBI[3:0]# signals are activated when the data on the data bus is inverted. If more than half the data bits, within a 16-bit group, would have been asserted electrically low, the bus agent may invert the data bus signals for that particular sub-phase for that 16-bit group.<br><br>DBI[3:0] Assignment To Data Bus<br><br>Bus Signal — Data Bus Signals<br>DBI3# — D[63:48]#<br>DBI2# — D[47:32]#<br>DBI1# — D[31:16]#<br>DBI0# — D[15:0]#</td></tr>
<tr><td>DBR#</td><td>Output</td><td>DBR# (Debug Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.</td></tr>
<tr><td>DBSY#</td><td>Input/ Output</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor FSB to indicate that the data bus is in use. The data bus is released after DBSY# is de-asserted. This signal must connect the appropriate pins/lands on all processor FSB agents.</td></tr>
<tr><td>DEFER#</td><td>Input</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be ensured in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or input/ output agent. This signal must connect the appropriate pins/lands of all processor FSB agents.</td></tr>
<tr><td>DP[3:0]#</td><td>Input/ Output</td><td>DP[3:0]# (Data parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins/lands of all processor FSB agents.</td></tr>
<tr><td>DRDY#</td><td>Input/ Output</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be de-asserted to insert idle clocks. This signal must connect the appropriate pins/lands of all processor FSB agents.</td></tr>
<tr><td>DSTBN[3:0]#</td><td>Input/ Output</td><td>DSTBN[3:0]# are the data strobes used to latch in D[63:0]#.<br><br>Signals — Associated Strobe<br>D[15:0]#, DBI0# — DSTBN0#<br>D[31:16]#, DBI1# — DSTBN1#<br>D[47:32]#, DBI2# — DSTBN2#<br>D[63:48]#, DBI3# — DSTBN3#</td></tr>
</table>

## Table 25. Signal Description (Sheet 1 of 9)

| Name | Type | Description |
|---|---|---|
| DSTBP[3:0]# | Input/ Output | DSTBP[3:0]# are the data strobes used to latch in D[63:0]#.<br>**Signals** — **Associated Strobe**<br>D[15:0]#, DBI0# — DSTBP0#<br>D[31:16]#, DBI1# — DSTBP1#<br>D[47:32]#, DBI2# — DSTBP2#<br>D[63:48]#, DBI3# — DSTBP3# |
| FCx | Other | FC signals are signals that are available for compatibility with other processors. |
| FERR#/PBE# | Output | FERR#/PBE# (floating point error/pending break event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR#/PBE# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. For additional information on the pending break event functionality, including the identification of support of the feature and enable/disable information, refer to volume 3 of the *Intel® 64 and IA-32 Architecture Software Developer's Manual* and the *Intel Processor Identification and the CPUID Instruction* application note. |
| GTLREF[1:0] | Input | GTLREF[1:0] determine the signal reference level for GTL+ input signals. GTLREF is used by the GTL+ receivers to determine if a signal is a logical 0 or logical 1. |
| HIT#<br><br>HITM# | Input/ Output<br><br>Input/ Output | HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together. |
| IERR# | Output | IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#.<br>This signal does not have on-die termination. Refer to Section 2.5.2 for termination requirements. |

## Table 25. Signal Description (Sheet 1 of 9)

| Name | Type | Description |
|---|---|---|
| IGNNE# | Input | IGNNE# (Ignore Numeric Error) is asserted to the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is de-asserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set.<br>IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. |
| IMPSEL | Input | IMPSEL input will determine whether the processor uses a 50 Ω or 60 Ω buffer. This pin must be tied to GND on 50Ω platforms and left as NC on 60Ω platforms. |
| INIT# | Input | INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins/lands of all processor FSB agents.<br>If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST). |
| ITP_CLK[1:0] | Input | ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals. |
| LINT[1:0] | Input | LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins/lands of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous.<br>Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these signals as LINT[1:0] is the default configuration. |
| LL_ID[1:0] | Output | The LL_ID[1:0] signals are used to select the correct loadline slope for the processor. LL_ID[1:0] = 00 for the Pentium 4 processor. |
| LOCK# | Input/ Output | LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins/lands of all processor FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction.<br>When the priority agent asserts BPRI# to arbitrate for ownership of the processor FSB, it will wait until it observes LOCK# de-asserted. This enables symmetric agents to retain ownership of the processor FSB throughout the bus locked operation and ensure the atomicity of lock. |

## Table 25. Signal Description (Sheet 1 of 9)

| Name | Type | Description |
|---|---|---|
| MCERR# | Input/ Output | MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor FSB agents.<br>MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options:<br>• Enabled or disabled.<br>• Asserted, if configured, for internal errors along with IERR#.<br>• Asserted, if configured, by the request initiator of a bus transaction after it observes an error.<br>• Asserted by any bus agent when it observes an error in a bus transaction.<br>For more details regarding machine check architecture, refer to the *Intel® 64 and IA-32 Architecture Software Developer's Manual, Volume 3: System Programming Guide*. |
| MSID[1:0] | Input | MSID[1:0] (input) MSID0 is used to indicate to the processor whether the platform supports 775_VR_CONFIG_05B processors. A 775_VR_CONFIG_05B processor will only boot if it's MSID0 pin is electrically low. A 775_VR_CONFIG_05A processor will ignore this input.<br>MSID1 must be electrically low for the processor to boot. |
| PROCHOT# | Input/ Output | As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system de-asserts PROCHOT#. See Section 5.2.4 for more details. |
| PWRGOOD | Input | PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD.<br>The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. |
| REQ[4:0]# | Input/ Output | REQ[4:0]# (Request Command) must connect the appropriate pins/lands of all processor FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#. Refer to the AP[1:0]# signal description for a details on parity checking of these signals. |

### Table 25. Signal Description (Sheet 1 of 9)

| Name | Type | Description |
|---|---|---|
| RESET# | Input | Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after $V_{CC}$ and BCLK have reached their proper specifications. On observing active RESET#, all FSB agents will de-assert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted.<br>A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 6.1.<br>This signal does not have on-die termination and must be terminated on the system board. |
| RS[2:0]# | Input | RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins/lands of all processor FSB agents. |
| RSP# | Input | RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins/lands of all processor FSB agents.<br>A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent ensuring correct parity. |
| SKTOCC# | Output | SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this signal to determine if the processor is present. |
| SMI# | Input | SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.<br>If SMI# is asserted during the de-assertion of RESET#, the processor will tri-state its outputs. |
| STPCLK# | Input | STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is de-asserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input. |
| TCK | Input | TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port). |
| TDI | Input | TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support. |
| TDO | Output | TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support. |

### Table 25. Signal Description (Sheet 1 of 9)

| Name | Type | Description |
|---|---|---|
| TESTHI[13:0] | Input | TESTHI[13:0] must be connected to the processor's appropriate power source (refer to VTT_OUT_LEFT and VTT_OUT_RIGHT signal description) through a resistor for proper processor operation. See Section 2.4 for more details. |
| THERMDA | Other | Thermal Diode Anode. See Section 5.2.7. |
| THERMDC | Other | Thermal Diode Cathode. See Section 5.2.7. |
| THERMTRIP# | Output | In the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature approximately 20 °C above the maximum $T_C$. Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level beyond where permanent silicon damage may occur. Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus, halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage ($V_{CC}$) must be removed following the assertion of THERMTRIP#. Driving of the THERMTRIP# signal is enabled within 10 µs of the assertion of PWRGOOD (provided VTTPWRGD, $V_{TT}$, and $V_{CC}$ are asserted) and is disabled on de-assertion of PWRGOOD (if VTTPWRGD, $V_{TT}$, or $V_{CC}$ are not valid, THERMTRIP# may also be disabled). Once activated, THERMTRIP# remains latched until PWRGOOD, VTTPWRGD, $V_{TT}$ or $V_{CC}$ is de-asserted. While the de-assertion of the PWRGOOD, VTTPWRGD, VTT or VCC signal will de-assert THERMTRIP#, if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted within 10 µs of the assertion of PWRGOOD (provided VTTPWRGD, $V_{TT}$, and $V_{CC}$ are asserted). |
| TMS | Input | TMS (Test Mode Select) is a JTAG specification support signal used by debug tools. |
| TRDY# | Input | TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins/lands of all FSB agents. |
| TRST# | Input | TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. |
| VCC | Input | VCC are the power lands for the processor. The voltage supplied to these lands is determined by the VID[5:0] pins. |
| VCCA | Input | VCCA provides isolated power for the internal processor core PLLs. |
| VCCIOPLL | Input | VCCIOPLL provides isolated power for internal processor FSB PLLs. |
| VCC_SENSE | Output | VCC_SENSE is an isolated low impedance connection to processor core power ($V_{CC}$). It can be used to sense or measure voltage near the silicon with little noise. |
| VCC_MB_ REGULATION | Output | This land is provided as a voltage regulator feedback sense point for $V_{CC}$. It is connected internally in the processor package to the sense point land U27 as described in the *Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop Socket 775*. |

### Table 25. Signal Description (Sheet 1 of 9)

| Name | Type | Description |
|---|---|---|
| VID[5:0] | Output | VID[5:0] (Voltage ID) signals are used to support automatic selection of power supply voltages ($V_{CC}$). Refer to the *Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop Socket 775* for more information. The voltage supply for these signals must be valid before the VR can supply $V_{CC}$ to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID signals becomes valid. The VID signals are needed to support the processor voltage specification variations. See Table 2 for definitions of these signals. The VR must supply the voltage that is requested by the signals, or disable itself. |
| VSS | Input | VSS are the ground pins for the processor and should be connected to the system ground plane. |
| VSSA | Input | VSSA is the isolated ground for internal PLLs. |
| VSS_SENSE | Output | VSS_SENSE is an isolated low impedance connection to processor core $V_{SS}$. It can be used to sense or measure ground near the silicon with little noise. |
| VSS_MB_<br>REGULATION | Output | This land is provided as a voltage regulator feedback sense point for $V_{SS}$. It is connected internally in the processor package to the sense point land V27 as described in the *Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop Socket 775*. |
| VTT | | Miscellaneous voltage supply. |
| VTT_OUT_LEFT<br><br>VTT_OUT_RIGHT | Output | The VTT_OUT_LEFT and VTT_OUT_RIGHT signals are included to provide a voltage supply for some signals that require termination to $V_{TT}$ on the motherboard. |
| VTT_SEL | Output | The VTT_SEL signal is used to select the correct $V_{TT}$ voltage level for the processor. This land is connected internally in the package to $V_{TT}$. |
| VTTPWRGD | Input | The processor requires this input to determine that the $V_{TT}$ voltages are stable and within specification. |

§ §

# 5 Thermal Specifications and Design Considerations

## 5.1 Processor Thermal Specifications

The Pentium 4 processor requires a thermal solution to maintain temperatures within the operating limits as set forth in Section 5.1.1. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components within the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete thermal solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor Integrated Heat Spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.

For more information on designing a component level thermal solution, refer to the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2).

***Note:*** The boxed processor will ship with a component thermal solution. Refer to Chapter 7 for details on the boxed processor.

### 5.1.1 Thermal Specifications

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum case temperature ($T_C$) specifications when operating at or below the Thermal Design Power (TDP) value listed per frequency in Table 26. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, refer to the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2).

The Pentium 4 processor uses a methodology for managing processor temperatures that is intended to support acoustic noise reduction through fan speed control. Selection of the appropriate fan speed will be based on the temperature reported by the processor's Thermal Diode. If the diode temperature is greater than or equal to $T_{CONTROL}$, then the processor case temperature must remain at or below the temperature as specified by the thermal profile. If the diode temperature is less than $T_{CONTROL}$, then the case temperature is permitted to exceed the thermal profile; but the diode temperature must remain at or below $T_{CONTROL}$. Systems that implement fan speed control must be designed to take these conditions into account. Systems that do not alter the fan speed only need to ensure the case temperature meets the thermal profile specifications.

To determine a processor's case temperature specification based on the thermal profile, it is necessary to accurately measure processor power dissipation. Intel has developed a methodology for accurate power measurement that correlates to Intel test temperature and voltage conditions. Refer to the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2) and the *Processor Power Characterization Methodology* for the details of this methodology.

The case temperature is defined at the geometric top center of the processor. Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP) indicated in Table 26 instead of the maximum processor power consumption. The Thermal Monitor feature is designed to protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained periods of time. For more details on the usage of this feature, refer to Section 5.2. **In all cases the Thermal Monitor or Thermal Monitor 2 feature must be enabled for the processor to remain within specification.**

### Table 26. Processor Thermal Specifications for 775_VR_CONFIG_05A Processors

| Processor Number | Core Frequency (GHz) | Thermal Design Power (W) | Minimum $T_C$ (°C) | Maximum $T_C$ (°C) | Notes |
|---|---|---|---|---|---|
| 631 | 3 GHz | 86 | 5 | See Table 28 and Figure 12 | 1, 2 |
| 641 | 3.20 GHz | 86 | 5 | See Table 28 and Figure 12 | 1, 2 |
| 651 | 3.40 GHz | 86 | 5 | See Table 28 and Figure 12 | 1, 2 |
| 661 | 3.60 GHz | 86 | 5 | See Table 28 and Figure 12 | 1, 2 |

**NOTES:**
1. Thermal Design Power (TDP) should be used for processor thermal solution design targets. The TDP is not the maximum power that the processor can dissipate.
2. This table shows the maximum TDP for a given frequency range. Individual processors may have a lower TDP. Therefore, the maximum $T_C$ will vary depending on the TDP of the individual processor. Refer to Table 28 and Figure 12 for the allowed combinations of power and $T_C$.

### Table 27. Processor Thermal Specifications for 775_VR_CONFIG_06 Processors

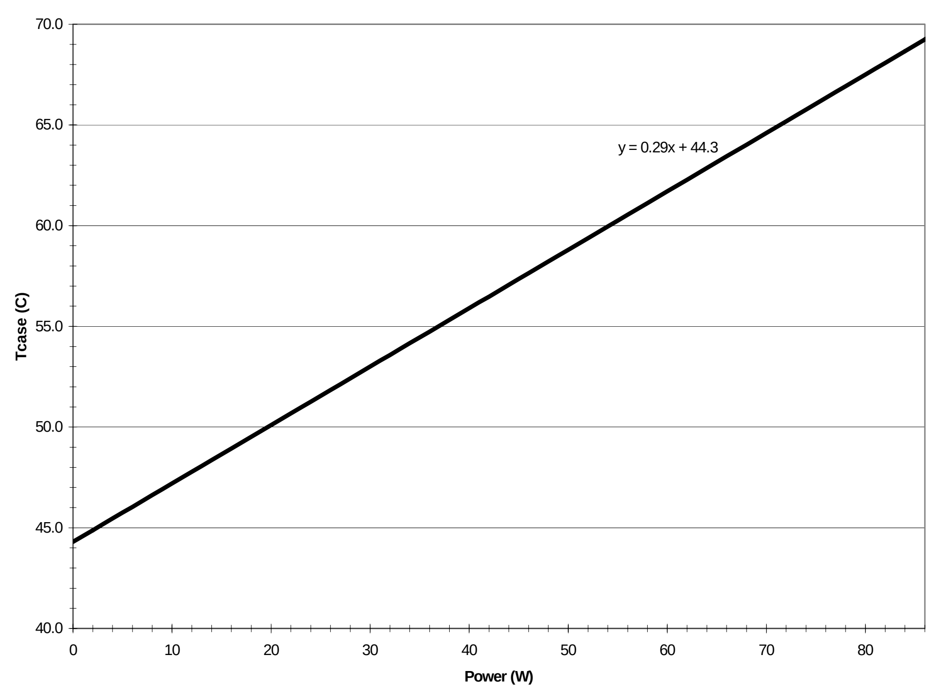
| Processor Number | Core Frequency (GHz) | Thermal Design Power (W) | Minimum $T_C$ (°C) | Maximum $T_C$ (°C) | Notes |
|---|---|---|---|---|---|
| 631<br>641<br>651 | 3 GHz<br>3.20 GHz<br>3.40 GHz | 65<br>65<br>65 | 5<br>5<br>5 | See Table 29and Figure 13 | 1, 2 |

**NOTES:**
1. Thermal Design Power (TDP) should be used for processor thermal solution design targets. The TDP is not the maximum power that the processor can dissipate.
2. This table shows the maximum TDP for a given frequency range. Individual processors may have a lower TDP. Therefore, the maximum $T_C$ will vary depending on the TDP of the individual processor. Refer to thermal profile figure and associated table for the allowed combinations of power and $T_C$.

## Table 28. Thermal Profile for 775_VR_CONFIG_05A Processors

| Power (W) | Maximum $T_C$ (°C) | Power (W) | Maximum $T_C$ (°C) | Power (W) | Maximum $T_C$ (°C) |
|---|---|---|---|---|---|
| 0 | 44.3 | 30 | 53.0 | 60 | 61.7 |
| 2 | 44.9 | 32 | 53.6 | 62 | 62.3 |
| 4 | 45.5 | 34 | 54.2 | 64 | 62.9 |
| 6 | 46.0 | 36 | 54.7 | 66 | 63.4 |
| 8 | 46.6 | 38 | 55.3 | 68 | 64.0 |
| 10 | 47.2 | 40 | 55.9 | 70 | 64.6 |
| 12 | 47.8 | 42 | 56.5 | 72 | 65.2 |
| 14 | 48.4 | 44 | 57.1 | 74 | 65.8 |
| 16 | 48.9 | 46 | 57.6 | 76 | 66.3 |
| 18 | 49.5 | 48 | 58.2 | 78 | 66.9 |
| 20 | 50.1 | 50 | 58.8 | 80 | 67.5 |
| 22 | 50.7 | 52 | 59.4 | 82 | 68.1 |
| 24 | 51.3 | 54 | 60.0 | 84 | 68.7 |
| 26 | 51.8 | 56 | 60.5 | 86 | 69.2 |
| 28 | 52.4 | 58 | 61.1 | | |

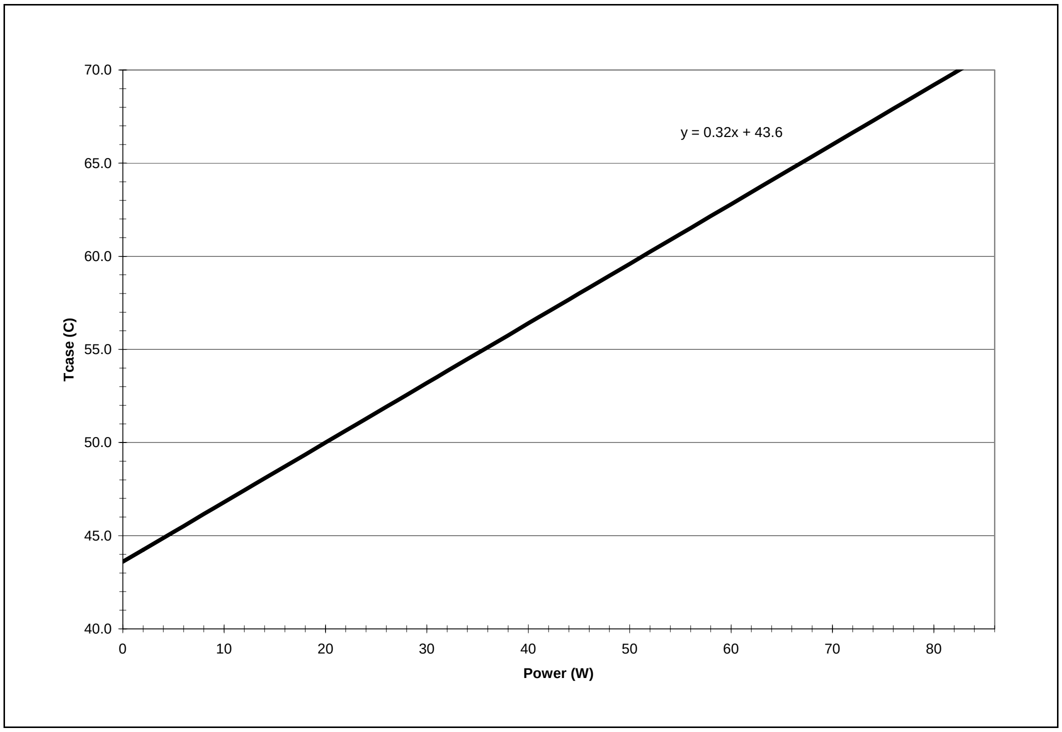
## Figure 12. Thermal Profile for 775_VR_CONFIG_05A Processors



### Table 29. Thermal Profile for 775_VR_CONFIG_06 Processors

| Power (W) | Maximum Tc (°C) | Power (W) | Maximum Tc (°C) |
|---|---|---|---|
| 0 | 43.6 | 34 | 54.5 |
| 2 | 44.2 | 36 | 55.1 |
| 4 | 44.9 | 38 | 55.8 |
| 6 | 45.5 | 40 | 56.4 |
| 8 | 46.2 | 42 | 57.0 |
| 10 | 46.8 | 44 | 57.7 |
| 12 | 47.4 | 46 | 58.3 |
| 14 | 48.1 | 48 | 59.0 |
| 16 | 48.7 | 50 | 59.6 |
| 18 | 49.4 | 52 | 60.2 |
| 20 | 50.0 | 54 | 60.9 |
| 22 | 50.6 | 56 | 61.5 |
| 24 | 51.3 | 58 | 62.2 |
| 26 | 51.9 | 60 | 62.8 |
| 28 | 52.6 | 62 | 63.4 |
| 30 | 53.2 | 64 | 64.1 |
| 32 | 53.8 | | |

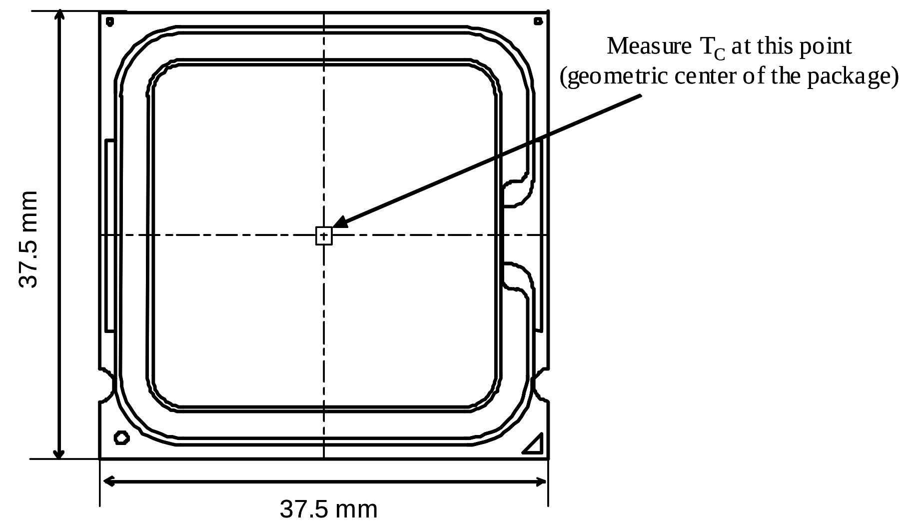
### Figure 13. Thermal Profile for 775_VR_CONFIG_06 Processors



### 5.1.2 Thermal Metrology

The maximum and minimum case temperatures ($T_C$) for the processor is specified in Table 26. This temperature specification is meant to help ensure proper operation of the processor. Figure 14 illustrates where Intel recommends $T_C$ thermal measurements should be made. For detailed guidelines on temperature measurement methodology, refer to the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2).

**Figure 14. Case Temperature ($T_C$) Measurement Location**




## 5.2 Processor Thermal Features

### 5.2.1 Thermal Monitor

The Thermal Monitor feature helps control the processor temperature by activating the thermal control circuit (TCC) when the processor silicon reaches its maximum operating temperature. The TCC reduces processor power consumption by modulating (starting and stopping) the internal processor core clocks. **The Thermal Monitor feature must be enabled for the processor to be operating within specifications.** The temperature at which Thermal Monitor activates the thermal control circuit is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

When the Thermal Monitor feature is enabled and a high temperature situation exists (i.e., TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30–50%). Clocks often will not be off for more than 3.0 microseconds when the TCC is active. Cycle times are processor speed dependent and decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and in some cases may result in a $T_C$ that exceeds the specified maximum temperature; this may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously. Refer to the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2) for information on designing a thermal solution.

The duty cycle for the TCC, when activated by the Thermal Monitor, is factory configured and cannot be modified. The Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

### 5.2.2 Thermal Monitor 2

The Pentium 4 processor also supports an additional power reduction capability known as Thermal Monitor 2. This mechanism provides an efficient means for limiting the processor temperature by reducing the power consumption within the processor.

When Thermal Monitor 2 is enabled, and a high temperature situation is detected, the Thermal Control Circuit (TCC) will be activated. The TCC causes the processor to adjust its operating frequency (via the bus multiplier) and input voltage (via the VID signals). This combination of reduced frequency and VID results in a reduction to the processor power consumption.

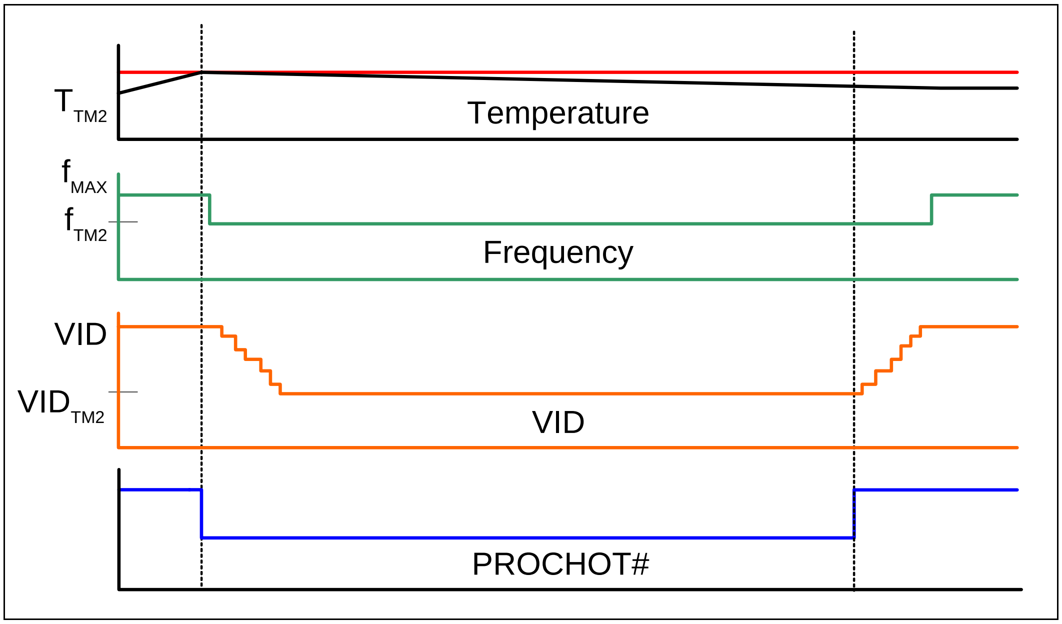
A processor enabled for Thermal Monitor 2 includes two operating points, each consisting of a specific operating frequency and voltage. The first operating point represents the normal operating condition for the processor. Under this condition, the core-frequency-to-FSB multiple used by the processor is that contained in the IA32_PERF_STS MSR and the VID is the one specified in Table 4. These parameters represent normal system operation.

The second operating point consists of both a lower operating frequency and voltage. When the TCC is activated, the processor automatically transitions to the new frequency. This transition occurs very rapidly (on the order of 5 μs). During the frequency transition, the processor is unable to service any bus requests, and consequently, all bus traffic is blocked. Edge-triggered interrupts are latched and kept pending until the processor resumes operation at the new frequency.

Once the new operating frequency is engaged, the processor will transition to the new core operating voltage by issuing a new VID code to the voltage regulator. The voltage regulator must support dynamic VID steps in order to support Thermal Monitor 2. During the voltage change, it will be necessary to transition through multiple VID codes to reach the target operating voltage. Each step will likely be one VID table entry (see Table 4). The processor continues to execute instructions during the voltage transition. Operation at the lower voltage reduces the power consumption of the processor.

A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the operating frequency and voltage transition back to the normal system operating point. Transition of the VID code will occur first, in order to insure proper operation once the processor reaches its normal operating frequency. Refer to Figure 15 for an illustration of this ordering.

**Figure 15. Thermal Monitor 2 Frequency and Voltage Ordering**




The PROCHOT# signal is asserted when a high temperature situation is detected, regardless of whether Thermal Monitor or Thermal Monitor 2 is enabled.

Note that the Thermal Monitor 2 TCC cannot be activated via the on demand mode. The Thermal Monitor TCC, however, can be activated through the use of the on demand mode.

### 5.2.3 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as “On-Demand” mode and is distinct from the Thermal Monitor feature. On-Demand mode is intended as a means to reduce system level power consumption. Systems using the Pentium 4 processor must not rely on software usage of this mechanism to limit the processor temperature.

If bit 4 of the ACPI P_CNT Control Register (located in the processor IA32_THERM_CONTROL MSR) is written to a '1', the processor immediately reduces its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI P_CNT Control Register. In On-Demand mode, the duty cycle can be programmed from 12.5% on/87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used in conjunction with the Thermal Monitor. If the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

### 5.2.4 PROCHOT# Signal

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If the Thermal Monitor is enabled (note that the Thermal Monitor must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#. Refer to the *Intel® 64 and IA-32 Architecture Software Developer's Manuals* for specific register and programming details.

The processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from over-temperature situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

One application is the thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR can cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR, and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. Refer to the *Voltage Regulator-Down (VRD) 10.1 Design Guide For Desktop and Transportable LGA775 Socket* for details on implementing the bi-directional PROCHOT# feature.

### 5.2.5 THERMTRIP# Signal

Regardless of whether or not Thermal Monitor or Thermal Monitor 2 is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature (refer to the THERMTRIP# definition in Table 25). At this point, the FSB signal THERMTRIP# will go active and stay active as described in Table 25. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles.

### 5.2.6 $T_{CONTROL}$ and Fan Speed Reduction

$T_{CONTROL}$ is a temperature specification based on a temperature reading from the thermal diode. The value for $T_{CONTROL}$ will be calibrated in manufacturing and configured for each processor. When $T_{DIODE}$ is above $T_{CONTROL}$, $T_C$ must be at or below $T_{C\text{-}MAX}$ as defined by the thermal profile in Table 28 and Figure 12; otherwise, the processor temperature can be maintained at $T_{CONTROL}$ (or lower) as measured by the thermal diode.

The purpose of this feature is to support acoustic optimization through fan speed control. Contact your Intel representative for further details and documentation.

### 5.2.7 Thermal Diode

The processor incorporates an on-die PNP transistor whose base emitter junction is used as a thermal "diode", with its collector shorted to Ground. A thermal sensor located on the system board may monitor the die temperature of the processor for thermal management and fan speed control. Table 30, Table 31, Table 32, and Table 33 provide the "diode" parameter and interface specifications. Two different sets of "diode" parameters are listed in Table 30 and Table 31. The Diode Model parameters (Table 30) apply to traditional thermal sensors that use the Diode Equation to determine the processor temperature. Transistor Model parameters (Table 31) have been added to support thermal sensors that use the transistor equation method. The Transistor Model may provide more accurate temperature measurements when the diode ideality factor is closer to the maximum or minimum limits. This thermal "diode" is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

### Table 30. Thermal "Diode" Parameters using Diode Model

| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{FW}$ | Forward Bias Current | 5 | — | 200 | µA | 1 |
| n | Diode Ideality Factor | 1.000 | 1.009 | 1.050 | - | 2, 3, 4 |
| $R_T$ | Series Resistance | 2.79 | 4.52 | 6.24 | Ω | 2, 3, 5 |

**NOTES:**

1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized across a temperature range of 50 – 80 °C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:

$$I_{FW} = I_S * (e^{qV_D/nkT} - 1)$$

   where $I_S$ = saturation current, q = electronic charge, $V_D$ = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
5. The series resistance, $R_T$, is provided to allow for a more accurate measurement of the junction temperature. $R_T$, as defined, includes the lands of the processor but does not include any socket resistance or board trace resistance between the socket and the external remote diode thermal sensor. $R_T$ can be used by remote diode thermal sensors with automatic series resistance cancellation to calibrate out this error term. Another application is that a temperature offset can be manually calculated and programmed into an offset register in the remote diode thermal sensors as exemplified by the equation:

$$T_{error} = [R_T * (N-1) * I_{FWmin}] / [nk/q * \ln N]$$

   where $T_{error}$ = sensor temperature error, N = sensor current ratio, k = Boltzmann Constant, q = electronic charge.

### Table 31. Thermal "Diode" Parameters using Transistor Model

| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{FW}$ | Forward Bias Current | 5 | — | 200 | µA | 1, 2 |
| $I_E$ | Emitter Current | 5 | — | 200 | µA | |
| $n_Q$ | Transistor Ideality | 0.997 | 1.001 | 1.005 | — | 3, 4, 5 |
| Beta | | 0.391 | — | 0.760 | — | 3, 4 |
| $R_T$ | Series Resistance | 2.79 | 4.52 | 6.24 | Ω | 3, 6 |

**NOTES:**

1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Same as $I_{FW}$ in Table 30.
3. Characterized across a temperature range of 50 – 80 °C.
4. Not 100% tested. Specified by design characterization.
5. The ideality factor, nQ, represents the deviation from ideal transistor model behavior as exemplified by the equation for the collector current:

$$I_C = I_S * (e^{qV_{BE}/n_QkT} - 1)$$

   Where $I_S$ = saturation current, q = electronic charge, $V_{BE}$ = voltage across the transistor base emitter junction (same nodes as VD), k = Boltzmann Constant, and T = absolute temperature (Kelvin).
6. The series resistance, $R_{T,}$ provided in the Diode Model Table (Table 30) can be used for more accurate readings as needed.

When calculating a temperature based on thermal diode measurements, a number of parameters must be either measured or assumed. Most devices measure the diode ideality and assume a series resistance and ideality trim value, although some are capable of also measuring the series resistance. Calculating the temperature is then accomplished using the equations listed under Table 30. In most temperature sensing devices, an expected value for the diode ideality is designed-in to the temperature calculation equation. If the designer of the temperature sensing device assumes a perfect diode the ideality value (also called $n_{trim}$) will be 1.000. Given that most diodes are not perfect, the designers usually select an $n_{trim}$ value that more closely matches the behavior of the diodes in the processor. If the processors diode ideality deviates from that of $n_{trim}$, each calculated temperature will be offset by a fixed amount. This temperature offset can be calculated with the equation:

$$T_{error(nf)} = T_{measured} \text{ X } (1 - n_{actual}/n_{trim})$$

Where $T_{error(nf)}$ is the offset in degrees C, $T_{measured}$ is in Kelvin, $n_{actual}$ is the measured ideality of the diode, and $n_{trim}$ is the diode ideality assumed by the temperature sensing device.

To improve the accuracy of diode based temperature measurements, a new register ($T_{diode\_Offset}$) has been added to processor that will contain thermal diode characterization data. During manufacturing each processors thermal diode will be evaluated for its behavior relative to a theoretical diode. Using the equation above, the temperature error created by the difference between $n_{trim}$ and the actual ideality of the particular processor will be calculated. This value ($T_{diode\_Offset}$) will be programmed in to the new diode correction MSR and when added to the $T_{diode\_Base}$ value can be used to correct temperatures read by diode based temperature sensing devices.

If the $n_{trim}$ value used to calculate $T_{diode\_Offset}$ differs from the $n_{trim}$ value used in a temperature sensing device, the $T_{error(nf)}$ may not be accurate. If desired, the $T_{diode\_Offset}$ can be adjusted by calculating $n_{actual}$ and then recalculating the offset using the actual $n_{trim}$ as defined in the temperature sensor manufacturers' datasheet.

The Diode_Base value and $n_{trim}$ used to calculate the Diode_Correction_Offset are listed in Table 32.

**Table 32. Thermal “Diode” $n_{trim}$ and Diode_Correction_Offset**

| Symbol | Parameter | | Unit |
|---|---|---|---|
| $n_{trim}$ | Diode ideality used to calculate Diode_Offset | 1.008 | — |
| Diode_Base | | 0 | °C |

**Table 33. Thermal Diode Interface**

| Signal Name | Land Number | Signal Description |
|---|---|---|
| THERMDA | AL1 | diode anode |
| THERMDC | AK1 | diode cathode |

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# 6 Features

## 6.1 Power-On Configuration Options

Several configuration options can be configured by hardware. The Pentium 4 processor samples the hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifications on these options, refer to Table 34.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset. All resets reconfigure the processor; for reset purposes, the processor does not distinguish between a "warm" reset and a "power-on" reset.

### Table 34. Power-On Configuration Option Signals

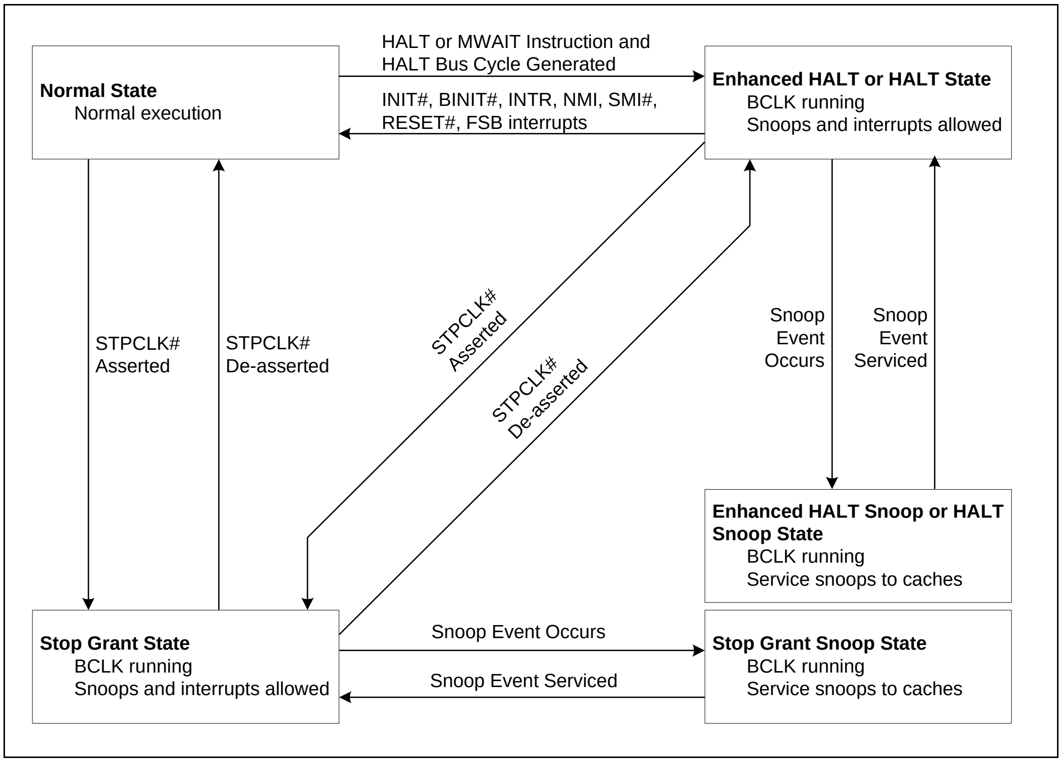
| Configuration Option | Signal[1,2] |
|---|---|
| Output tristate | SMI# |
| Execute BIST | INIT# |
| In Order Queue pipelining (set IOQ depth to 1) | A7# |
| Disable MCERR# observation | A9# |
| Disable BINIT# observation | A10# |
| APIC Cluster ID (0-3) | A[12:11]# |
| Disable bus parking | A15# |
| Disable Hyper-Threading Technology | A31# |
| Symmetric agent arbitration ID | BR0# |
| RESERVED | A[6:3]#, A8#, A[14:13]#, A[16:35]# |

**NOTES:**
1. Asserting this signal during RESET# will select the corresponding option.
2. Address signals not identified in this table as configuration options should not be asserted during RESET#.

## 6.2 Clock Control and Low Power States

The processor allows the use of AutoHALT and Stop-Grant states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 16 for a visual representation of the processor low power states.

### Figure 16. Processor Low Power State Machine




## 6.2.1 Normal State

This is the normal operating state for the processor.

## 6.2.2 HALT and Enhanced HALT Powerdown States

The Pentium 4 processor supports the HALT or Enhanced HALT powerdown state. The Enhanced HALT Powerdown state is configured and enabled via the BIOS. The Enhanced HALT state must be enabled via the BIOS for the processor to remain within its specifications.

The Enhanced HALT state is a lower power state as compared to the Stop Grant State.

If Enhanced HALT is not enabled, the default Powerdown state entered will be HALT. Refer to the following sections for details about the HALT and Enhanced HALT states.

### 6.2.2.1 HALT Powerdown State

HALT is a low power state entered when all the logical processors have executed the HALT or MWAIT instructions. When one of the logical processors executes the HALT instruction, that logical processor is halted; however, the other processor continues normal operation. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the HALT Power Down state. See the *Intel® 64 and IA-32 Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the HALT Power Down state. See the *Intel® 64 and IA-32 Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the HALT Power Down state. When the system de-asserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in HALT Power Down state, the processor will process bus snoops.

#### 6.2.2.2 Enhanced HALT Powerdown State

Enhanced HALT is a low power state entered when all logical processors have executed the HALT or MWAIT instructions and Enhanced HALT has been enabled via the BIOS. When one of the logical processors executes the HALT instruction, that logical processor is halted; however, the other processor continues normal operation.

The processor will automatically transition to a lower frequency and voltage operating point before entering the Enhanced HALT state. Note that the processor FSB frequency is not altered; only the internal core frequency is changed. When entering the low power state, the processor will first switch to the lower bus ratio and then transition to the lower VID.

While in Enhanced HALT state, the processor will process bus snoops.

The processor exits the Enhanced HALT state when a break event occurs. When the processor exits the Enhanced HALT state, it will first transition the VID to the original value and then change the bus ratio back to the original value.

### 6.2.3 Stop Grant State

When the STPCLK# signal is asserted, the Stop Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle.

Since the GTL+ signals receive power from the FSB, these signals should not be driven (allowing the level to return to $V_{TT}$) for minimum power drawn by the termination resistors in this state. In addition, all other input signals on the FSB should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop Grant state. The event will be latched and can be serviced by software upon exit from the Stop Grant state.

RESET# causes the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the de-assertion of the STPCLK# signal.

A transition to the Grant Snoop state will occur when the processor detects a snoop on the FSB (see Section 6.2.4).

While in the Stop-Grant State, SMI#, INIT#, BINIT#, and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal State. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor will process a FSB snoop.

## 6.2.4 Enhanced HALT Snoop or HALT Snoop State, Stop Grant Snoop State

The Enhanced HALT Snoop State is used in conjunction with the new Enhanced HALT state. If Enhanced HALT state is not enabled in the BIOS, the default Snoop State entered will be the HALT Snoop State. Refer to the following sections for details on HALT Snoop State, Grant Snoop State and Enhanced HALT Snoop State.

### 6.2.4.1 HALT Snoop State, Stop Grant Snoop State

The processor will respond to snoop transactions on the FSB while in Stop-Grant state or in HALT Power Down state. During a snoop transaction, the processor enters the HALT Snoop State:Stop Grant Snoop state. The processor will stay in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB). After the snoop is serviced, the processor will return to the Stop Grant state or HALT Power Down state, as appropriate.

### 6.2.4.2 Enhanced HALT Snoop State

The Enhanced HALT Snoop State is the default Snoop State when the Enhanced HALT state is enabled via the BIOS. The processor will remain in the lower bus ratio and VID operating point of the Enhanced HALT state.

While in the Enhanced HALT Snoop State, snoops are handled the same way as in the HALT Snoop State. After the snoop is serviced the processor will return to the Enhanced HALT state.

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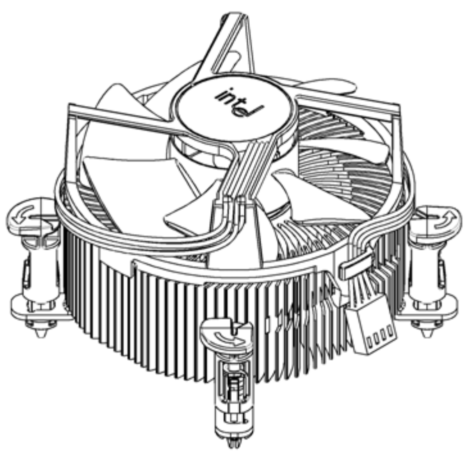
# 7 Boxed Processor Specifications

The Intel Pentium 4 processor will also be offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from baseboards and standard components. The boxed Pentium 4 processor will be supplied with a cooling solution. This chapter documents baseboard and system requirements for the cooling solution that will be supplied with the boxed Pentium 4 processor. This chapter is particularly important for OEMs that manufacture baseboards for system integrators. Unless otherwise noted, all figures in this chapter are dimensioned in millimeters and inches [in brackets]. Figure 17 shows a mechanical representation of a boxed Pentium 4 processor.

***Note:*** Drawings in this section reflect only the specifications on the Intel boxed processor product. These dimensions should not be used as a generic keep-out zone for all cooling solutions. It is the system designers' responsibility to consider their proprietary cooling solution when designing to the required keep-out zone on their system platforms and chassis. Refer to the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2) for further guidance.

**Figure 17. Mechanical Representation of the Boxed Processor**



**NOTE:** The airflow of the fan heatsink is into the center and out of the sides of the fan heatsink.

## 7.1 Mechanical Specifications

### 7.1.1 Boxed Processor Cooling Solution Dimensions

This section documents the mechanical specifications of the boxed Pentium 4 processor. The boxed processor will be shipped with an unattached fan heatsink. Figure 17 shows a mechanical representation of the boxed Pentium 4 processor.

Clearance is required around the fan heatsink to ensure unimpeded airflow for proper cooling. The physical space requirements and dimensions for the boxed processor with assembled fan heatsink are shown in Figure 18 (Side View), and Figure 19 (Top View). The airspace requirements for the boxed processor fan heatsink must also be incorporated into new baseboard and system designs. Airspace requirements are shown in Figure 23 and Figure 24. Note that some figures have centerlines shown (marked with alphabetic designations) to clarify relative dimensioning.

**Figure 18. Space Requirements for the Boxed Processor (Side View; applies to all four side views)**

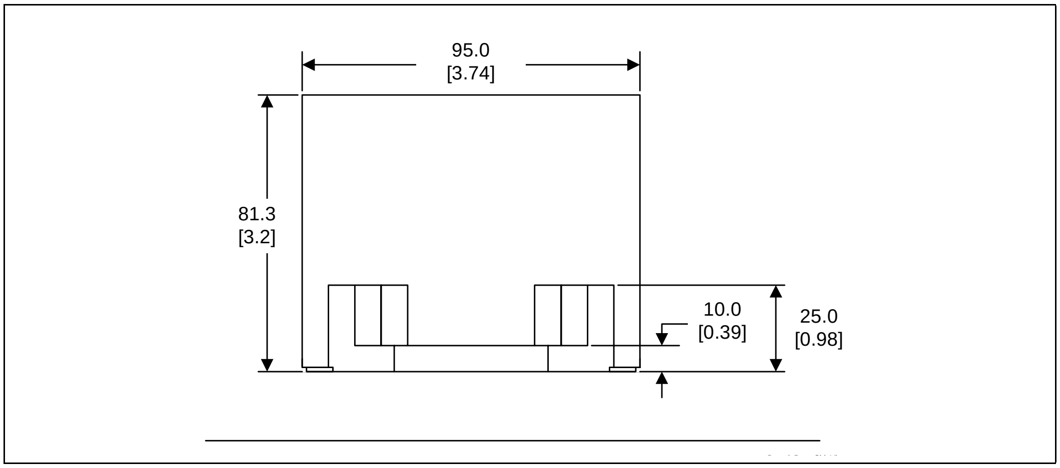
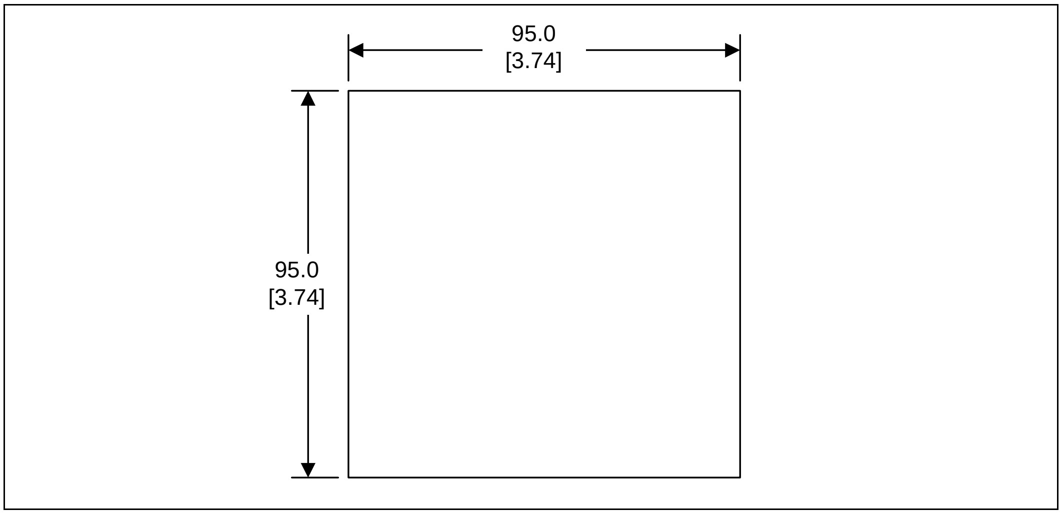


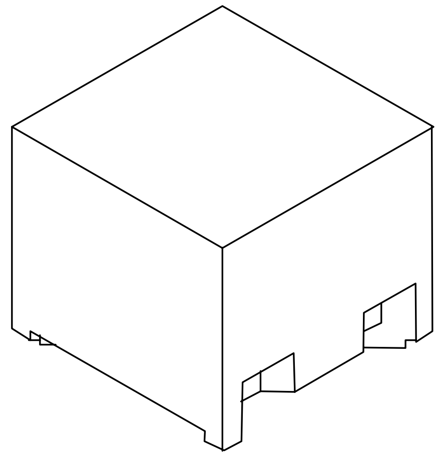

**Figure 19. Space Requirements for the Boxed Processor (Top View)**




**NOTES:**

1. The boxed Pentium 4 processor in the 775-land package cooling solution with clip is currently under development and, at this time, is preliminary. The diagrams shown may not reflect the final product.
2. Diagram does not show the attached hardware for the clip design and is provided only as a mechanical representation.

**Figure 20. Space Requirements for the Boxed Processor (Overall View)**



### 7.1.2 Boxed Processor Fan Heatsink Weight

The boxed processor fan heatsink will not weigh more than 550 grams. See Chapter 5 and the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2) for details on the processor weight and heatsink requirements.

### 7.1.3 Boxed Processor Retention Mechanism and Heatsink Attach Clip Assembly

The boxed processor thermal solution requires a heatsink attach clip assembly, to secure the processor and fan heatsink in the baseboard socket. The boxed processor will ship with the heatsink attach clip assembly.

## 7.2 Electrical Requirements

### 7.2.1 Fan Heatsink Power Supply

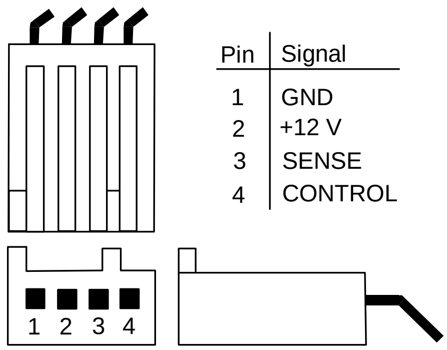
The boxed processor's fan heatsink requires a +12 V power supply. A fan power cable will be shipped with the boxed processor to draw power from a power header on the baseboard. The power cable connector and pinout are shown in Figure 21. Baseboards must provide a matched power header to support the boxed processor. Table 35 contains specifications for the input and output signals at the fan heatsink connector. The fan heatsink outputs a SENSE signal, which is an open-collector output that pulses at a rate of two pulses per fan revolution. A baseboard pull-up resistor provides $V_{OH}$ to match the system board-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

The fan heatsink receives a PWM signal from the motherboard from the fourth pin of the connector labeled as CONTROL.

***Note:*** The boxed processor’s fan heatsink requires a constant +12 V supplied to pin 2 and does not support variable voltage control or 3-pin PWM control.

The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the platform documentation, or on the system board itself. Figure 22 shows the location of the fan power connector relative to the processor socket. The baseboard power header should be positioned within 4.33 inches from the center of the processor socket.

## Figure 21. Boxed Processor Fan Heatsink Power Cable Connector Description




Straight square pin, 4-pin terminal housing with polarizing ribs and friction locking ramp.

0.100" pitch, 0.025" square pin width.

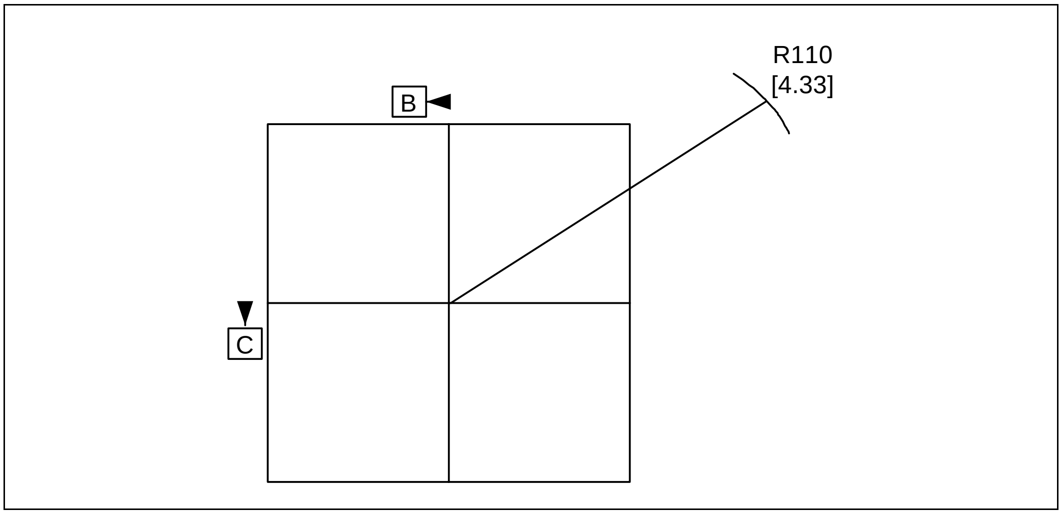
Match with straight pin, friction lock header on mainboard.

## Table 35. Fan Heatsink Power and Signal Specifications

| Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| +12 V: 12 volt fan power supply | 10.2 | 12 | 13.8 | V | |
| IC:<br>Peak Fan current draw<br>Fan start-up current draw<br>Fan start-up current draw maximum duration | <br>—<br>—<br>— | <br>1.1<br>—<br>— | <br>1.5<br>2.2<br>1.0 | <br>A<br>A<br>Second | |
| SENSE: SENSE frequency | — | 2 | — | pulses per fan revolution | 1 |
| CONTROL | 21 | 25 | 28 | kHz | 2,3 |

**NOTES:**
1. Baseboard should pull this pin up to 5 V with a resistor.
2. Open Drain Type, Pulse Width Modulated.
3. Fan will have a pull-up resistor to 4.75 V, maximum 5.25 V.

**Figure 22. Baseboard Power Header Placement Relative to Processor Socket**




## 7.3 Thermal Specifications

This section describes the cooling requirements of the fan heatsink solution used by the boxed processor.

### 7.3.1 Boxed Processor Cooling Requirements

The boxed processor may be directly cooled with a fan heatsink. However, meeting the processor's temperature specification is also a function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specification is in Chapter 5. The boxed processor fan heatsink is able to keep the processor temperature within the specifications in chassis that provide good thermal management. For the boxed processor fan heatsink to operate properly, it is critical that the airflow provided to the fan heatsink is unimpeded. Airflow of the fan heatsink is into the center and out of the sides of the fan heatsink. Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 23 and Figure 24 illustrate an acceptable airspace clearance for the fan heatsink. The air temperature entering the fan should be kept below 38 °C. A Thermally Advantaged Chassis with an Air Guide 1.1 is recommended to meet the 38 °C requirement. Again, meeting the processor's temperature specification is the responsibility of the system integrator.

***Note:*** The processor fan is the primary source of airflow for cooling the $V_{CC}$ voltage regulator. Dedicated voltage regulator cooling components may be necessary if the selected fan is not capable of keeping regulator components below maximum rated temperatures.

**Figure 23. Boxed Processor Fan Heatsink Airspace Keep-out Requirements (Side 1 View)**

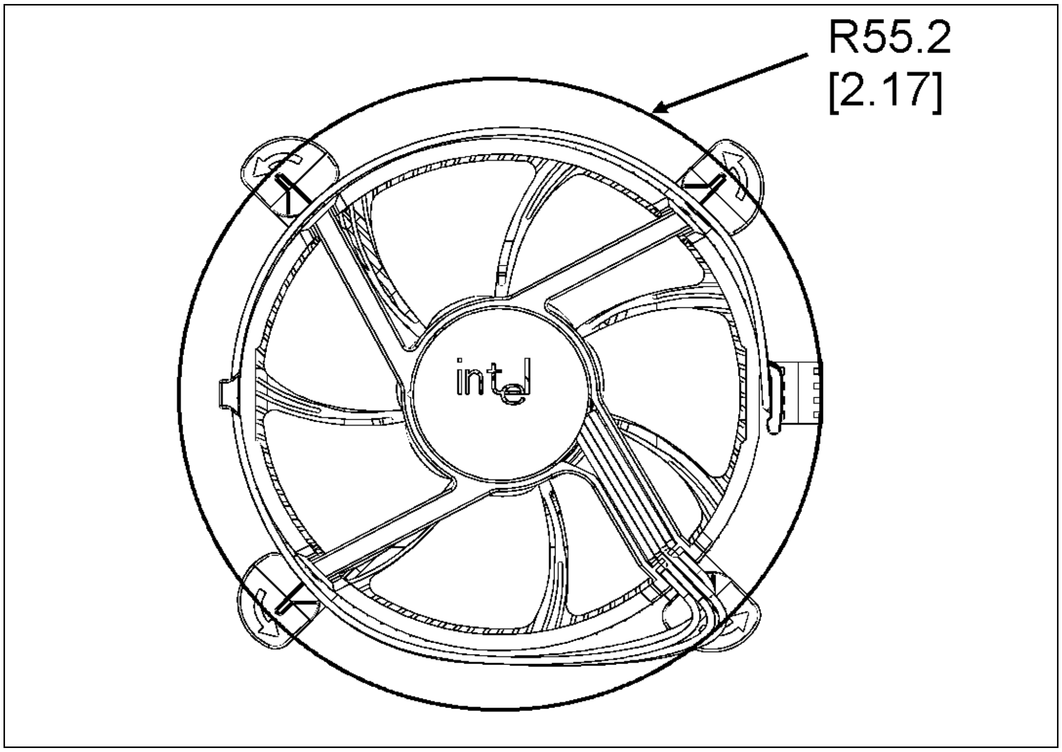
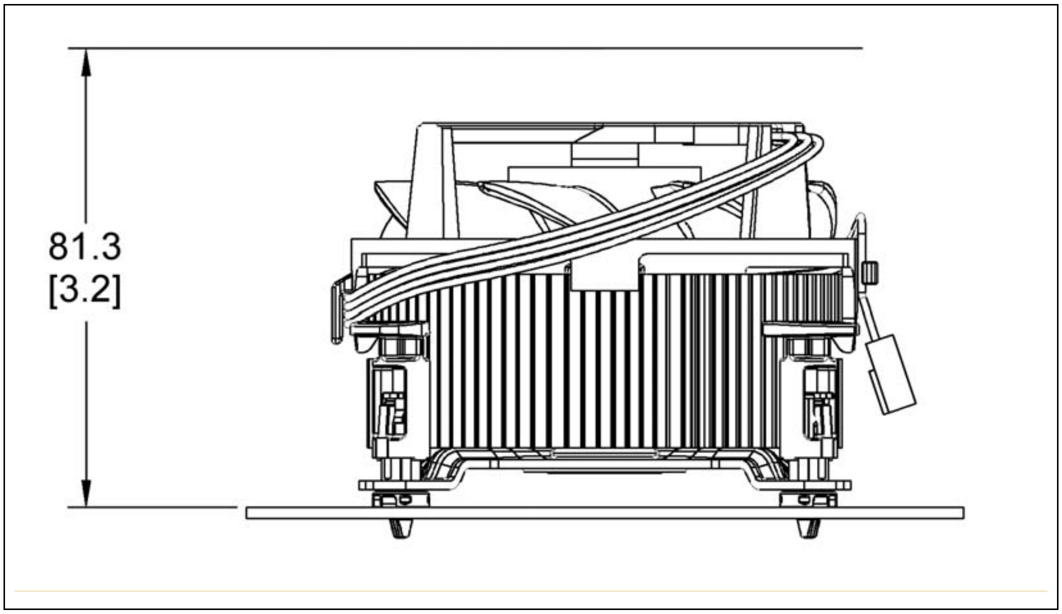



**Figure 24. Boxed Processor Fan Heatsink Airspace Keep-out Requirements (Side 2 View)**

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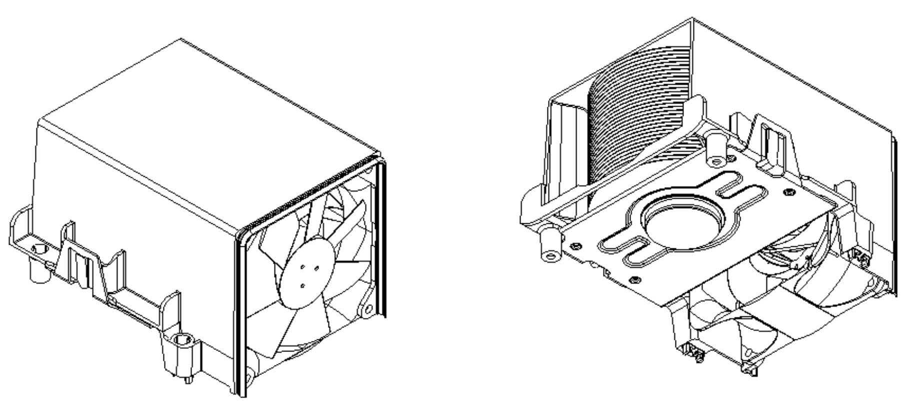
# 8 Balanced Technology Extended (BTX) Boxed Processor Specifications

The Intel Pentium 4 processors will be offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from largely standard components. The boxed Intel Pentium 4 processor will be supplied with a cooling solution known as the Thermal Module Assembly (TMA). Each processor will be supplied with one of the two available types of TMAs – Type I or Type II. This chapter documents motherboard and system requirements for both the TMAs that will be supplied with the boxed Pentium 4 processor in the 775-land package. This chapter is particularly important for OEMs that manufacture motherboards for system integrators. Figure 25 shows a mechanical representation of a boxed Pentium 4 processor in the 775-land package with a Type I TMA. Figure 26 illustrates a mechanical representation of a boxed Pentium 4 processor in the 775-land package with Type II TMA.

***Note:*** Unless otherwise noted, all figures in this chapter are dimensioned in millimeters and inches [in brackets].

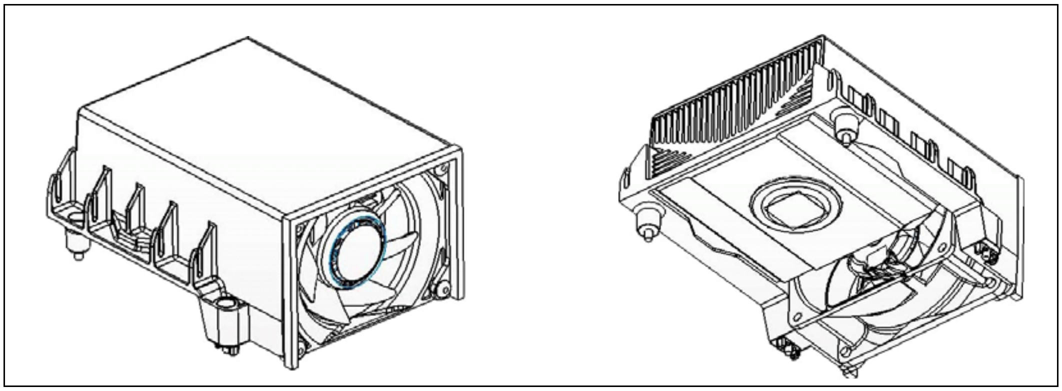
***Note:*** Drawings in this section reflect only the specifications on the Intel boxed processor product. These dimensions should not be used as a generic keep-out zone for all cooling solutions. It is the system designer's responsibility to consider their proprietary cooling solution when designing to the required keep-out zone on their system platforms and chassis. Refer to the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2) for further guidance.

**Figure 25. Mechanical Representation of the Boxed Processor with a Type I TMA**



**NOTE: The duct, clip, heatsink, and fan can differ from this drawing representation but the basic shape and size will remain the same.**

**Figure 26. Mechanical Representation of the Boxed Processor with a Type II TMA**



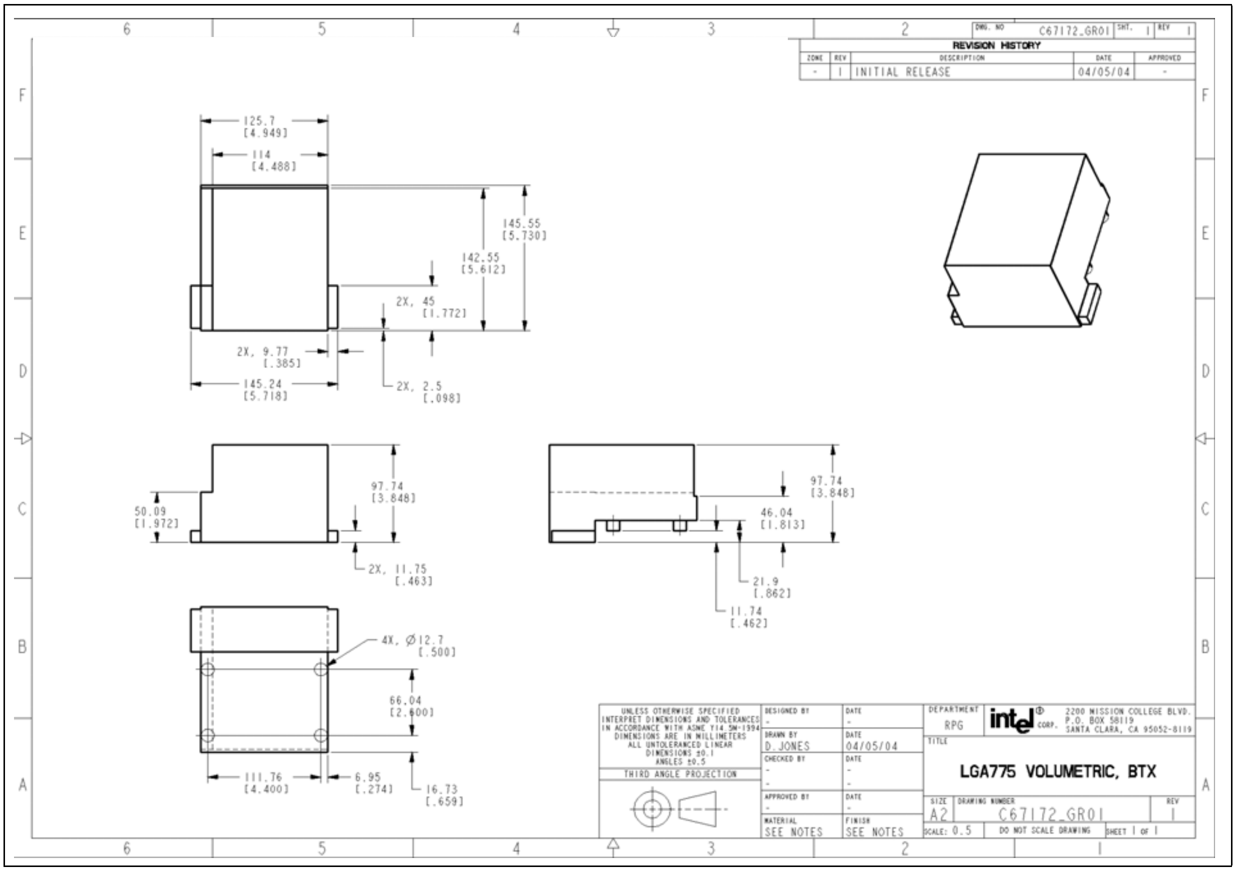
**NOTE: The duct, clip, heatsink and fan can differ from this drawing representation but the basic shape and size will remain the same.**

## 8.1 Mechanical Specifications

### 8.1.1 Balanced Technology Extended (BTX) Type I and Type II Boxed Processor Cooling Solution Dimensions

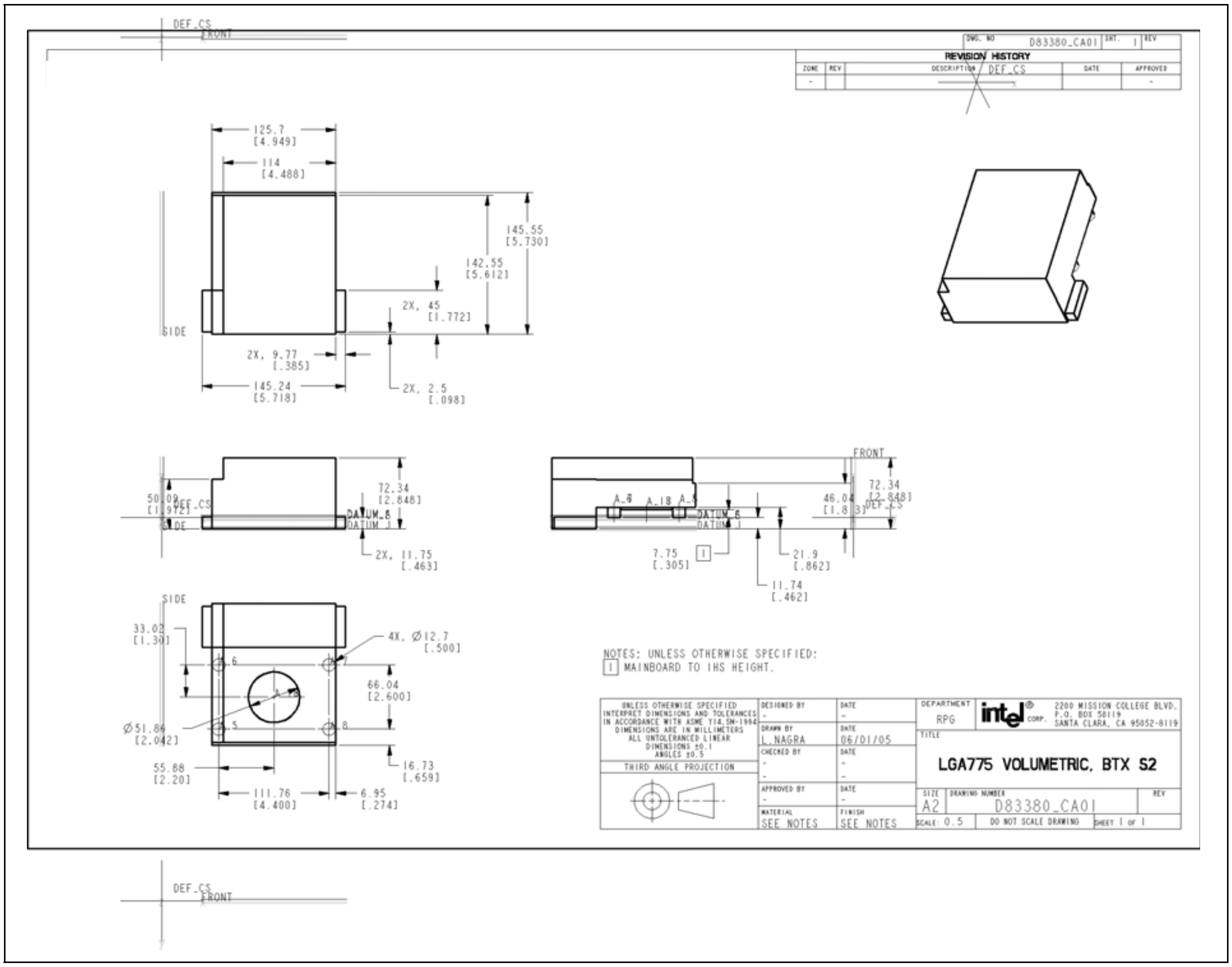
This section documents the mechanical specifications of the boxed Intel Pentium 4 processor TMA. The boxed processor will be shipped with an unattached TMA. Figure 27 shows a mechanical representation of the boxed Pentium 4 processor in the 775-land package for Type I TMA. Figure 28 shows a mechanical representation of the boxed Pentium 4 processor in the 775-land package for Type II TMA. The physical space requirements and dimensions for the boxed processor with assembled fan thermal module are shown.

## Figure 27. Requirements for the Balanced Technology Extended (BTX) Type I Keep-out Volumes




**NOTE:** Diagram does not show the attached hardware for the clip design and is provided only as a mechanical representation.

**Figure 28. Requirements for the Balanced Technology Extended (BTX) Type II Keep-out Volume**




**NOTE:** Diagram does not show the attached hardware for the clip design and is provided only as a mechanical representation.

## 8.1.2 Boxed Processor Thermal Module Assembly Weight

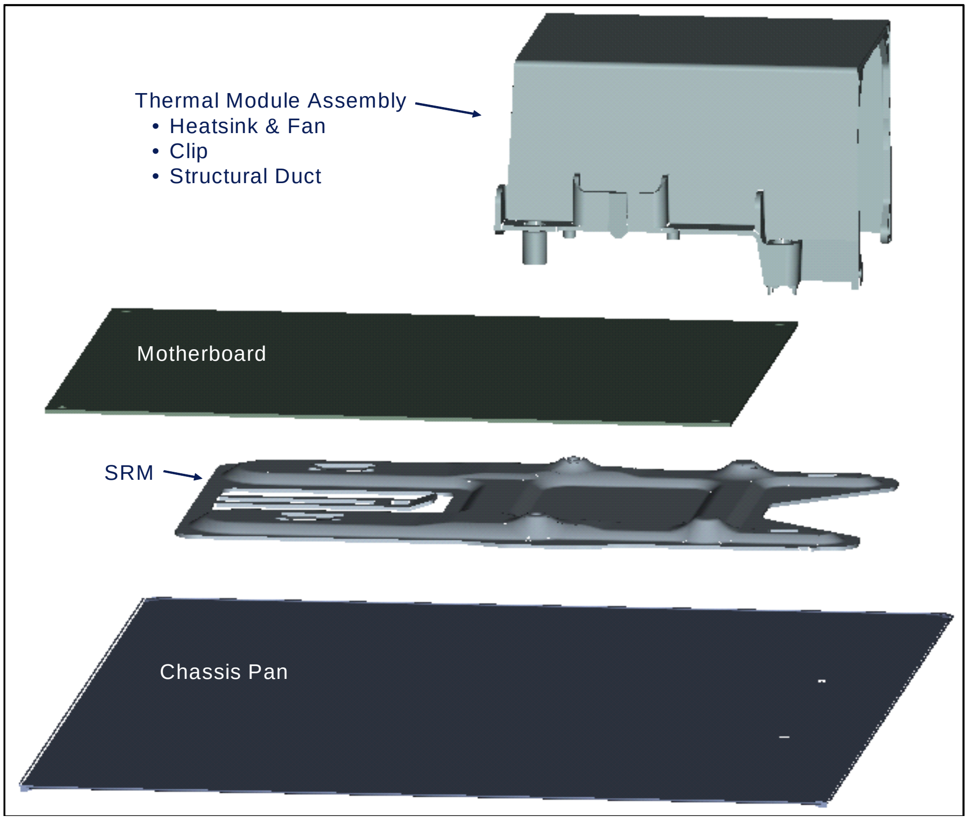
The boxed processor thermal module assembly for Type I BTX will not weigh more than 1200 grams. The boxed processor thermal module assembly for Type II BTX will not weigh more than 1200 grams. See Chapter 5 and the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2) for details on the processor weight and thermal module assembly requirements.

## 8.1.3 Boxed Processor Support and Retention Module (SRM)

The boxed processor TMA requires an SRM assembly provided by the chassis manufacturer. The SRM provides the attach points for the TMA and provides structural support for the board by distributing the shock and vibration loads to the chassis base pan. The boxed processor TMA will ship with the heatsink attach clip assembly, duct and screws for attachment. The SRM must be supplied by the chassis hardware vendor. See the *Support and Retention Module (SRM) External Design Requirements*

*Document*, *Balanced Technology Extended (BTX) System Design Guide*, and the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2) for more detailed information regarding the support and retention module and chassis interface and keepout zones. Figure 29 illustrates the assembly stack including the SRM.

**Figure 29. Assembly Stack Including the Support and Retention Module**




## 8.2 Electrical Requirements

### 8.2.1 Thermal Module Assembly Power Supply

The boxed processor's Thermal Module Assembly (TMA) requires a +12 V power supply. The TMA will include power cable to power the integrated fan and will plug into the 4-wire fan header on the baseboard. The power cable connector and pinout are shown in Figure 30. Baseboards must provide a compatible power header to support the boxed processor. Table 36 contains specifications for the input and output signals at the TMA.

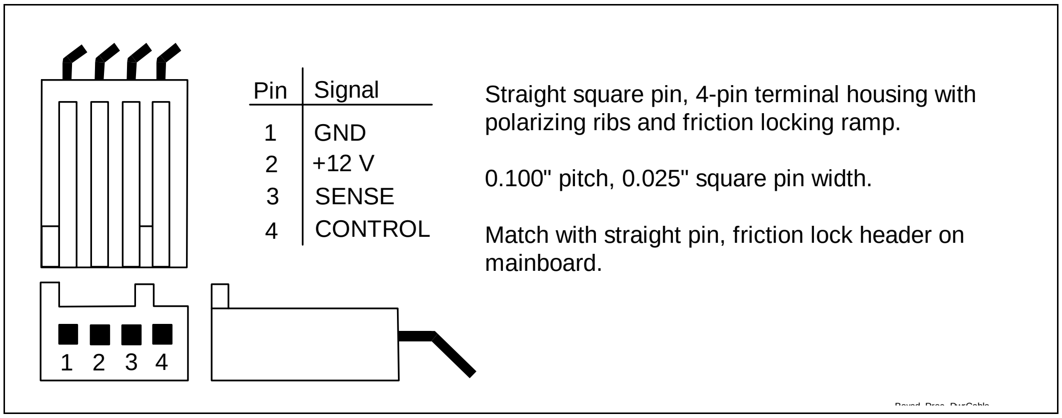
The TMA outputs a SENSE signal, which is an open- collector output that pulses at a rate of 2 pulses per fan revolution. A baseboard pull-up resistor provides $V_{OH}$ to match the system board-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

The TMA receives a Pulse Width Modulation (PWM) signal from the motherboard from the $4^{th}$ pin of the connector labeled as CONTROL.

***Note:*** The boxed processor's TMA requires a constant +12 V supplied to pin 2 and does not support variable voltage control or 3-pin PWM control.

The power header on the baseboard must be positioned to allow the TMA power cable to reach it. The power header identification and location should be documented in the platform documentation, or on the system board itself. Figure 31 shows the location of the fan power connector relative to the processor socket. The baseboard power header should be positioned within 4.33 inches from the center of the processor socket.

### Figure 30. Boxed Processor TMA Power Cable Connector Description

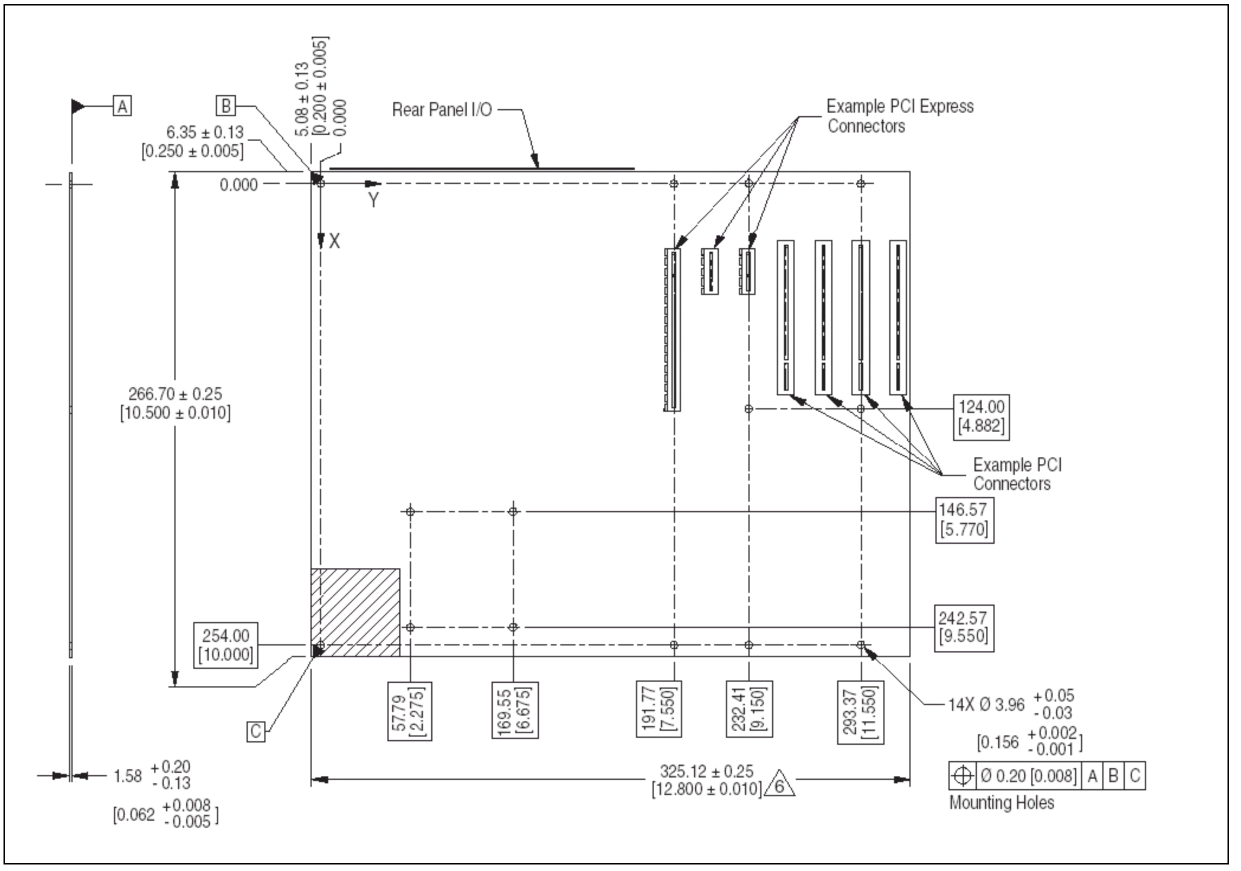



### Table 36. TMA Power and Signal Specifications

| Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| +12 V: 12 volt fan power supply | 10.2 | 12 | 13.8 | V | |
| IC:<br>Peak Fan current draw<br>Fan start-up current draw<br>Fan start-up current draw maximum duration | <br>—<br>—<br>— | <br>1.0<br>—<br>— | <br>1.5<br>2.0<br>1.0 | <br>A<br>A<br>Second | |
| SENSE: SENSE frequency | — | 2 | — | pulses per fan revolution | 1 |
| CONTROL | 21 | 25 | 28 | kHz | 2,3 |

**NOTES:**
1. Baseboard should pull this pin up to 5 V with a resistor.
2. Open Drain Type, Pulse Width Modulated.
3. Fan will have a pull-up resistor to 4.75 V, maximum 5.25 V.

**Figure 31. Balanced Technology Extended (BTX) Mainboard Power Header Placement (Hatched Area)**




## 8.3 Thermal Specifications

This section describes the cooling requirements of the thermal module assembly solution used by the boxed processor.

### 8.3.1 Boxed Processor Cooling Requirements

The boxed processor may be directly cooled with a TMA. However, meeting the processor's temperature specification is also a function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor case temperature specification is in Chapter 5. The boxed processor TMA is able to keep the processor temperature within the specifications in Table 26 for chassis that provide good thermal management. For the boxed processor TMA to operate properly, it is critical that the airflow provided to the TMA is unimpeded. Airflow of the TMA is into the duct and out of the rear of the duct in a linear flow. Blocking the airflow to the TMA inlet reduces the cooling efficiency and decreases fan life. Filters will reduce or impede airflow which will result in a reduced performance of the TMA. The air temperature entering the fan should be kept below 35.5°C. Again, meeting the processor's temperature specification is the responsibility of the system integrator.

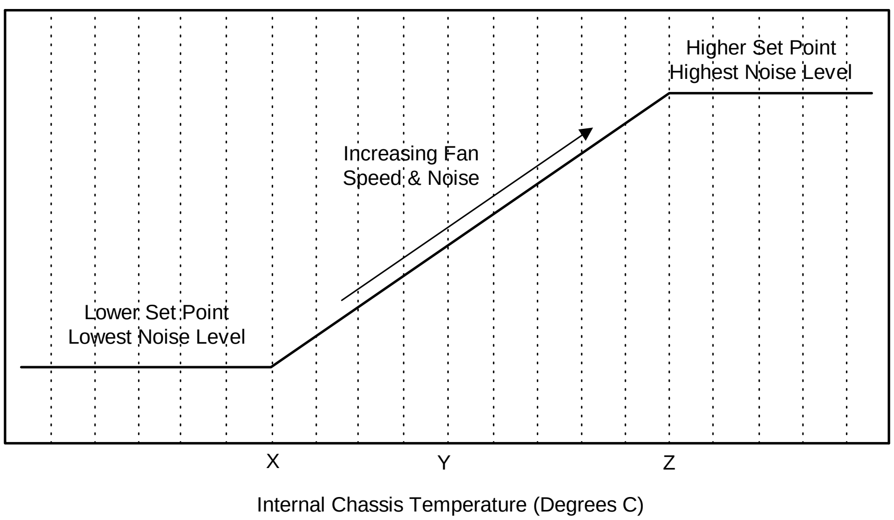
In addition, Type I TMA must be used with Type I chassis only and Type II TMA with Type II chassis only. Type I TMA will not fit in a Type II chassis due to the height difference. In the event a Type II TMA is installed in a Type I chassis, the gasket on the chassis will not seal against the Type II TMA and poor acoustic performance will occur as a result.

### 8.3.2 Variable Speed Fan

The boxed processor fan will operate at different speeds over a short range of temperatures based on a thermistor located in the fan hub area. This allows the boxed processor fan to operate at a lower speed and noise level while thermistor temperatures are low. If the thermistor senses a temperatures increase beyond a lower set point, the fan speed will rise linearly with the temperature until the higher set point is reached. At that point, the fan speed is at its maximum. As fan speed increases, so do fan noise levels. These set points are represented in Figure 32 and Table 37. The internal chassis temperature should be kept below 35.5°C. Meeting the processor's temperature specification (see Chapter 5) is the responsibility of the system integrator.

***Note:*** The motherboard must supply a constant +12 V to the processor's power header to ensure proper operation of the variable speed fan for the boxed processor (refer to Table 37) for the specific requirements).

**Figure 32. Boxed Processor TMA Set Points**



### Table 37. TMA Set Points for 3-wire operation of BTX Type I and Type II Boxed Processors

| Boxed Processor TMA Set Point (°C) | Boxed Processor Fan Speed | Notes |
|---|---|---|
| X ≤ 23 | When the internal chassis temperature is below or equal to this set point, the fan operates at its lowest speed. Recommended maximum internal chassis temperature for nominal operating environment. | 1 |
| Y = 29 | When the internal chassis temperature is at this point, the fan operates between its lowest and highest speeds. Recommended maximum internal chassis temperature for worst-case operating environment. | |
| Z ≥ 35.5 | When the internal chassis temperature is above or equal to this set point, the fan operates at its highest speed. | 1 |

**NOTES:**
1. Set point variance is approximately ±1°C from Thermal Module Assembly to Thermal Module Assembly.

If the boxed processor TMA 4-pin connector is connected to a 4-pin motherboard header and the motherboard is designed with a fan speed controller with PWM output (see CONTROL in Table 36) and remote thermal diode measurement capability, the boxed processor will operate as described in the following paragraphs.

As processor power has increased, the required thermal solutions have generated increasingly more noise. Intel has added an option to the boxed processor that allows system integrators to have a quieter system in the most common usage.

The 4-wire PWM controlled fan in the TMA solution provides better control over chassis acoustics. It allows better granularity of fan speed and lowers overall fan speed than a voltage-controlled fan. Fan RPM is modulated through the use of an ASIC located on the motherboard that sends out a PWM control signal to the $4^{th}$ pin of the connector labeled as CONTROL. The fan speed is based on a combination of actual processor temperature and thermistor temperature.

If the 4-wire PWM controlled fan in the TMA solution is connected to a 3-pin baseboard processor fan header it will default back to a thermistor controlled mode, allowing compatibility with existing 3-pin baseboard designs. Under thermistor controlled mode, the fan RPM is automatically varied based on the $T_{inlet}$ temperature measured by a thermistor located at the fan inlet.

For more details on specific motherboard requirements for 4-wire based fan speed control see the appropriate processor Thermal and Mechanical Design Guidelines (see Section 1.2).

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# 9 Debug Tools Specifications

## 9.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging Pentium 4 processor systems. Tektronix and Agilent should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Pentium 4 processor systems, the LAI is critical in providing the ability to probe and capture FSB signals. There are two sets of considerations to keep in mind when designing a Pentium 4 processor system that can make use of an LAI: mechanical and electrical.

### 9.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the processor. The LAI lands plug into the processor socket, while the processor lands plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may differ from the space normally occupied by the processor heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

### 9.1.2 Electrical Considerations

The LAI will also affect the electrical performance of the FSB; therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution it provides.

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