

# MN4021B/MN4021BS

## 8-Bit Static Shift Register

### Outline

The MN4031B/S consisting of eight register cells which respectively have parallel inputs is an 8-bit static shift register to enable both clock synchronizing series input/series output conversion and parallel input/series output conversion by control of the parallel/series control input (PL).

### Truth Table

#### Serial operation

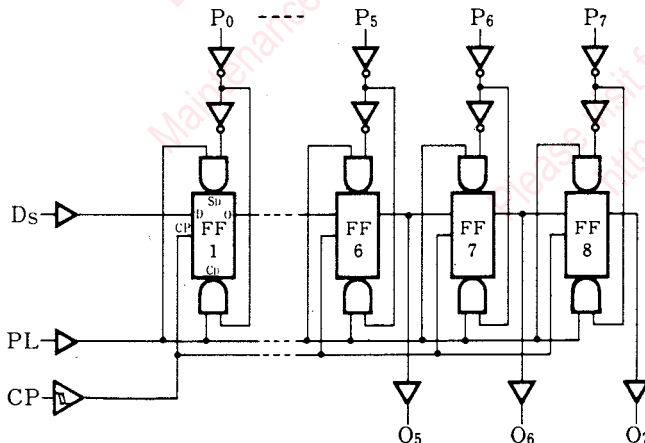
n	Input			Output		
	CP	D <sub>s</sub>	PL	O <sub>s</sub>	O <sub>6</sub>	O <sub>7</sub>
1		D <sub>1</sub>	L	×	×	×
2		D <sub>2</sub>	L	×	×	×
3		D <sub>3</sub>	L	×	×	×
6		×	L	D <sub>1</sub>	×	×
7		×	L	D <sub>2</sub>	D <sub>1</sub>	×
8		×	L	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>
		×	L	no change		

#### Parallel operation

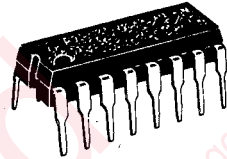
n	Input			Output		
	CP	D <sub>s</sub>	PL	O <sub>s</sub>	O <sub>6</sub>	O <sub>7</sub>
	×	×	H	P <sub>5</sub>	P <sub>6</sub>	P <sub>7</sub>

Note) × : don't care  
 D<sub>n</sub> : H or L  
 n : Number of clock pulse

### Logic Diagram



P-3



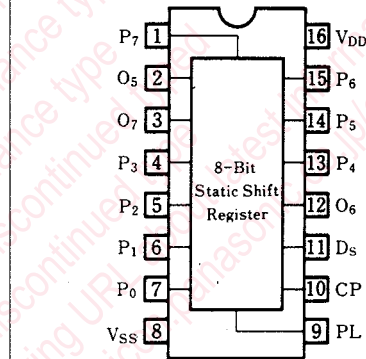
16-pin plastic DIL package

P-4



16-pin PANAFLAT package (SO-16D)

### Pin Configuration



■ Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply voltage	V <sub>DD</sub>	-0.5~+18	V
Input voltage	V <sub>I</sub>	-0.5~V <sub>DD</sub> +0.5*	V
Output pin voltage	V <sub>O</sub>	-0.5~V <sub>DD</sub> +0.5*	V
Peak input · output pin current	±I <sub>I</sub>	max. 10	mA
Power dissipation (per package)	Ta=-40~+60°C	max. 400	mW
	Ta=+60~+80°C	Decrease to 200mW at the rate of 8mW/°C	
Power dissipation (per output pin)	P <sub>D</sub>	max. 100	mW
Operating ambient temperature	T <sub>opr</sub>	-40~+85	°C
Storage temperature	T <sub>stg</sub>	-65~+150	°C

\* V<sub>DD</sub>+0.5V should be lower than 18V.

■ DC Characteristics (V<sub>SS</sub>=0V)

Item	V <sub>DD</sub> (V)	Symbol	Condition	Ta=-40°C		Ta=25°C		Ta=85°C		Unit
				min.	max.	min.	max.	min.	max.	
Static supply current	5	I <sub>DD</sub>	V <sub>I</sub> =V <sub>SS</sub> or V <sub>DD</sub>	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output voltage low level	5	V <sub>OL</sub>	V <sub>I</sub> =V <sub>SS</sub> or V <sub>DD</sub>  I <sub>O</sub>  <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output voltage high level	5	V <sub>OH</sub>	V <sub>I</sub> =V <sub>SS</sub> or V <sub>DD</sub>  I <sub>O</sub>  <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input voltage low level	5	V <sub>IL</sub>	I <sub>O</sub>  <1μA V <sub>O</sub> =0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			—	3	—	3	—	3	
	15			—	4	—	4	—	4	
Input voltage high level	5	V <sub>IH</sub>	I <sub>O</sub>  <1μA V <sub>O</sub> =0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			7	—	7	—	7	—	
	15			11	—	11	—	11	—	
Output current low level	5	I <sub>OL</sub>	V <sub>O</sub> =0.4V, V <sub>I</sub> =0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10			1.3	—	1.1	—	0.9	—	
	15			3.6	—	3	—	2.4	—	
Output current high level	5	-I <sub>OH</sub>	V <sub>O</sub> =4.6V, V <sub>I</sub> =0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10			1.3	—	1.1	—	0.9	—	
	15			3.6	—	3	—	2.4	—	
Output current high level	5	-I <sub>OH</sub>	V <sub>O</sub> =2.5V, V <sub>I</sub> =0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input leakage current	15	±I <sub>I</sub>	V <sub>I</sub> =0 or 15V	—	0.3	—	0.3	—	1	μA

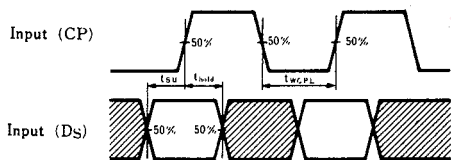
■ Switching Characteristics (Ta=25°C, V<sub>SS</sub>=0V, C<sub>L</sub>=50pF)

Item	V <sub>DD</sub> (V)	Symbol	min.	typ.	max.	Unit
Output rise time	5	t <sub>TLH</sub>	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output fall time	5	t <sub>THL</sub>	—	60	180	ns
	10		—	30	90	
	15		—	20	60	

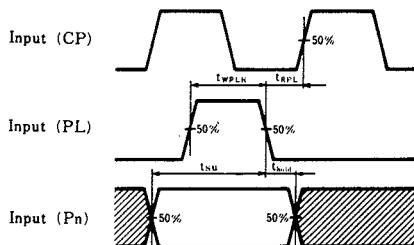
■ Switching Characteristics (cont.)

Item	V <sub>DD</sub> (V)	Symbol	min.	typ.	max.	Unit
Propagation time CP→On (H→L)	5	t <sub>PHL</sub>	—	170	510	ns
	10		—	65	195	
	15		—	45	135	
Propagation time CP→On (L→H)	5	t <sub>PLH</sub>	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Propagation time PL→On (H→L)	5	t <sub>PHL</sub>	—	240	720	ns
	10		—	90	270	
	15		—	60	180	
Propagation time PL→On (L→H)	5	t <sub>PLH</sub>	—	175	525	ns
	10		—	70	210	
	15		—	50	150	
Set-up time D <sub>S</sub> →CP	5	t <sub>su</sub>	—	45	135	ns
	10		—	15	45	
	15		—	10	30	
Set-up time P <sub>n</sub> →PL	5	t <sub>su</sub>	—	70	210	ns
	10		—	25	75	
	15		—	20	60	
Hold time D <sub>S</sub> →CP	5	t <sub>hold</sub>	—	20	60	ns
	10		—	10	30	
	15		—	8	24	
Hold time P <sub>n</sub> →PL	5	t <sub>hold</sub>	—	-10	24	ns
	10		—	0	24	
	15		—	0	24	
Minimum clock pulse width	5	t <sub>WCPL</sub>	—	55	165	ns
	10		—	20	60	
	15		—	15	45	
Minimum PL pulse width	5	t <sub>WPLH</sub>	—	75	225	ns
	10		—	25	75	
	15		—	20	60	
PL recovery time	5	t <sub>RPL</sub>	—	65	195	ns
	10		—	20	60	
	15		—	15	45	
Maximum clock frequency	5	f <sub>max</sub>	4	9	—	MHz
	10		12	25	—	
	15		18	37	—	
Input capacitance		C <sub>I</sub>	—	—	7.5	pF

● Switching waveforms



Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D<sub>S</sub>.



Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P<sub>n</sub> to PL. Set-up and hold times are shown as positive values but may be specified as negative values.

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