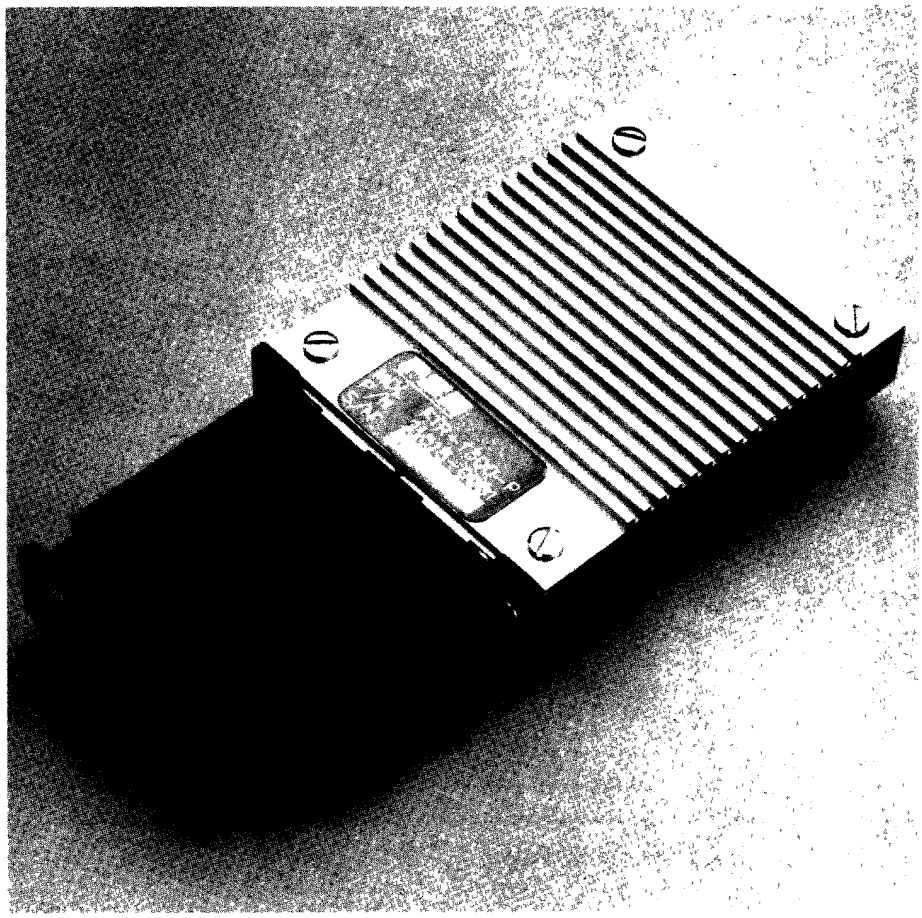
FDDI Transceiver

PRELIMINARY

T-41.91

FTR-1300-P
Enhanced FDDI Transceiver

Features



- ❑ FDDI Conforming
- ❑ Completely Compatible With The Motorola MC68000 Series FDDI IC Chip Set
- ❑ Designed to Interface With Commercial Chip Set or Semi-Custom/Gate Array FDDI Implementations
- ❑ Electrical Signal Interface
  - Parallel 25 MHz TTL Symbol Wide Data
  - TTL Clock, Control, and Status Lines
- ❑ Integral High Speed Timing Recovery
  - Optimized For 25 MHz Symbol Clock Rate
  - Supports FDDI-I or FDDI-II Operation
  - 60 to 160 MBaud Serial Data Rate Operation, OEM Selectable
  - Optional Serial Bit Clock and Data Outputs
- ❑ Standard +5 Volt and −5.2 Volt Power Supplies
- ❑ Sturdy Package With Integral FDDI MIC Receptacle
- ❑ Integral Phase Lock Loop Clock Recovery and Status Output
- ❑ Signal Detect Status Output
- ❑ Integral NRZI Encoding/ Decoding
- ❑ Transmit Disable Control
- ❑ Integral Parallel to Serial and Serial to Parallel Conversion

Description

The Enhanced FDDI Transceiver (FTR-1300-P) provides a fully compliant Fiber Distributed Data Interface (FDDI) optical interface which may be accessed by convenient symbol-wide (5 bit) parallel TTL data and clock signals. All high speed line rate (125 Mbaud for FDDI) interconnections are performed within the FTR-1300-P module, thereby relieving the user from the necessity of conforming to ECL design rules. The 5 bit transmit and receive parallel data interfaces are ideal for transferring the 4B/5B encoded symbols required for FDDI and limit the external clock rate to 25 MHz.

The FTR-1300-P may be used with commercial chip sets or semicustom logic to implement an FDDI node or used as a versatile building block in a variety of point-to-point fiber optic data transmission applications.

The PCO Enhanced FDDI Transceiver, Model FTR-1300-P, is completely compatible with the Motorola MC68000 series FDDI IC Chip Set. There is a direct electrical interface between the two products. For more information on Motorola's Chip Set, contact Motorola directly.

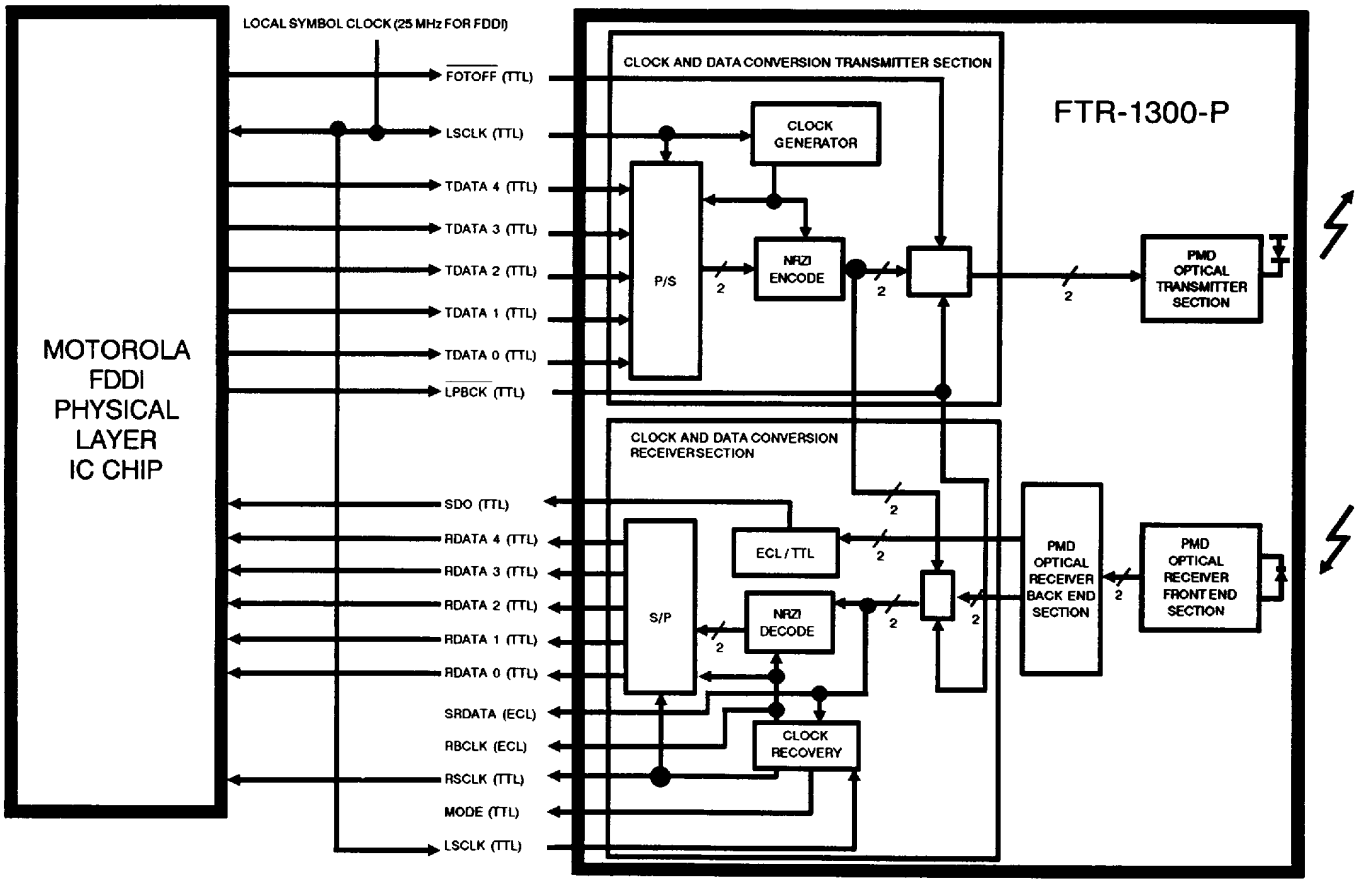
"Enhanced" Transceiver Benefits

PRELIMINARY

- Completely Compatible With Motorola MC68000 Series FDDI IC Chip Set
  - Direct Electrical Interface
  - For More Information On Motorola's Chip Set, Contact Motorola Directly.
- Integral 125 MHz Bit Clock Recovery:
  - Proven Operation At 125 MHz Can Support FDDI-I and FDDI-II
  - No Customer Timing Recovery Design Required
- Parallel 25 MBaud TTL Symbol Interface
  - No ECL Design Required
  - No Analog Design Required
  - Maximum Customer Design Flexibility
  - Allows Custom, Gate-Array, Or Commercial IC PHY Designs

Circuit Operation

FTR-1300-P Functional Block Diagram and Electrical Interface to Motorola MC68000 Series FDDI IC Chip Set



Transmitter Section Operation

The Transmitter Section accepts a 5 bit parallel input on the rising edge of an externally applied TTL clock (LSCLK1). The TTL clock drives an internal 5X frequency multiplier to generate a synchronized high speed clock which is used to perform a parallel to serial conversion on the input data. The high speed serial data is converted to NRZI (Non-Return to Zero, Invert on Ones), which is applied to a high speed driver circuit which controls the light emitting diode (LED). The LED emits optical radiation at nominal 1300 nanometer wavelength with parameters which conform to the FDDI Physical Layer Medium Dependent (PMD) requirements. A TTL control signal is available to disable the LED independently of the state of the parallel inputs.

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Receiver Section Operation

The Receiver Section converts the high speed optical signal (60 to 160 Mbaud) to an electrical signal and extracts the high frequency clock from the serial data. The high frequency clock is used to perform NRZI to NRZ code conversion and to return the serial data to parallel format. The high speed clock is divided by 5 and the parallel TTL data is output in 5 bit parallel form on the edge of the recovered TTL clock. The parallel output data is not aligned to symbol boundaries, i.e. in general it will consist of bits from two transmitted symbols. An external 5B/4B decoder circuit must establish symbol alignment. The optical interface conforms to the FDDI PMD requirements, including a TTL level Signal Detect indication (SDO) that the optical signal is within specifications. In addition, a TTL level signal (MODE) indicates that the phase lock loop clock recovery circuit is synchronized to the optical signal. An additional control signal ($\overline{\text{LPBACK}}$) causes the high speed NRZI output of the Transmitter Section to replace the recovered optical signal at the Receiver Section for diagnostic purposes.

Receiver Phase Lock Loop

The Receiver Section utilizes phase lock loop techniques to recover the high speed clock from the serial data. When no data is available (indicated by a logic LOW on the signal detect "SDO" pin), the PLL is locked to five times the LSCLK2 reference frequency. When serial data from the optical receiver is available (SDO goes HIGH), the PLL will acquire lock within 1 microsecond if the frequency of the optical signal is within $\pm 0.5\%$ of 5X LSCLK2. When lock is acquired the MODE signal will go to a logic HIGH level. If the frequency error between the optical data and LSCLK2 exceeds $\pm 1\%$ at any time after lock is acquired, MODE will go to the LOW state, the PLL will lock to 5X LSCLK2, and the PLL will attempt to relock to the serial input data.

Packaging And Media Interface Connector

The Enhanced FDDI Transceiver is housed in a rugged metal enclosure with excellent heat dissipation capability. The optical interface mates with the FDDI Media Interface Connector (MIC) to provide a duplex connection to the optical emitter and detector. The electrical footprint corresponds to that of two 20 pin dual-in-line patterns (.400 inch pitch).

Transmitter Performance (PMD Section)*

Optical Interface	Symbol	Minimum	Typ.	Max	Units
Data Rate	B	60	125	160	Mb/s
Optical Output Power	$\bar{P}_O$	−18.5	–	−14.0	dBm
Center Wavelength	λ_c	1270	–	1380	nm
Rise Time (10% to 90%)	t_r	0.6	–	3.5	ns
Fall Time (90% to 10%)	t_f	0.6	–	3.5	ns
Random Jitter (P-P)	RJ	0.0	–	0.76	ns
Duty Cycle Distortion (P-P)	DCD	0.0	–	1.0	ns
Data Dependent Jitter (P-P)	DDJ	0.0	–	0.6	ns
Extinction Ratio (pl/ph) x 100%	–	–	–	10	%
Transmit Disable Power	P_{off}	–	–	−45.0	dBm
LED Display Delay Time	$t_{disable}$	–	–	1	µs
Spectral Width	–	–	–	165	nm
Operating Temperature Range	T	0	–	+70	°C

* Beginning of Life Performance over the operating temperature range.

Receiver Performance (PMD Section)*

PRELIMINARY

Optical Interface		Symbol	Minimum	Typ.	Max	Units
Data Rate		B	60	125	160	Mb/s
Input Power (2.5×10^{-10} BER)[1]		$\bar{P}_{in}$	−31.0	–	−14.0	dBm
Signal Detect Thresholds	Assertion	$\bar{P}_{sd}$	–	–	−31.0	dBm
	Deassertion		−45.0	–	–	
Signal Detect Hysteresis		–	1.5	–	–	dB
Signal Detect Timing	Assertion	t_{sd}	–	–	100	µs
	Deassertion		–	–	350	
Operating Temperature Range		T	0	–	+70	°C
Wavelength of Operation		–	1100	1320	1600	nm

* Beginning of Life Performance over the operating temperature range.

Notes: 1. The receiver sensitivity is optimized for 125 Mb/s operation. Some loss of sensitivity may occur at higher and lower bit rates.

Electrical Interface Characteristics

Parameter	Symbol	Minimum	Typ.	Max	Units
Supply Voltage	V_{EE}	−5.5	−5.2	−4.9	V
	V_{CC}	4.75	5.0	5.25	V
Supply Current	I_{EE}	–	520	–	mA
	I_{CC}	–	140	–	mA
Power Dissipation	P	–	3.5	–	W

Electrical Characteristics

Parameter	Min	Max	Unit
High Level Input Voltage	2.0	V_{CC}	Volts
Low Level Input Voltage	0	0.8	Volts
High Level Input Current	–	0.02	mA
Low Level Input Current	–	−0.1	mA
Output High Voltage	2.4	–	Volts
Output Low Voltage (I_{sink} = 4 mA)	–	0.5	Volts

Pin Out Diagram

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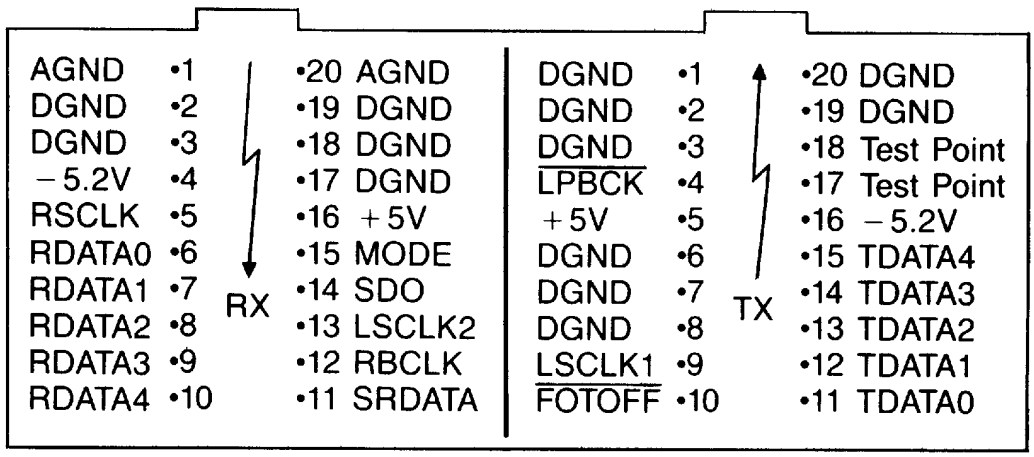

TOP VIEW

Transmitter Section Pin Description

PIN	NAME	FUNCTION
11 12 13 14 15	TDATA0 TDATA1 TDATA2 TDATA3 TDATA4	Parallel TTL symbol data to Transmitter Section. All 5 bits are clocked in simultaneously on the rising edge of LSCLK1. Data is shifted out serially in the order TDATA4 first to TDATA0 last.
9	LSCLK1	TTL symbol clock. The rising edge enters TDATA4-0 into the Transmitter Section. This clock provides the reference frequency for the Transmitter Section 5X clock multiplier function.
10	$\overline{\text{FOTOFF}}$	TTL control signal which disables the optical transmitter when at a logic LOW level; when disabled the transmit LED is OFF, emitting little or no optical energy (less than −45 dBm).
4	$\overline{\text{LPBACK}}$	TTL control signal which implements the loopback function when at a logic LOW level. When the loopback function is enabled, serial data from the Transmit Section replaces the input from the optical receiver at the Receiver Section. When $\overline{\text{LPBACK}}$ is activated, the optical output of the Transmit Section is enabled unless explicitly disabled by $\overline{\text{FOTOFF}}$.

Receiver Section Pin Description

PIN	NAME	FUNCTION
6 7 8 9 10	RDATA0 RDATA1 RDATA2 RDATA3 RDATA4	Parallel TTL symbol data output from the Receiver Section. Data output is synchronized with RSCLK such that 5 bits are output on rising edge of RSCLK. RDATA4 corresponds to the first serial bit received and RDATA0 to the fifth.
5	RSCLK	Recovered symbol clock at one fifth the serial data rate. See Table 2 for interpreting the clock source.
14	SDO	TTL status output which indicates that the optical input signal to the Receiver Section meets the Signal Detect indicator performance requirements of the FDDI PMD. A logic HIGH indicates normal operation and a logic LOW indicates insufficient optical input signal. SDO is output on the rising edge of LSCLK2. See Table 2.
15	MODE	TTL status output which indicates by a logic HIGH level that the Receiver Section phase lock loop is locked to the incoming optical signal. See Table 2.
13	LSCLK2	TTL reference clock for the Receive Section phase lock loop at one fifth the serial data rate. Normally tied to LSCLK1 of the Transmitter Section.
12	RBCLK	Recovered high speed clock at the serial data rate. The signal level is standard 10K ECL.
11	SRDATA	Recovered high speed serial data aligned with RBCLK. Signal level is standard 10K ECL.

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Dimensions

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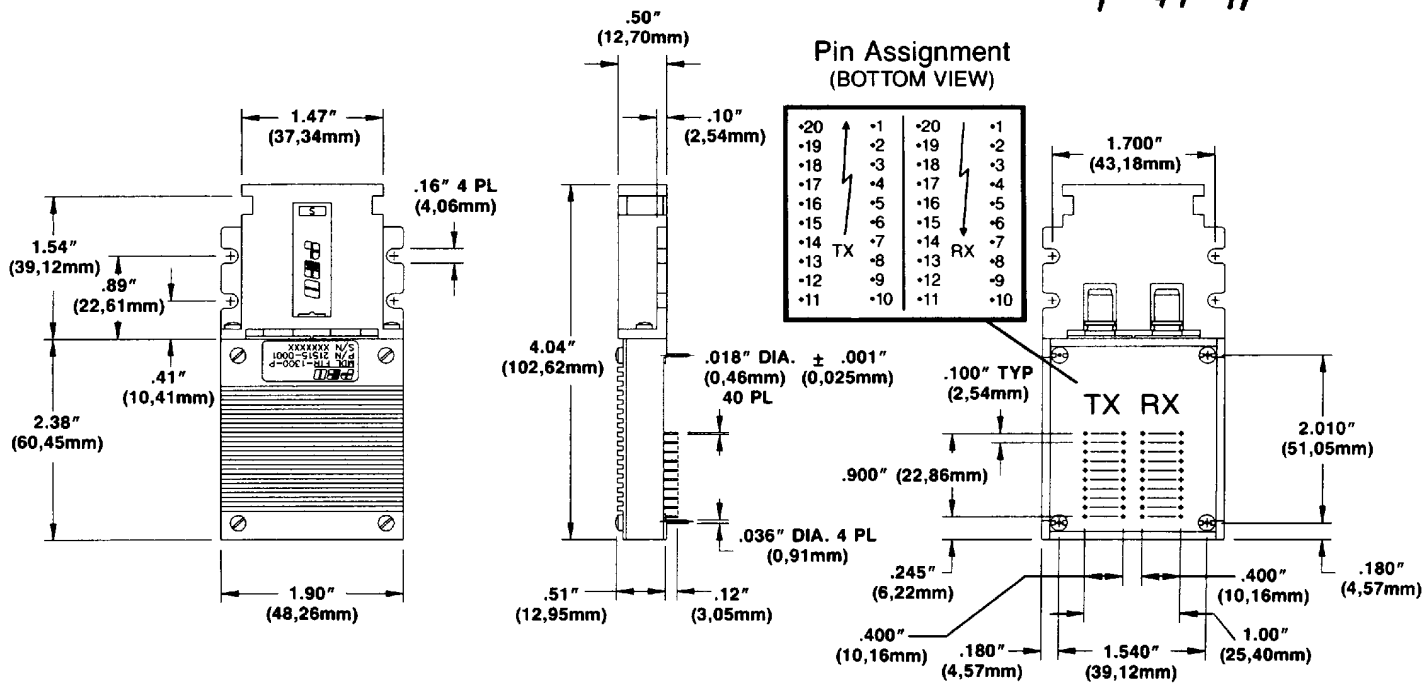

Transmitter Function

Control Inputs (TTL)		FUNCTION	LED
$\overline{\text{FOTOFF}}$	$\overline{\text{LPBCK}}$		
1	1	Normal Operation	Coded Data
0	1	Fiber Optic Transmitter Disabled	Off
1	0	Loopback Mode	Coded Data
0	0	Loopback Mode	Off

TABLE 1.

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Receiver Function

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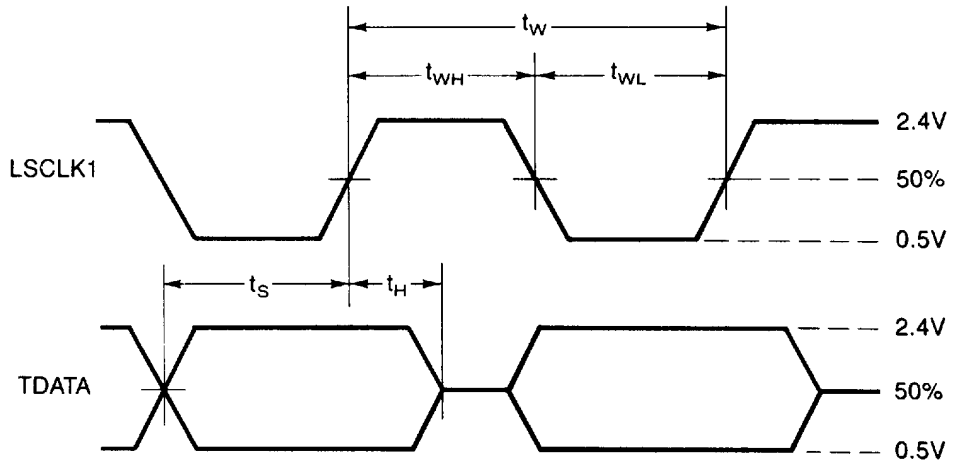
Optical Signal Level	Control Input $\overline{\text{LPBCK}}$	Function	SRDATA (ECL)	RDATAn (TTL)	SDO (TTL)	MODE (TTL)
Above Threshold	1	Normal Operation	Serial Data from Optical Input	Parallel Data from Optical Input	1	1 = Locked 0 = Unlocked
Below Threshold	1	Fiber Optic Receive Disabled	Forced to Logic 0	Forced to Logic 0	0	0
Doesn't Matter	0	Loopback Mode	Loop Back Data	Parallel Data From Loopback	1	1 = Locked 0 = Unlocked

TABLE 2.

Transmitter Timing



Symbol	Parameter	Min. (ns)	Typ. (ns)	Max. (ns)
t_W	LSCLK1 Period	33	40	100
t_{WH}	LSCLK1 High Time	15	—	—
t_{WL}	LSCLK1 Low Time	15	—	—
t_S	TDATA Setup Time	12	—	—
t_H	TDATA Hold Time	0	—	—

TRANSMITTER TIMING

FIG. 1

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Receiver Timing

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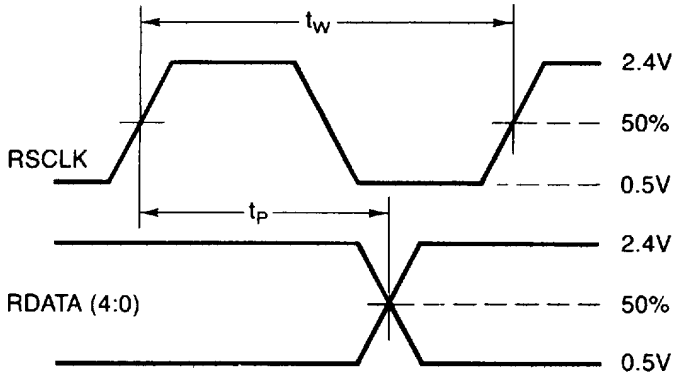
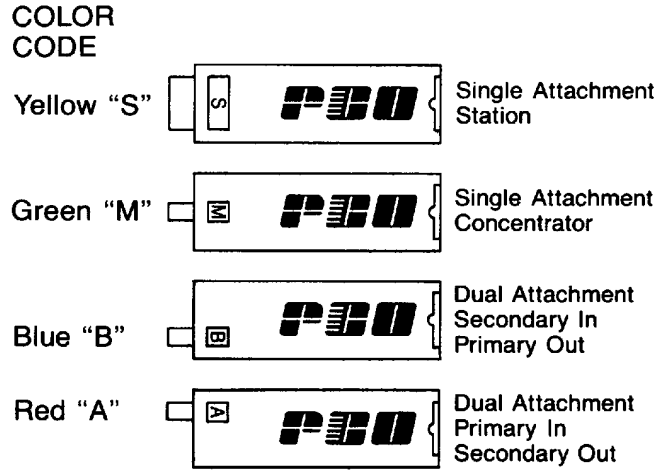


Symbol	Parameter	Min. (ns)	Typ. (ns)	Max. (ns)
t_W	RSCLK Period	33	40	100
t_P	Propagation Delay	15	—	20

RECEIVER TIMING
FIG. 2

MIC Receptacle Keying Information-Exclusive PCO MICkey™ System

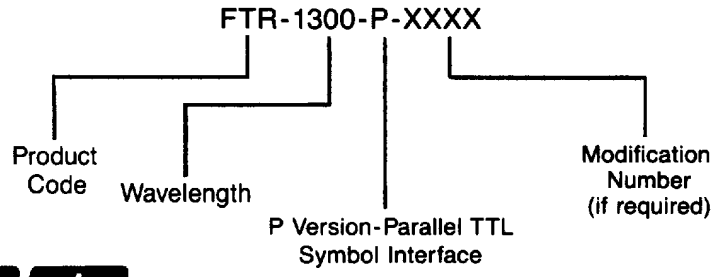
The PCO MICkey™ System offers the flexibility of a keying approach which may be set or changed in the field, or at your facility. Each MICkey insert fits into PCO's common FDDI transceiver configuration, and may be quickly snapped into place, or extracted, as a final step to configure to any specific application or installation. The four FDDI required MICkey inserts are provided with each PCO FDDI transceiver. They may be installed at the PCO factory according to your specifications, or you may install them yourself. The MICkey inserts are also available separately. Call your local PCO technical representative for complete information.



Complementary FDDI Components

The PCO Enhanced FDDI Transceiver, Model FTR-1300-P, is completely compatible with the Motorola MC68000 Series FDDI IC Chip Set. There is a direct electrical interface between the two products. For more information on Motorola's Chip Set contact Motorola directly.

Ordering Information



For further information, contact your local PCO technical representative.

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