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April 1st, 2010
Renesas Electronics Corporation

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MOS INTEGRATED CIRCUIT

78011F, 78012F, 78013F, 78014F, 78015F, 78016F, 78018F

8-BIT SINGLE-CHIP MICROCONTROLLER

Phase-out/Discontinued

★ DESCRIPTION

The μ PD78011F, 78012F, 78013F, 78014F, 78015F, 78016F, and 78018F are the products in the μ PD78018F subseries within the 78K/0 series.

Compared with the older μ PD78014 subseries, this subseries operates at lower voltage and provides a fuller set of ROM and RAM variations.

A one-time PROM or EPROM product μ PD78P018F capable of operating in the same power supply voltage range as of the mask ROM product and other development tools are also provided.

Functions are described in detail in the following User's Manual, which should be read when carrying out design work.

μ PD78018F, 78018FY Subseries User's Manual : U10659E
78K/0 Series Users Manual – Instruction : U12326E

FEATURES

- Large on-chip ROM & RAM

Item Product Name	Program Memory (ROM)	Data Memory			Package
		Internal High-Speed RAM	Internal Expanded RAM	Buffer RAM	
μ PD78011F	8K bytes	512 bytes	–	32 bytes	<ul style="list-style-type: none"> • 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic LQFP (12 × 12 mm)
μ PD78012F	16K bytes				
μ PD78013F	24K bytes		1024 bytes		
μ PD78014F	32K bytes				
μ PD78015F	40K bytes	512 bytes			
μ PD78016F	48K bytes				
★ μ PD78018F	60K bytes		1024 bytes		

- External memory expansion space : 64K bytes
- Minimum instruction execution time can be varied from high-speed (0.4 μ s) to ultra-low-speed (122 μ s)
- I/O ports: 53 (N-ch open-drain : 4)
- 8-bit resolution A/D converter : 8 channels
- Serial interface : 2 channels
- Timer : 5 channels
- Supply voltage : $V_{DD} = 1.8$ to 5.5 V

APPLICATION FIELDS

Cellular phone, pager, VCR, audio, camera, home appliances, etc

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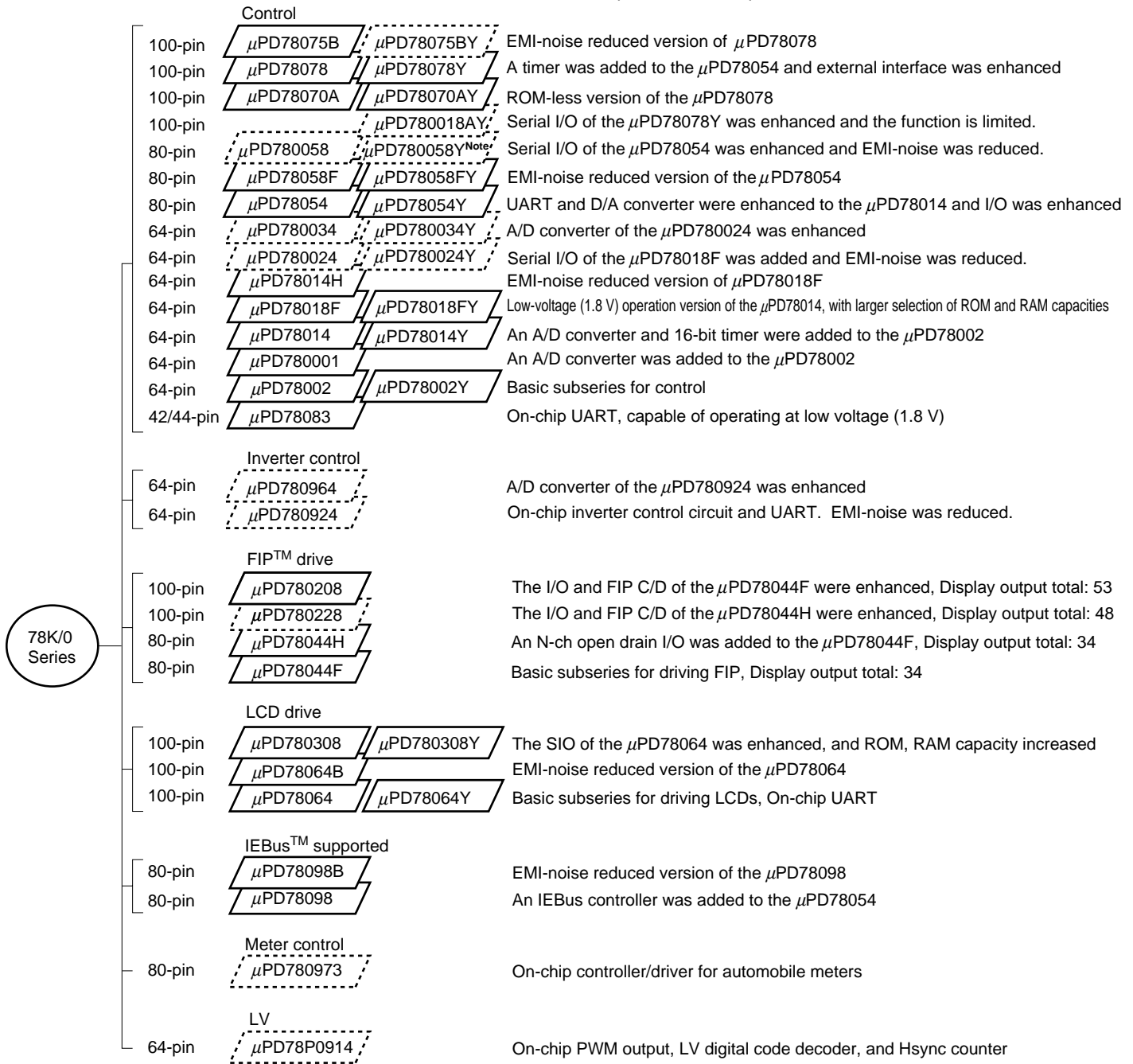
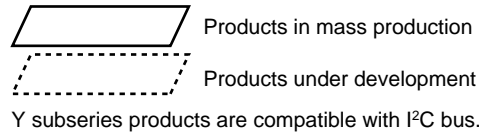
ORDERING INFORMATION

Part Number	Package
μPD78011FCW-xxx	64-pin plastic shrink DIP (750 mil)
μPD78011FGC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78011FGK-xxx-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD78012FCW-xxx	64-pin plastic shrink DIP (750 mil)
μPD78012FGC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78012FGK-xxx-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD78013FCW-xxx	64-pin plastic shrink DIP (750 mil)
μPD78013FGC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78013FGK-xxx-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD78014FCW-xxx	64-pin plastic shrink DIP (750 mil)
μPD78014FGC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78014FGK-xxx-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD78015FCW-xxx	64-pin plastic shrink DIP (750 mil)
μPD78015FGC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78015FGK-xxx-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD78016FCW-xxx	64-pin plastic shrink DIP (750 mil)
μPD78016FGC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78016FGK-xxx-8A8	64-pin plastic LQFP (12 × 12 mm)
★ μPD78018FCW-xxx	64-pin plastic shrink DIP (750 mil)
★ μPD78018FGC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)
★ μPD78018FGK-xxx-8A8	64-pin plastic LQFP (12 × 12 mm)

Remark xxx indicates a ROM code suffix.

★ 78K/0 SERIES DEVELOPMENT

The following shows the products organized according to usage. The names in the parallelograms are subseries names.



Note Under planning

The following lists the main functional differences between subseries products.

Subseries Name	Function	ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V _{DD} MIN. Value	External Expansion										
			8-bit	16-bit	Watch	WDT																	
Control	μPD78075B	32K-40K	4ch	1ch	1ch	1ch	8ch	-	2ch	3ch (UART: 1ch)	88	1.8 V	○										
	μPD78078	48K-60K									61	2.7 V											
	μPD78070A	-																					
	μPD780058	24K-60K	2ch						2ch	3ch (time division UART: 1ch)	68	1.8 V											
	μPD78058F	48K-60K								3ch (UART: 1ch)	69	2.7 V											
	μPD78054	16K-60K							2.0 V														
	μPD780034	8K-32K							-	8ch	-	3ch (UART: 1ch, time division 3-wire: 1ch)	51	1.8 V									
	μPD780024								8ch	-	2ch	53	1.8 V										
	μPD78014H											2.7 V											
	μPD78018F	8K-60K																					
	μPD78014	8K-32K																					
	μPD780001	8K																	-	-	1ch	39	-
	μPD78002	8K-16K																		1ch	-	53	○
	μPD78083												8ch		1ch (UART: 1ch)	33	1.8 V	-					
Inverter control	μPD780964	8K-32K							3ch	Note		1ch	-	8ch	-	2ch (UART: 2ch)	47	2.7 V	○				
	μPD780924												8ch	-									
FIP drive	μPD780208	32K-60K	2ch	1ch	1ch	1ch	8ch	-	-	2ch	74	2.7 V	-										
	μPD780228	48K-60K		3ch	-					-	1ch	72		4.5 V									
	μPD78044H	32K-48K	2ch	1ch	1ch					68	2.7 V												
	μPD78044F	16K-40K								2ch													
LCD drive	μPD780308	48K-60K	2ch	1ch	1ch	1ch	8ch	-	-	3ch (time division UART: 1ch)	57	2.0 V	-										
	μPD78064B	32K								2ch (UART: 1ch)													
	μPD78064	16K-32K																					
IEBus supported	μPD78098	40K-60K	2ch	1ch	1ch	1ch	8ch	-	2ch	3ch (UART: 1ch)	69	2.7 V	○										
	μPD78098B	32K-60K																					
Meter control	μPD780973	24K-32K	3ch	1ch	1ch	1ch	5ch	-	-	2ch (UART: 1ch)	56	4.5 V	-										
LV	μPD78P0914	32K	6ch	-	-	1ch	8ch	-	-	2ch	54	4.5 V	○										

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTION (1/2)

Item		Product Name						
		μPD78011F	μPD78012F	μPD78013F	μPD78014F	μPD78015F	μPD78016F	μPD78018F
Internal memory	ROM	8K bytes	16K bytes	24K bytes	32K bytes	40K bytes	48K bytes	60K bytes
	High-speed RAM	512 bytes			1024 bytes			
	Expanded RAM	—					512 bytes	1024 bytes
	Buffer RAM	32 bytes						
Memory space		64K bytes						
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)						
Minimum instruction execution time		On-chip minimum instruction execution time cycle modification function						
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (at 10.0 MHz operation)						
	When subsystem clock selected	122 μs (at 32.768 kHz operation)						
Instruction set		<ul style="list-style-type: none"> • 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc. 						
I/O ports		Total : 53 <ul style="list-style-type: none"> • CMOS input : 2 • CMOS I/O : 47 • N-channel open-drain I/O (15 V withstand voltage) : 4 						
A/D converter		<ul style="list-style-type: none"> • 8-bit resolution × 8 channels • Operable over a wide power supply voltage range: AV_{DD} = 1.8 to 5.5 V 						
Serial interface		<ul style="list-style-type: none"> • 3-wire serial I/O/SBI/2-wire serial I/O mode selectable: 1 channel • 3-wire mode (on-chip max. 32 bytes automatic data transmit/receive function): 1 channel 						
Timer		<ul style="list-style-type: none"> • 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel 						
Timer output		3 (14-bit PWM output × 1)						
Clock output		39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz (at main system clock: 10.0 MHz operation), 32.768 kHz (at subsystem clock: 32.768 kHz operation)						
Buzzer output		2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock: 10.0 MHz operation)						
Vectored interrupt sources	Maskable	Internal : 8 External : 4						
	Non-maskable	Internal : 1						
	Software	1						

Phase-out/Discontinued

OVERVIEW OF FUNCTION (2/2)

Product Name \ Item	μPD78011F	μPD78012F	μPD78013F	μPD78014F	μPD78015F	μPD78016F	μPD78018F
Test input	Internal : 1 External : 1						
Supply voltage	V _{DD} = 1.8 to 5.5 V						
Operating ambient temperature	T _A = -40 to +85°C						
Package	<ul style="list-style-type: none"> • 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic LQFP (12 × 12 mm) 						

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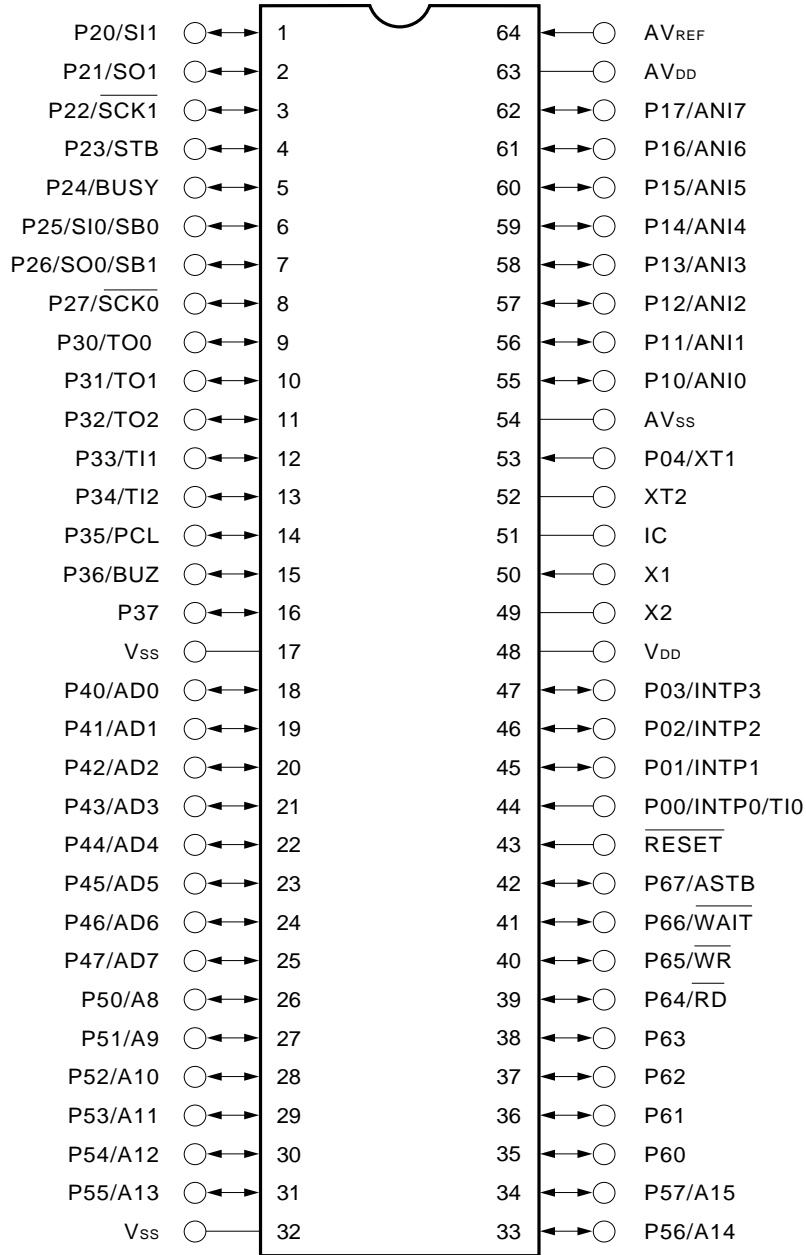
1. PIN CONFIGURATION (Top View)

• 64-Pin Plastic Shrink DIP (750 mil)

μPD78011FCW-xxx, 78012FCW-xxx, 78013FCW-xxx,

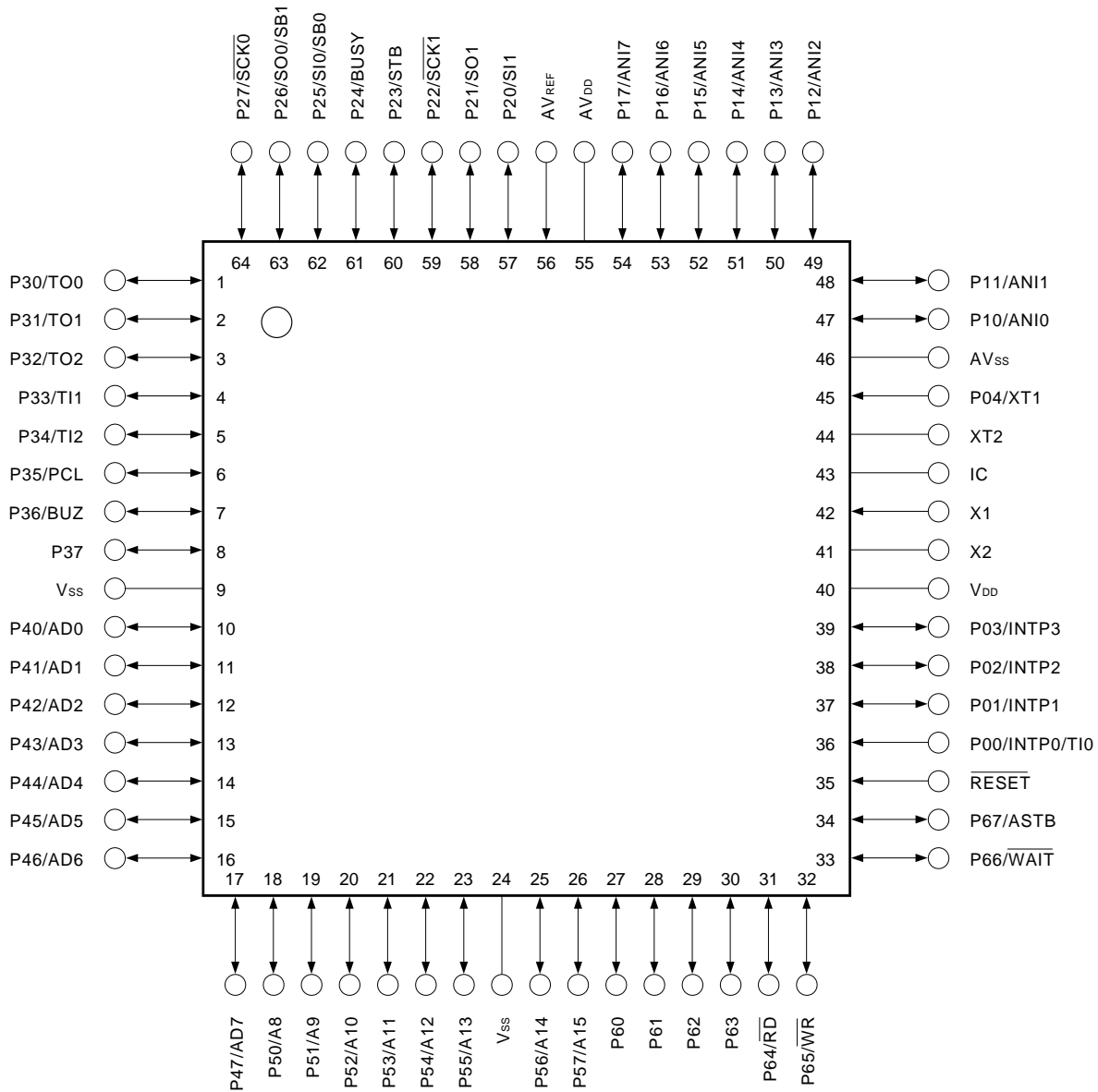
μPD78014FCW-xxx, 78015FCW-xxx, 78016FCW-xxx,

★ μPD78018FCW-xxx



- Cautions**
1. Always connect the IC (Internally Connected) pin to Vss directly.
 2. Always connect the AVDD pin to VDD.
 3. Always connect the AVss pin to Vss.

- 64-Pin Plastic QFP (14 × 14 mm)
 - μPD78011FGC-xxx-AB8, 78012FGC-xxx-AB8, 78013FGC-xxx-AB8,
 - μPD78014FGC-xxx-AB8, 78015FGC-xxx-AB8, 78016FGC-xxx-AB8,
- ★ μPD78018FGC-xxx-AB8
- 64-Pin Plastic LQFP (12 × 12 mm)
 - μPD78011FGK-xxx-8A8, 78012FGK-xxx-8A8, 78013FGK-xxx-8A8,
 - μPD78014FGK-xxx-8A8, 78015FGK-xxx-8A8, 78016FGK-xxx-8A8,
- ★ μPD78018FGK-xxx-8A8

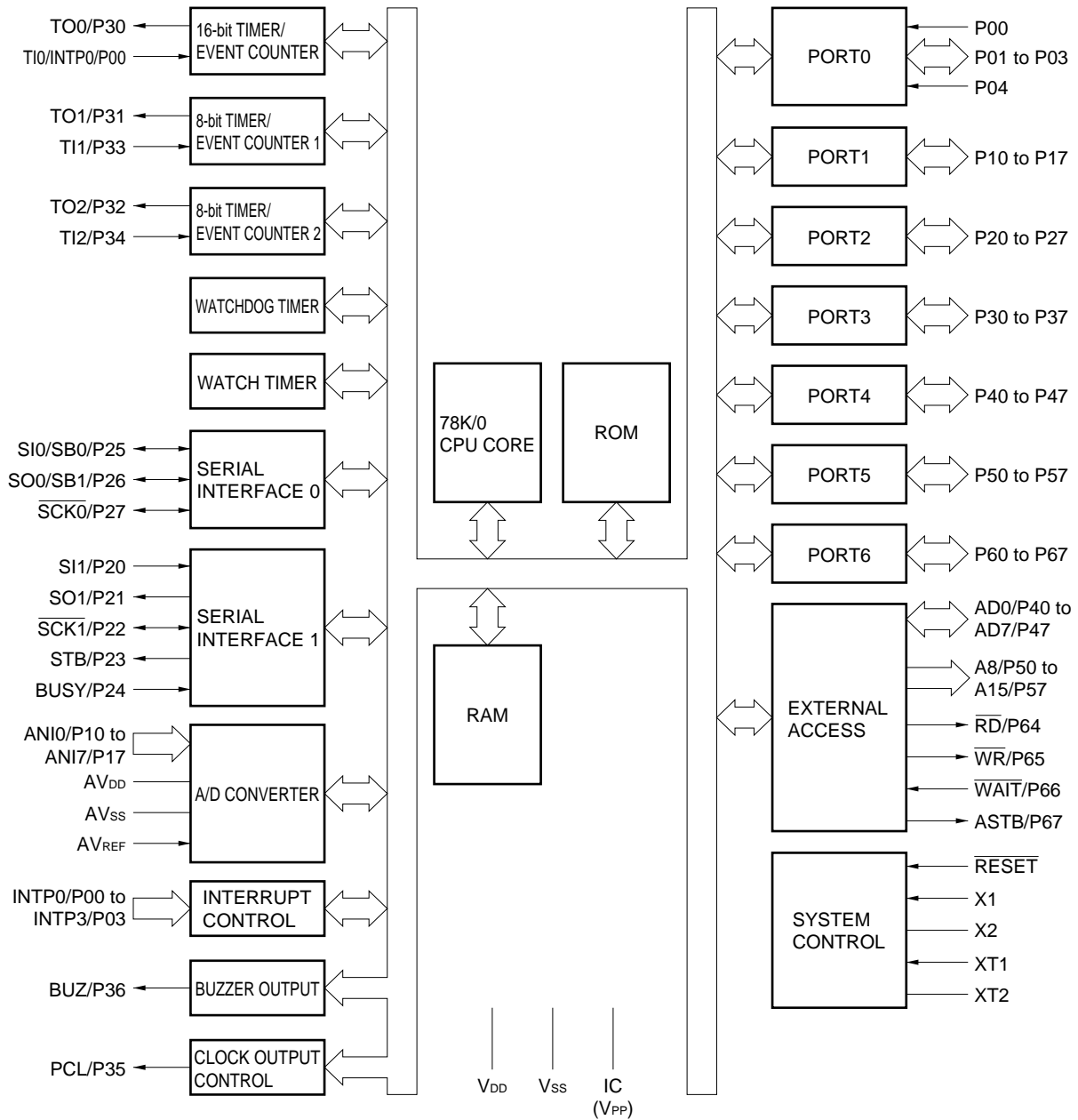


- Cautions**
1. Always connect the IC (Internally Connected) pin to Vss directly.
 2. Always connect the AVDD pin to VDD.
 3. Always connect the AVss pin to Vss.

Phase-out/Discontinued

A8 to A15	: Address Bus	PCL	: Programmable Clock
AD0 to AD7	: Address/Data Bus	\overline{RD}	: Read Strobe
ANI0 to ANI7	: Analog Input	\overline{RESET}	: Reset
ASTB	: Address Strobe	SB0, SB1	: Serial Bus
AVDD	: Analog Power Supply	$\overline{SCK0}, \overline{SCK1}$: Serial Clock
AVREF	: Analog Reference Voltage	SI0, SI1	: Serial Input
AVSS	: Analog Ground	SO0, SO1	: Serial Output
BUSY	: Busy	STB	: Strobe
BUZ	: Buzzer Clock	TI0 to TI2	: Timer Input
IC	: Internally Connected	TO0 to TO2	: Timer Output
INTP0 to INTP3	: Interrupt from Peripherals	VDD	: Power Supply
P00 to P04	: Port0	VSS	: Ground
P10 to P17	: Port1	\overline{WAIT}	: Wait
P20 to P27	: Port2	\overline{WR}	: Write Strobe
P30 to P37	: Port3	X1, X2	: Crystal (Main System Clock)
P40 to P47	: Port4	XT1, XT2	: Crystal (Subsystem Clock)
P50 to P57	: Port5		
P60 to P67	: Port6		

2. BLOCK DIAGRAM



- Remarks** 1. Internal ROM & RAM capacity varies depending on the product.
 2. () : μPD78P018F

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	I/O	Function		On Reset	Dual-Function Pin
P00	Input	Port 0 5-bit I/O port	Input only	Input	INTP0/TI0
P01	Input/ output		Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used in software.	Input	INTP1
P02					INTP2
P03					INTP3
P04 ^{Note 1}	Input		Input only	Input	XT1
P10 to P17	Input/ output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used in software. ^{Note 2}		Input	ANI0 to ANI7
P20	Input/ output	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used in software.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{\text{SCK0}}$
P30	Input/ output	Port 3 8-bit input/output port. Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistor can be used in software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40 to P47	Input/ output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit unit. When used as an input port, on-chip pull-up resistor can be used in software. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

- Notes 1.** When using the P04/XT1 pins as an input port, set 1 to bit 6 (FRC) of the processor clock control register (PCC). Do not use the on-chip feedback register of the subsystem clock oscillator.
- 2.** When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input, on-chip pull-up resistor is automatically unused.

3.1 PORT PINS (2/2)

Pin Name	I/O	Function		On Reset	Dual-Function Pin
P50 to P57	Input/output	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used in software.		Input	A8 to A15
P60	Input/output	Port 6 8-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.	Input	—
P61					
P62					
P63					
P64		When used as an input port, on-chip pull-up resistor can be used in software.	\overline{RD}		
P65			\overline{WR}		
P66			\overline{WAIT}		
P67			ASTB		

3.2 PINS OTHER THAN PORT PINS (1/2)

Pin Name	I/O	Function		On Reset	Dual-Function Pin
INTP0	Input	External interrupt request input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.		Input	P00/T10
INTP1					P01
INTP2		Falling edge detection external interrupt request input.			P02
INTP3					P03
SI0	Input	Serial interface serial data input.		Input	P25/SB0
SI1					P20
SO0	Output	Serial interface serial data output.		Input	P26/SB1
SO1					P21
SB0	Input/output	Serial interface serial data input/output.		Input	P25/SI0
SB1					P26/SO0
$\overline{SCK0}$	Input/output	Serial interface serial clock input/output.		Input	P27
$\overline{SCK1}$					P22
STB	Output	Serial interface automatic transmit/receive strobe output.		Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.		Input	P24

3.2 PINS OTHER THAN PORT PINS (2/2)

Pin Name	I/O	Function	On Reset	Dual-Function Pin
T10	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
T11		External count clock input to 8-bit timer (TM1).		P33
T12		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer (TM0) output (shared as 14-bit PWM output).	Input	P30
TO1		8-bit timer (TM1) output.		P31
TO2		8-bit timer (TM2) output.		P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
AD0 to AD7	Input /output	Low-order address/data bus at external memory expansion.	Input	P40 to P47
A8 to A15	Output	High-order address bus at external memory expansion.	Input	P50 to P57
\overline{RD}	Output	External memory read operation strobe signal output.	Input	P64
\overline{WR}		External memory write operation strobe signal output.		P65
\overline{WAIT}	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address information output at port 4 and port 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AVREF	Input	A/D converter reference voltage input.	—	—
AVDD	—	A/D converter analog power supply. Connected to V _{DD} .	—	—
AVSS	—	A/D converter ground potential. Connected to V _{SS} .	—	—
\overline{RESET}	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P04
XT2	—		—	—
V _{DD}	—	Positive power supply.	—	—
V _{SS}	—	Ground potential.	—	—
IC	—	Internal connection. Connected to V _{SS} directly.	—	—

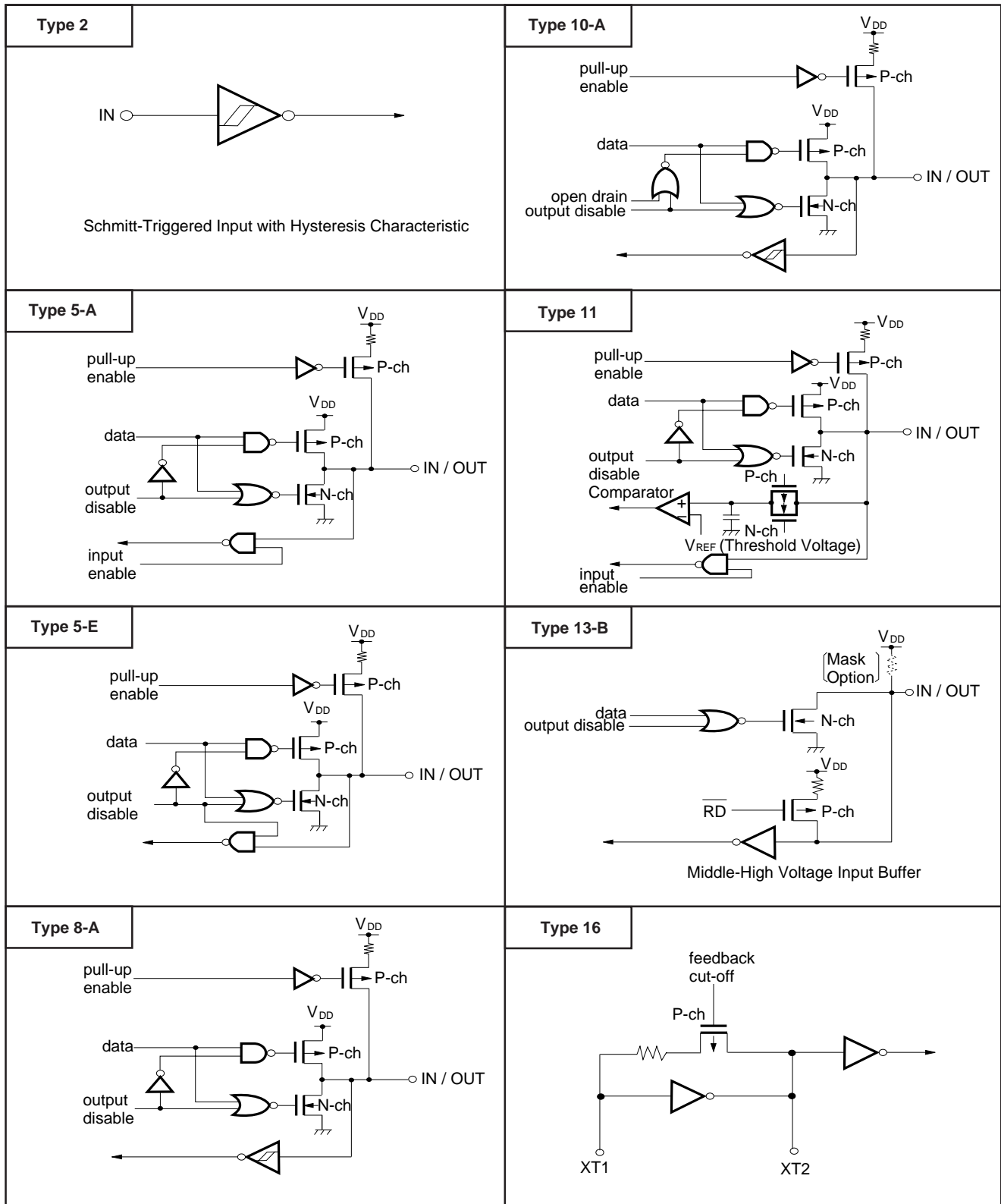
3.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, refer to **Figure 3-1**.

Table 3-1. Input/Output Circuit Type of Each Pin

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when Not Used	
P00/INTP0/TI0	2	Input	Connected to V _{SS} .	
P01/INTP1	8-A	Input/output	Individually connected to V _{SS} via resistor.	
P02/INTP2				
P03/INTP3				
P04/XT1	16	Input	Connected to V _{DD} or V _{SS} .	
P10/ANI0 to P17/ANI7	11	Input/output	Individually connected to V _{DD} or V _{SS} via resistor.	
P20/SI1	8-A			
P21/SO1	5-A			
P22/ $\overline{\text{SCK1}}$	8-A			
P23/STB	5-A			
P24/BUSY	8-A			
P25/SI0/SB0	10-A			
P26/SO0/SB1				
P27/ $\overline{\text{SCK0}}$				
P30/TO0	5-A			
P31/TO1				
P32/TO2				
P33/TI1	8-A			
P34/TI2				
P35/PCL	5-A			
P36/BUZ				
P37				
P40/AD0 to P47/AD7	5-E			Individually connected to V _{DD} via resistor.
P50/A8 to P57/A15	5-A			Individually connected to V _{DD} or V _{SS} via resistor.
P60 to P63	13-B			Individually connected to V _{DD} via resistor.
P64/ $\overline{\text{RD}}$	5-A			Individually connected to V _{DD} or V _{SS} via resistor.
P65/ $\overline{\text{WR}}$				
P66/ $\overline{\text{WAIT}}$				
P67/ASTB				
$\overline{\text{RESET}}$	2	Input	—	
XT2	16	—	Leave open.	
AV _{REF}	—	—	Connected to V _{SS} .	
AV _{DD}			Connected to V _{DD} .	
AV _{SS}			Connected to V _{SS} .	
IC			Connected to V _{SS} directly.	

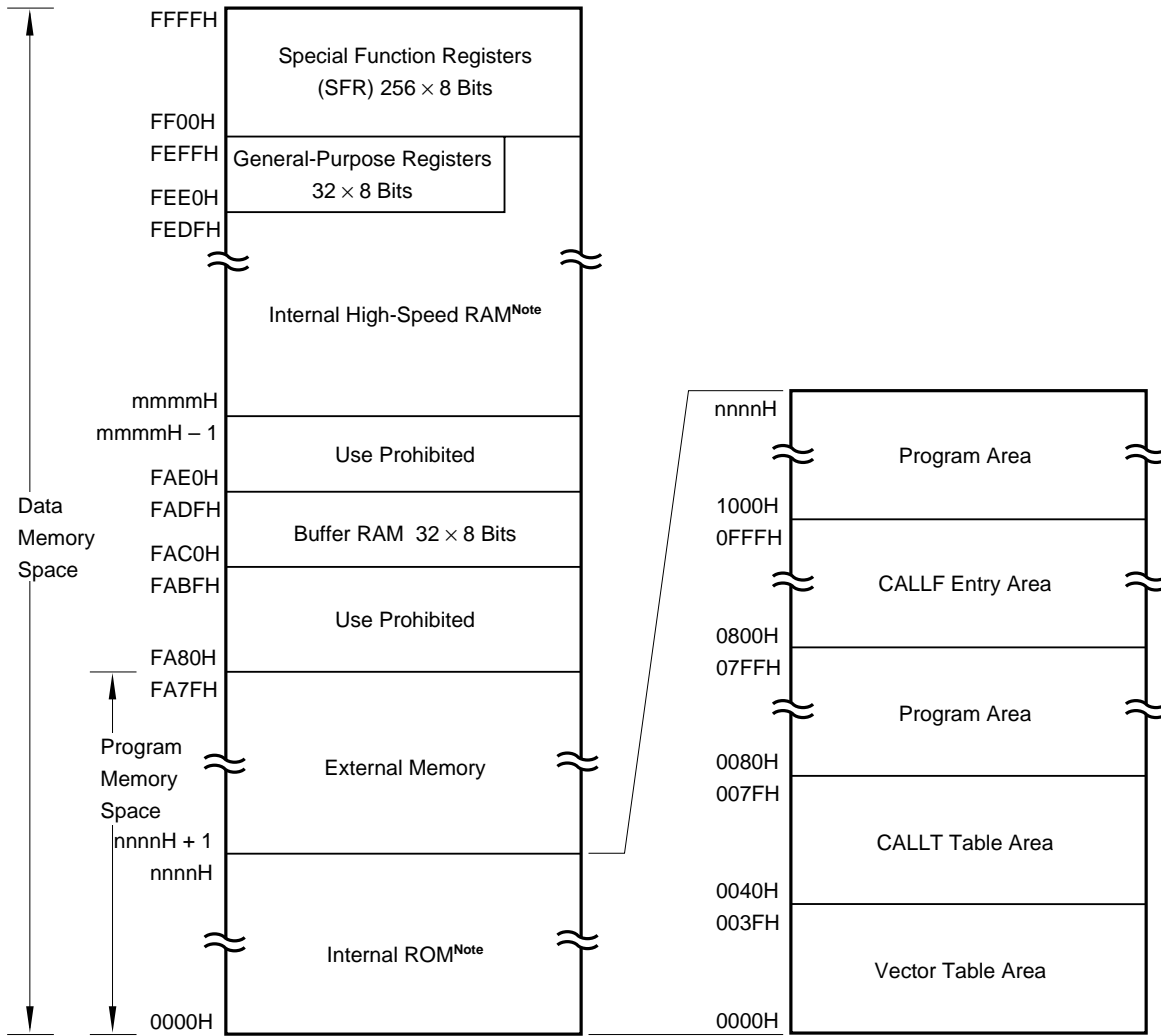
Figure 3-1. Pin Input/Output Circuits



★ 4. MEMORY SPACE

The memory maps of the μPD78011F, 78012F, 78013F, 78014F, 78015F, 78016F, and 78018F are shown in Figure 4-1 and 4-2.

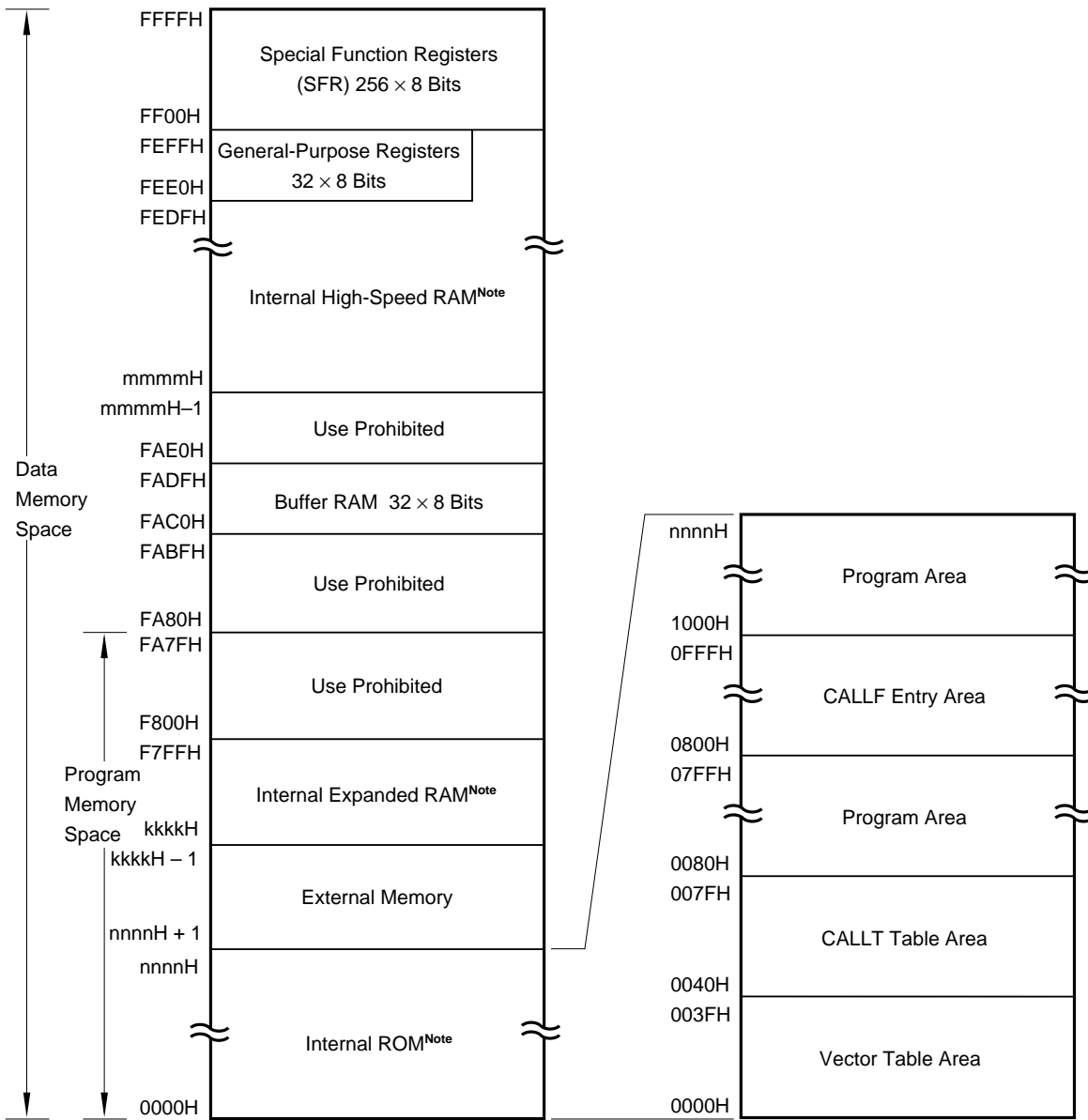
Figure 4-1. Memory Map (μPD78011F, 78012F, 78013F, 78014F)



Note Internal ROM and internal high-speed RAM capacities vary depending on the product (refer to the table below).

Product Name	Internal ROM End Address nnnnH	Internal High-Speed RAM Start Address mmmmH
μPD78011F	1FFFH	FD00H
μPD78012F	3FFFH	
μPD78013F	5FFFH	FB00H
μPD78014F	7FFFH	

Figure 4-2. Memory Map (μPD78015F, 78016F, 78018F)



Note Internal ROM, internal high-speed RAM, and internal expanded RAM capacities vary depending on the product (refer to the table below).

Product Name	Internal ROM End Address n n n n H	Internal High-Speed RAM Start Address m m m m H	Internal Expanded RAM Start Address k k k k H
μPD78015F	9FFFH	FB00H	F600H
μPD78016F	BFFFH		F400H
μPD78018F	EFFFH		

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 PORTS

The I/O port has the following three types

- CMOS input (P00, P04) : 2
 - CMOS input/output (P01 to P03, port 1 to port 5, P64 to P67) : 47
 - N-ch open-drain input/output(15V withstand voltage) (P60 to P63) : 4
-
- Total : 53

Table 5-1. Functions of Ports

Port Name	Pin Name	Function
Port 0	P00, P04	Dedicated Input port
	P01 to P03	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used in software.
Port 1	P10 to P17	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used in software.
Port 2	P20 to P27	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used in software.
Port 3	P30 to P37	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used in software.
Port 4	P40 to P47	Input/output ports. Input/output can be specified in 8-bit units. When used as an input port, pull-up resistor can be used in software. Test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used in software. LED can be driven directly.
Port 6	P60 to P63	N-ch open-drain input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.
	P64 to P67	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used in software.

5.2 CLOCK GENERATOR

There are two types of clock generator: main system clock and subsystem clock. The minimum instruction execution time can be changed.

- 0.4μs/0.8μs/1.6μs/3.2μs/6.4μs (Main system clock: at 10.0 MHz operation)
- 122μs (Subsystem clock: at 32.768 KHz operation)

Figure 5-1. Clock Generator Block Diagram

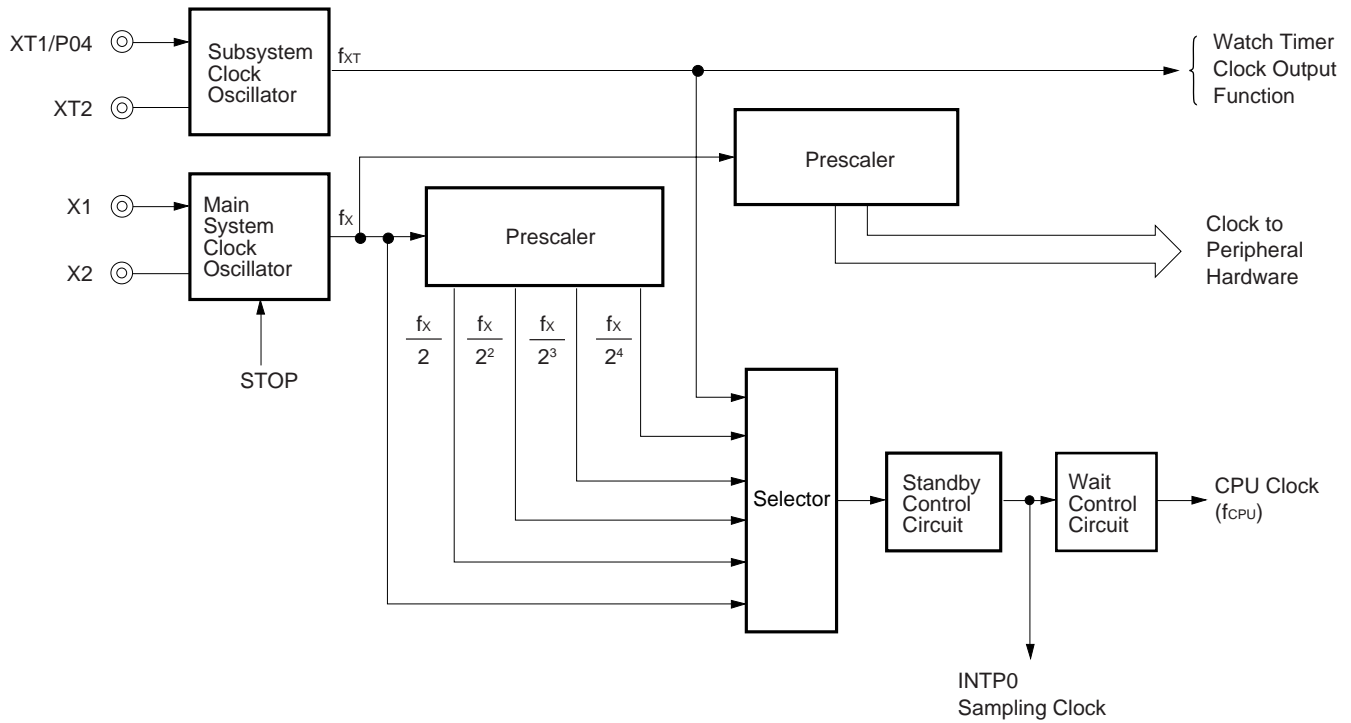


Figure 5-3. 8-bit Timer/Event Counter Block Diagram

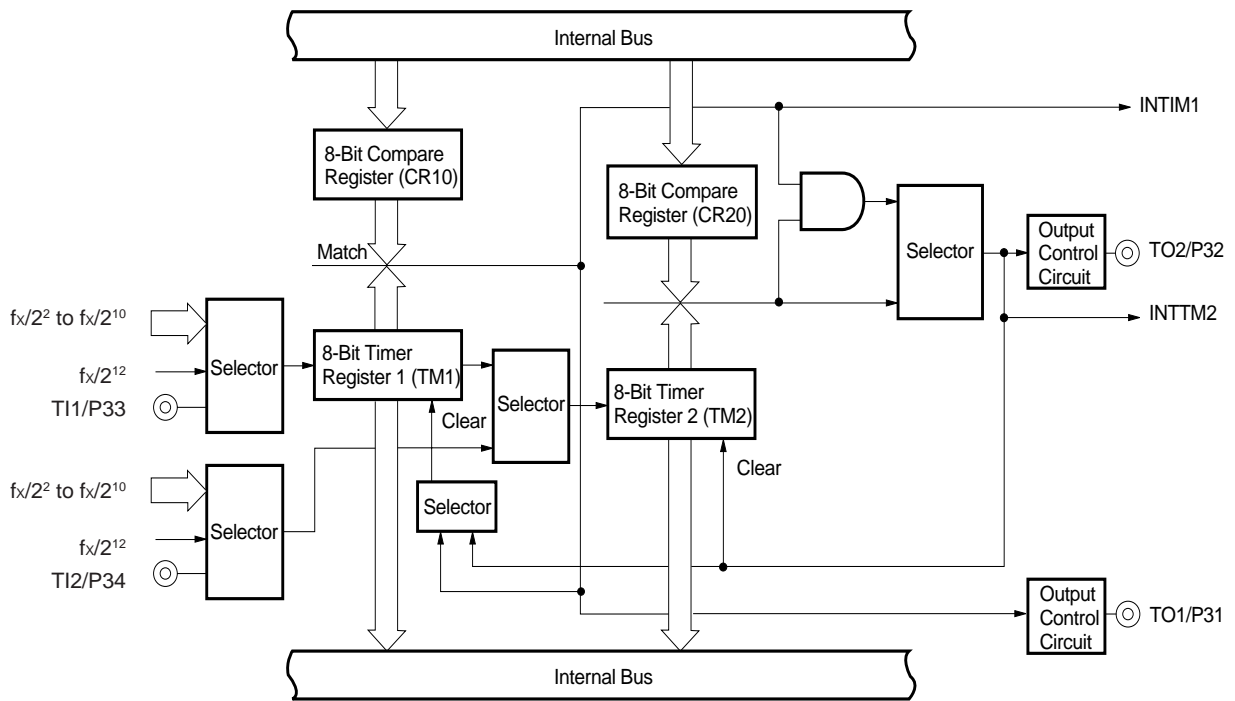


Figure 5-4. Watch Timer Block Diagram

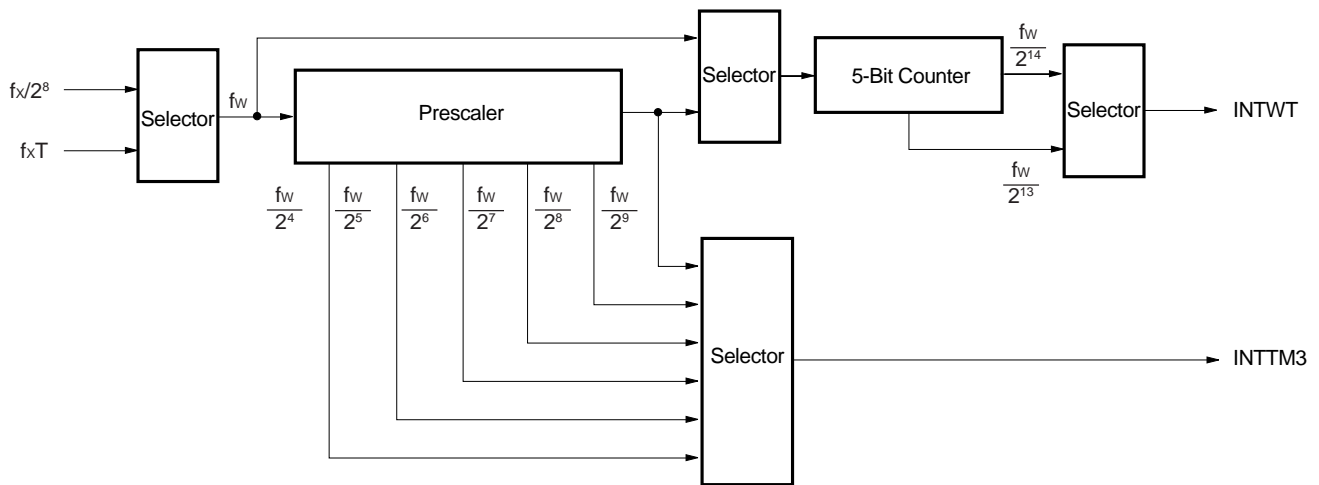
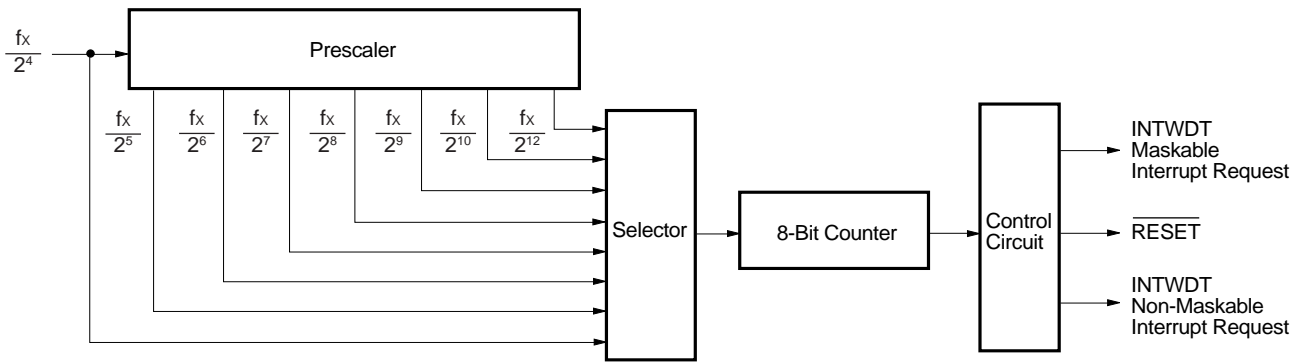


Figure 5-5. Watchdog Timer Block Diagram

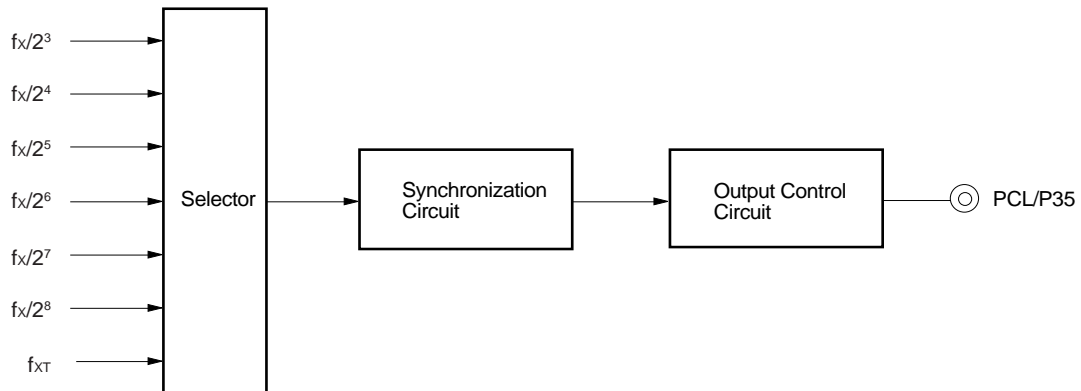


5.4 CLOCK OUTPUT CONTROL CIRCUIT

The clock with the following frequencies can be output for clock output.

- 39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz (Main system clock: at 10.0 MHz operation)
- 32.768 kHz (Subsystem clock: at 32.768 kHz operation)

Figure 5-6. Clock Output Control Block Diagram

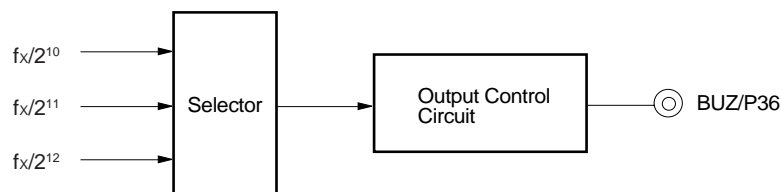


5.5 BUZZER OUTPUT CONTROL CIRCUIT

The clock with the following frequencies can be output for buzzer output.

- 2.4 kHz/4.9 kHz/9.8 kHz (Main system clock: at 10.0 MHz operation)

Figure 5-7. Buzzer Output Control Block Diagram

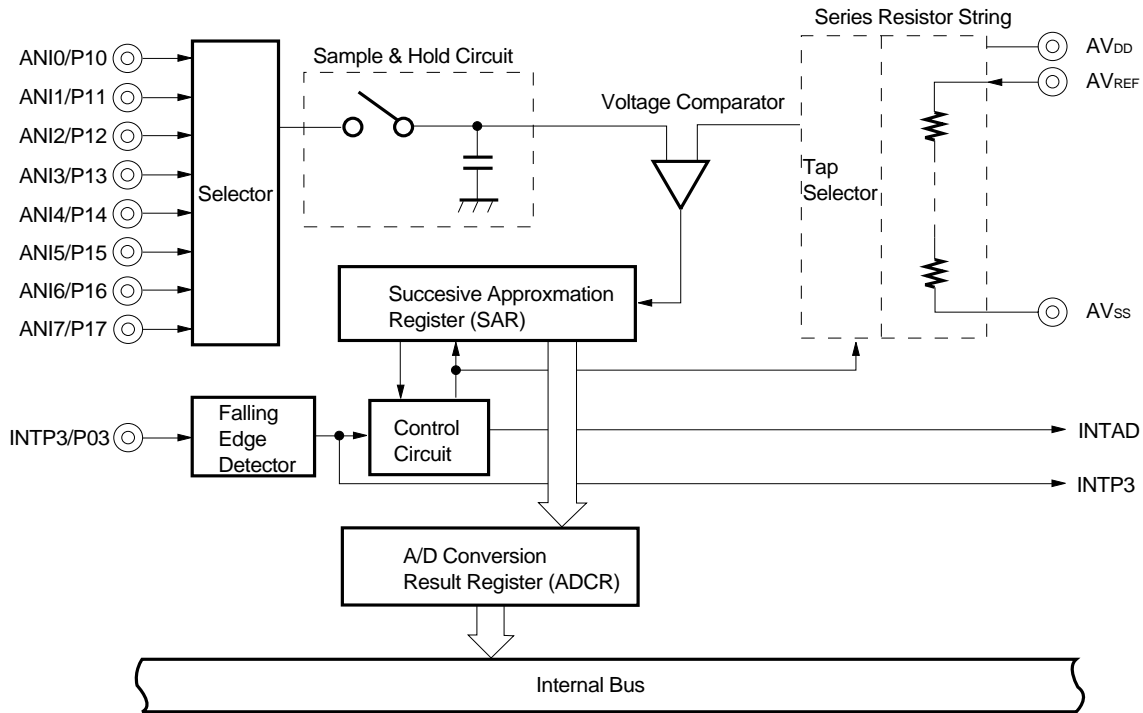


5.6 A/D CONVERTER

The A/D converter has on-chip eight 8-bit resolution channels. There are the following two method to start A/D conversion.

- Hardware starting
- Software starting

Figure 5-8. A/D Converter Block Diagram



5.7 SERIAL INTERFACES

There are two on-chip clocked serial interfaces as follows.

- Serial Interface channel 0
- Serial Interface channel 1

Table 5-3. Type and Function of Serial Interface

Function	Serial Interface Channel 0	Serial Interface Channel 1
3-wire serial I/O mode	O (MSB/LSB-first switchable)	O (MSB/LSB-first switchable)
3-wire serial I/O mode with automatic data transmit/receive function	–	O (MSB/LSB-first switchable)
SBI (Serial Bus Interface) mode	O (MSB-first)	–
2-wire serial I/O mode	O (MSB-first)	–

Figure 5-9. Serial Interface Channel 0 Block Diagram

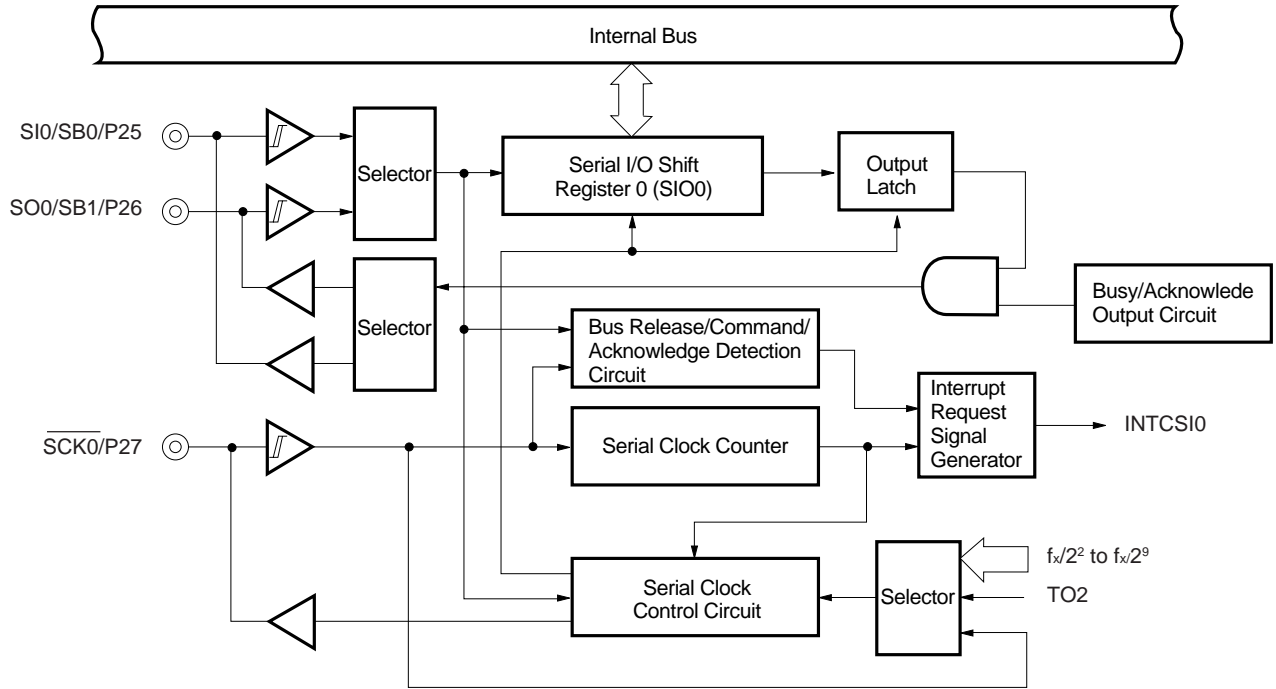
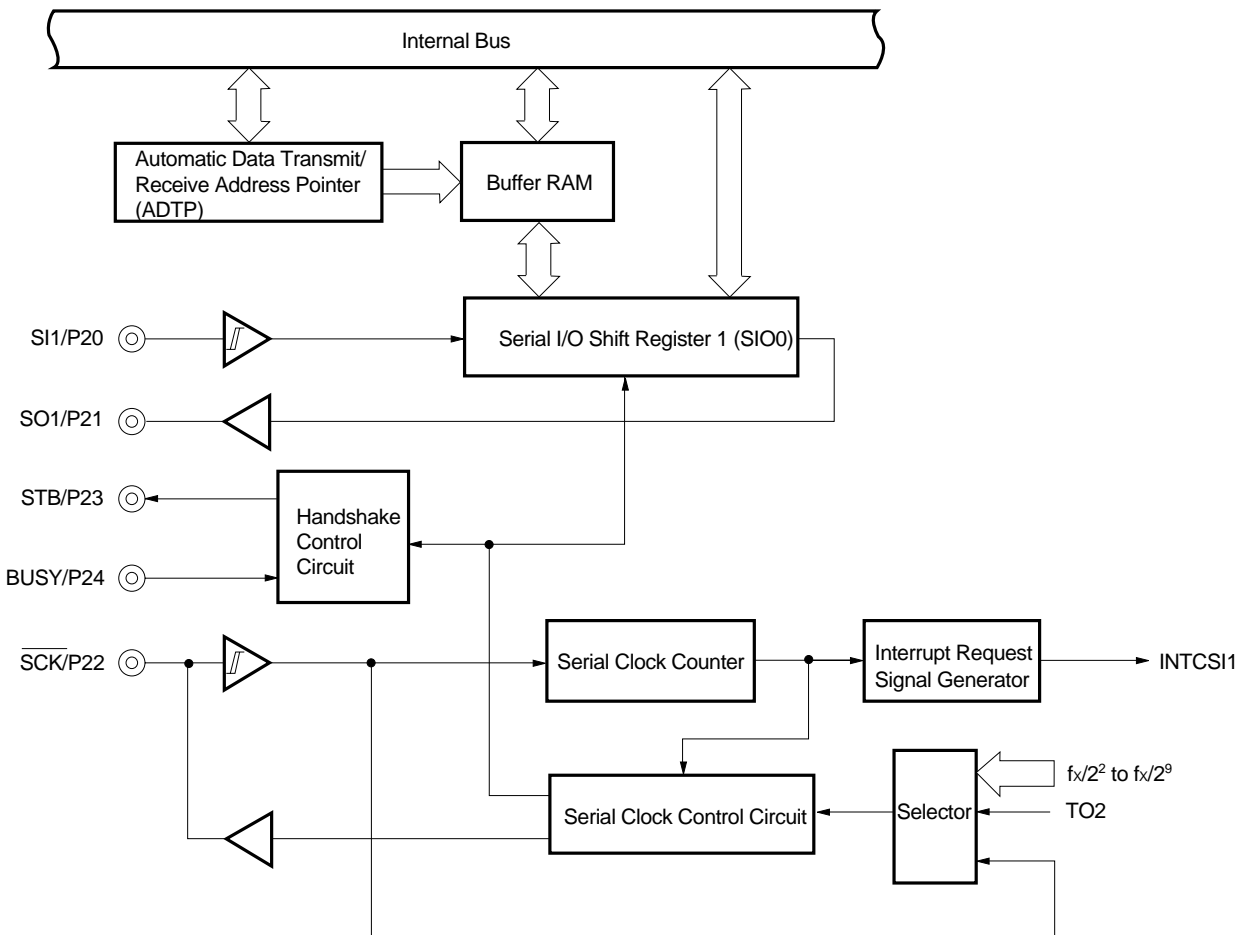


Figure 5-10. Serial Interface Channel 1 Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 INTERRUPT FUNCTIONS

There are interrupt functions, 14 sources of three different kinds, as shown below.

- Non-maskable : 1
- Maskable : 12
- Software : 1

Table 6-1. Interrupt Source List

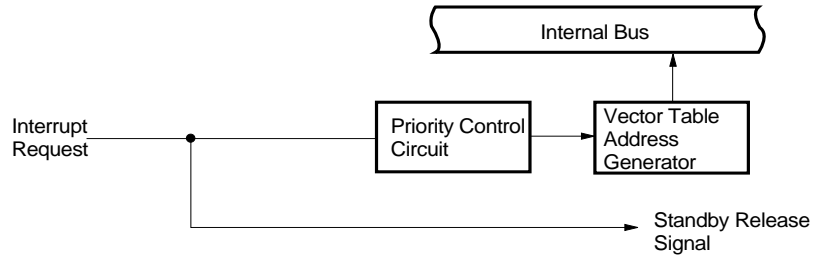
Interrupt Type	Default Priority ^{Note 1}	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuratin Type ^{Note 2}		
		Name	Trigger					
Non-maskable	—	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)		
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			External	0006H 0008H 000AH 000CH	(B)
	1	INTP0	Pin input edge detection	Internal	000EH 0010H 0012H 0014H 0016H 0018H 001AH			(C)
	2	INTP1						(D)
	3	INTP2						(B)
	4	INTP3				(B)		
	5	INTCSI0	Serial interface channel 0 transfer end	Internal	000EH 0010H 0012H 0014H 0016H 0018H 001AH	(B)		
	6	INTCSI1	Serial interface channel 1 transfer end					
	7	INTTM3	Reference time interval signal from watch timer					
	8	INTTM0	16 bit timer/event counter match signal generation					
	9	INTTM1	8-bit timer/event counter 1 match signal generation					
	10	INTTM2	8-bit timer/event counter 2 match signal generation					
11	INTAD	A/D converter conversion end						
Software	—	BRK	BRK instruction execution	—	003EH	(E)		

Notes 1. The default priority is the priority applicable when more than one maskable interrupt request is generated. 0 is the highest priority and 11, the lowest.

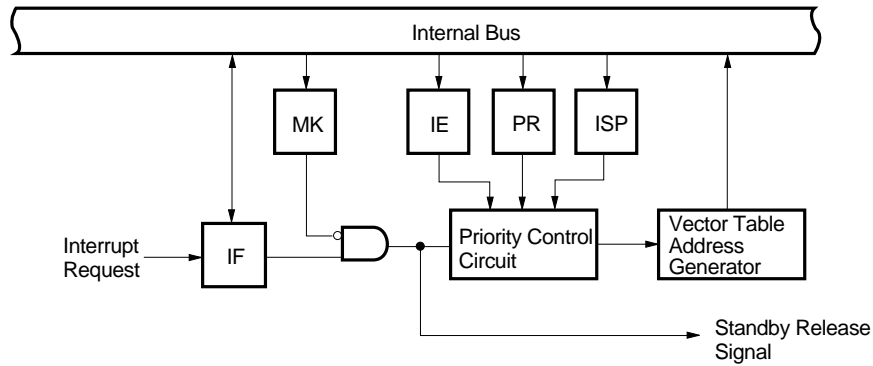
2. Basic configuration types (A) to (E) correspond to (A) to (E) on the next page.

Figure 6-1. Basic Interrupt Function Configuration (1/2)

(A) Internal Non-Maskable Interrupt



(B) Internal Maskable Interrupt



(C) External Maskable Interrupt (INTP0)

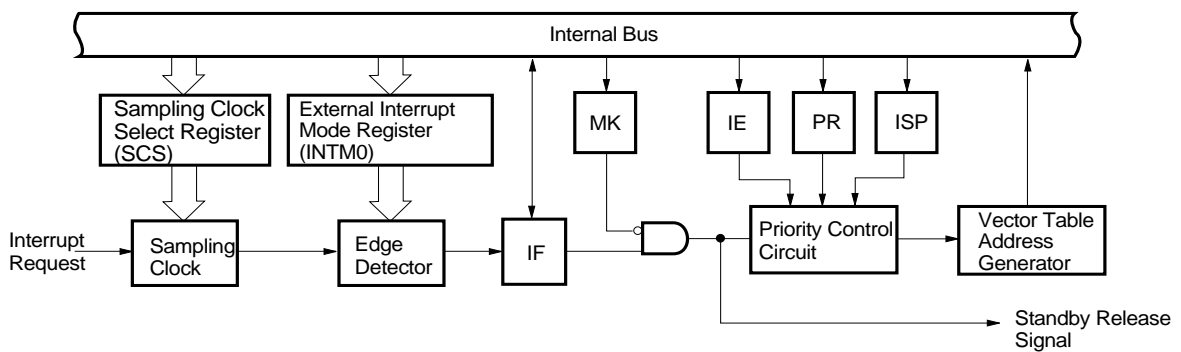
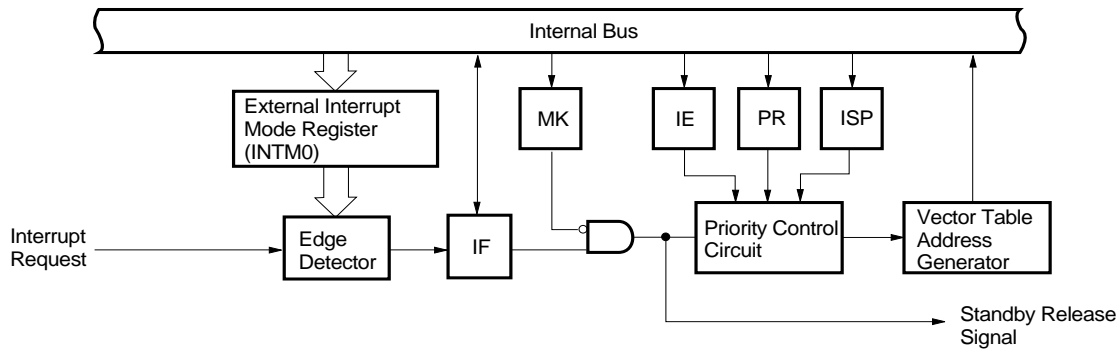
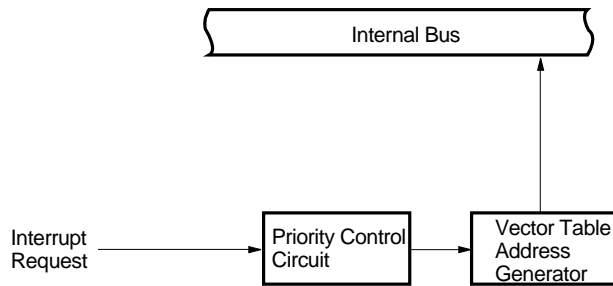


Figure 6-1. Basic Interrupt Function Configuration (2/2)

(D) External Maskable Interrupt (Except INTP0)



(E) Software Interrupt



- IF : Interrupt request flag
- IE : Interrupt enable flag
- ISP : In-service priority flag
- MK : Interrupt mask flag
- PR : Priority specification flag

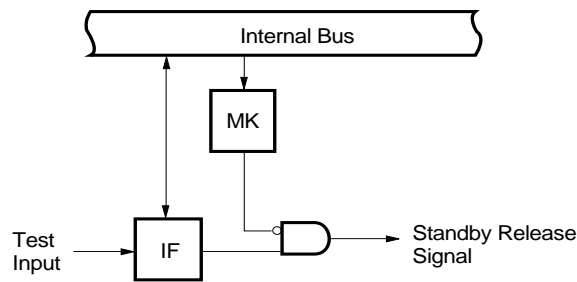
6.2 TEST FUNCTIONS

There are two test functions as shown in Table 6-2.

Table 6-2. Test Source List

Test Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
INTPT4	Port 4 falling edge detection	External

Figure 6-2. Test Function Basic Configuration



IF : Test input flag
 MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

The external device expansion function is used to connect external devices to areas other than the internal ROM, RAM and SFR.

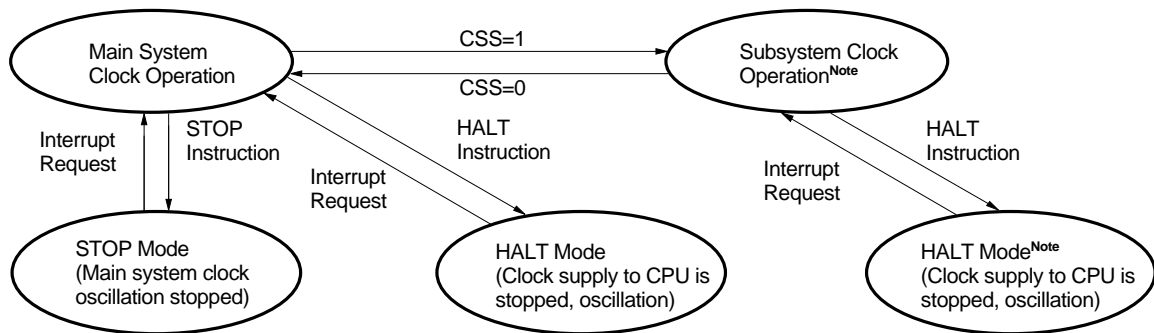
Ports 4 to 6 are used for connection with external devices.

8. STANDBY FUNCTIONS

There are the following two standby functions to reduce the current dissipation.

- **HALT mode** : The CPU operating clock is stopped. The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
- **STOP mode** : The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates with ultra-low power consumption using only the subsystem clock.

Figure 8-1. Standby Functions



Note The power consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set the bit 7 (MCC) of the processor clock control register (PCC) to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program by the program.

9. RESET FUNCTIONS

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin.
- Internal reset by watchdog timer runaway time detection.

Phase-out/Discontinued

10. INSTRUCTION SET

(1) 8-Bit Instruction

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand 1st Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	\$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV	ADD ADDC SUB SUBC AND OR XOR CMP										INC DEC
★ B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV SUBC AND OR XOR CMP	MOV ADD ADDC SUB									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r=A

Phase-out/Discontinued

(2) 16-Bit Instruction

MOVW, XCHW ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand 1st Operand	#byte	AX	rp ^{Note}	saddrp	!addr16	SP	None	
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW ^{Note}						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp=BC, DE, HL.

(3) Bit Manipulation Instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd Operand 1st Operand	A.bit	sfr.bit	saddr.bit	PWS.bit	[HL].bit	CY	\$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call Instruction/Branch Instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd Operand 1st Operand	AX	!addr16	!addr11	[addr5]	\$addr16
Basic instruction	BR	CALL, BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound instruction					BT,BF,BTCLR, DBNZ

(5) Other Instruction

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V _{DD}			-0.3 to +7.0	V
	AV _{DD}			-0.3 to V _{DD} + 0.3	V
	AV _{REF}			-0.3 to V _{DD} + 0.3	V
	AV _{SS}			-0.3 to +0.3	V
Input voltage	V _{I1}	P00 to P04, P10 to P17, P20 to P27, P30 to P37 P40 to P47, P50 to P57, P64 to P67, X1, X2, XT2		-0.3 to V _{DD} + 0.3	V
	V _{I2}	P60 to P67	Open-drain	-0.3 to +16	V
Output voltage	V _O			-0.3 to V _{DD} + 0.3	V
Analog input voltage	V _{AN}	P10 to P17	Analog input pin	AV _{SS} - 0.3 to AV _{REF} + 0.3	V
Output current high	I _{OH}	1 pin		-10	mA
		P10 to P17, P20 to P27, P30 to P37 total		-15	mA
		P01 to P03, P40 to P47, P50 to P57, P60 to P67 total		-15	mA
Output current low	I _{OL} Note	1 pin	Peak value	30	mA
			rms	15	mA
		P40 to P47, P50 to P55 total	Peak value	100	mA
			rms	70	mA
		P01 to P03, P56, P57, P60 to P67 total	Peak value	100	mA
			rms	70	mA
		P01 to P03, P64 to P67 total	Peak value	50	mA
			rms	20	mA
		P10 to P17, P20 to P27, P30 to P37 total	Peak value	50	mA
			rms	20	mA
Operating ambient temperature	T _A			-40 to +85	°C
Storage temperature	T _{stg}			-65 to +150	°C

Note rms should be calculated as follows: [rms] = [peak value] × √duty

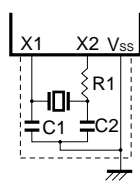
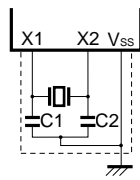
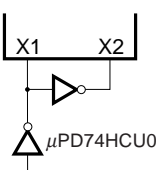
Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{IN}	f = 1 MHz Unmeasured pins returned to 0 V			15	pF
I/O capacitance	C _{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67		15	pF
			P60 to P63		20	pF

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

Main System Clock Oscillation Circuit Characteristics (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (f _x) Note 1	2.7 V ≤ V _{DD} ≤ 5.5 V	1		10	MHz
			1.8 V ≤ V _{DD} < 2.7 V	1		5	
		Oscillation stabilization time Note 2	After V _{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (f _x) Note 1	2.7 V ≤ V _{DD} ≤ 5.5 V	1		10	MHz
			1.8 V ≤ V _{DD} < 2.7 V	1		5	
		Oscillation stabilization time Note 2	V _{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f _x) Note 1		1.0		10.0	MHz
		X1 input high/low level width (t _{xH} , t _{xL})		45		500	ns

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

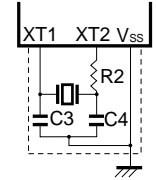
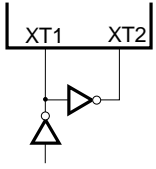
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wiring the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should not be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as V_{SS}.
- Do not ground wiring to a ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Subsystem Clock Oscillation Circuit Characteristics ($T_A = -40$ to $+85$ °C, $V_{DD} = 1.8$ to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	$V_{DD} = 4.5$ to 5.5 V		1.2	2	s
External clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high/low level width (t_{XTH} , t_{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should not be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as V_{SS} .
- Do not ground wiring to a ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

2. The subsystem clock oscillation circuit is a circuit with a low amplification level, more prone to misoperation due to noise than the main system clock.

Particular care is therefore required with the wiring method when the subsystem clock is used.

★ **Recommended Oscillation Circuit Constant**

Recommended oscillation circuit constant differs depending on the model.

(1) μPD78011F, 78012F, 78013F, 78014F

(a) **Main system clock: ceramic resonator** (T_A = -45 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
TDK Corp.	CCR4.19MC3	4.19	Built-in	Built-in	1.8	5.5
	FCR4.19MC5	4.19	Built-in	Built-in	1.8	5.5
	CCR5.00MC3	5.00	Built-in	Built-in	1.8	5.5
	FCR5.00MC5	5.00	Built-in	Built-in	1.8	5.5
	CCR8.38MC	8.00	Built-in	Built-in	2.7	5.5
	FCR8.38MC5	8.00	Built-in	Built-in	2.7	5.5
	CCR10.00MC	10.00	Built-in	Built-in	2.7	5.5
	FCR10.00MC5	10.00	Built-in	Built-in	2.7	5.5
Murata Mfg. Co. Ltd.	CSA4.19MG	4.19	30	30	1.8	5.5
	CST4.19MGW	4.19	Built-in	Built-in	1.8	5.5
	CSA5.00MG	5.00	30	30	1.8	5.5
	CST5.00MGW	5.00	Built-in	Built-in	1.8	5.5
	CSA8.38MTZ	8.38	30	30	2.7	5.5
	CST8.38MTW	8.38	Built-in	Built-in	2.7	5.5
	CSA10.00MTZ	10.00	30	30	2.7	5.5
	CST10.00MTW	10.00	Built-in	Built-in	2.7	5.5

(b) **Main system clock: ceramic resonator** (T_A = -20 to +80 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Kyocera Corp.	PBRC5.00A	5.00	33	33	1.8	5.5
	PBRC5.00B	5.00	Built-in	Built-in	1.8	5.5
	KBR-5.00MSA	5.00	33	33	1.8	5.5
	KBR-5.00MKS	5.00	Built-in	Built-in	1.8	5.5
	KBR-8M	8.00	33	33	2.7	5.5
	KBR-10M	10.00	33	33	2.7	5.5

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee the accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact manufacturer of the resonator being used.

(2) μPD78015F, 78016F

(a) Main system clock: ceramic resonator (T_A = -45 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
TDK Corp.	CSB1000J	1.00	100	100	5.6	1.8	6.0
	CSA2.00MG040	2.00	100	100	0	1.8	6.0
	CST2.00MG040	2.00	Built-in	Built-in	0	1.8	6.0
	CSA4.00MG040	4.00	100	100	0	1.8	6.0
	CST4.00MGW040	4.00	Built-in	Built-in	0	1.8	6.0
	CSA6.00MG	6.00	30	30	0	1.8	6.0
	CST6.00MGW	6.00	Built-in	Built-in	0	1.8	6.0
	CSA10.0MTZ	10.0	30	30	0	1.8	6.0
	CST10.0MTW	10.0	Built-in	Built-in	0	1.8	6.0
Murata Mfg. Co. Ltd. (EMI noise reduced products)	CSA6.00MG040	6.00	100	100	0	2.7	6.0
	CST6.00MGW040	6.00	Built-in	Built-in	0	2.7	6.0
	CSA10.0MTZ040	10.0	100	100	0	2.7	6.0
	CST10.0MTW040	10.0	Built-in	Built-in	0	2.7	6.0
TDK Corp.	FCR4.0MC5	4.0	Built-in	Built-in	2.2	1.8	6.0
	FCR10.0MC	10.0	Built-in	Built-in	1.0	1.8	6.0

(b) Main system clock: ceramic resonator (T_A = -20 to +80 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Kyocera Corp.	PBRC5.00A	5.00	33	33	1.8	5.5
	PBRC5.00B	5.00	Built-in	Built-in	1.8	5.5
	KBR-5.00MSA	5.00	33	33	1.8	5.5
	KBR-5.00MKS	5.00	Built-in	Built-in	1.8	5.5
	KBR-8M	8.00	33	33	2.7	5.5
	KBR-10M	10.00	33	33	2.7	5.5

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee the accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact manufacturer of the resonator being used.

(3) μPD78018F

(a) Main system clock: ceramic resonator (T_A = -40 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
TDK Corp.	CCR4.0MC3	4.00	Built-in	Built-in	1.8	5.5
	FCR4.0MC5	4.00	Built-in	Built-in	1.8	5.5
	CCR8.0MC5	8.00	Built-in	Built-in	2.7	5.5
	FCR8.0MC	8.00	Built-in	Built-in	2.7	5.5
	CCR10.0MC5	10.0	Built-in	Built-in	2.7	5.5
	FCR10.0MC	10.0	Built-in	Built-in	2.7	5.5
Murata Mfg. Co. Ltd.	CSA4.0MG	4.00	30	30	1.8	5.5
	CST4.0MGW	4.00	Built-in	Built-in	1.8	5.5
	CSA8.0MTZ	8.00	30	30	2.7	5.5
	CST8.0MTW	8.00	Built-in	Built-in	2.7	5.5

(b) Main system clock: ceramic resonator (T_A = -20 to +80 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Kyocera Corp.	FBRC4.00A	4.00	33	33	1.8	5.5
	FBRC4.00B	4.00	Built-in	Built-in	1.8	5.5
	KBR-4.00MSB	4.00	33	33	1.8	5.5
	KBR-4.00MKC	4.00	Built-in	Built-in	1.8	5.5
	KBR-8M	8.00	33	33	2.7	5.5
	KBR-10M	10.00	33	33	2.7	5.5

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee the accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact manufacturer of the resonator being used.

DC Characteristics ($T_A = -40$ to $+85$ °C, $V_{DD} = 1.8$ to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage high	V _{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to 67	V _{DD} = 2.7 to 5.5 V	0.7 V _{DD}		V _{DD}	V
				0.8 V _{DD}		V _{DD}	V
	V _{IH2}	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$	V _{DD} = 2.7 to 5.5 V	0.8 V _{DD}		V _{DD}	V
				0.85 V _{DD}		V _{DD}	V
	V _{IH3}	P60 to P63 (N-ch open-drain)	V _{DD} = 2.7 to 5.5 V	0.7 V _{DD}		15	V
				0.8 V _{DD}		15	V
	V _{IH4}	X1, X2	V _{DD} = 2.7 to 5.5 V	V _{DD} - 0.5		V _{DD}	V
				V _{DD} - 0.2		V _{DD}	V
	V _{IH5}	XT1/P04, XT2	4.5 V ≤ V _{DD} ≤ 5.5 V	0.8 V _{DD}		V _{DD}	V
			2.7 V ≤ V _{DD} < 4.5 V	0.9 V _{DD}		V _{DD}	V
1.8 V ≤ V _{DD} < 2.7 V Note			0.9 V _{DD}		V _{DD}	V	
Input voltage low	V _{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to 67	V _{DD} = 2.7 to 5.5 V	0		0.3 V _{DD}	V
				0		0.2 V _{DD}	V
	V _{IL2}	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$	V _{DD} = 2.7 to 5.5 V	0		0.2 V _{DD}	V
				0		0.15 V _{DD}	V
	V _{IL3}	P60 to P63	4.5 V ≤ V _{DD} ≤ 5.5 V	0		0.3 V _{DD}	V
			2.7 V ≤ V _{DD} < 4.5 V	0		0.2 V _{DD}	V
				0		0.1 V _{DD}	V
	V _{IL4}	X1, X2	V _{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V _{IL5}	XT1/P04, XT2	4.5 V ≤ V _{DD} ≤ 5.5 V	0		0.2 V _{DD}	V
2.7 V ≤ V _{DD} < 4.5 V			0		0.1 V _{DD}	V	
1.8 V ≤ V _{DD} < 2.7 V Note			0		0.1 V _{DD}	V	
Output voltage high	V _{OH1}	V _{DD} = 4.5 to 5.5 V, I _{OH} = -1 mA	V _{DD} - 1.0			V	
		I _{OH} = -100 μA	V _{DD} - 0.5			V	
Output voltage low	V _{OL1}	P50 to P57, P60 to P63	V _{DD} = 4.5 to 5.5 V, I _{OL} = 15 mA		0.4	2.0	V
		P01 to P03, P10 to P17, P20 to P27 P30 to P37, P40 to P47, P64 to P67	V _{DD} = 4.5 to 5.5 V, I _{OL} = 1.6 mA			0.4	V
	V _{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V _{DD} = 4.5 to 5.5 V, open-drain pulled-up (R = 1 KΩ)			0.2 V _{DD}	V
	V _{OL3}	I _{OL} = 400 μA				0.5	V

Note When using XT1/P04 as P04, input the inverse of P04 to XT2 using an inverter.

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

DC Characteristics ($T_A = -40$ to $+85$ °C, $V_{DD} = 1.8$ to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current high	I _{LIH1}	V _{IN} = V _{DD}			3	μA
	I _{LIH2}				20	μA
	I _{LIH3}	V _{IN} = 15 V			80	μA
Input leakage current low	I _{LIL1}	V _{IN} = 0 V			-3	μA
	I _{LIL2}				-20	μA
	I _{LIL3}				-3 Note	μA
Output leakage current high	I _{LOH1}	V _{OUT} = V _{DD}			3	μA
Output leakage current low	I _{LOL}	V _{OUT} = 0 V			-3	μA
Mask option pull-up resistor	R1	V _{IN} = 0 V, P60 to P63	20	40	90	kΩ
Software pull-up resistor	R2	V _{IN} = 0 V, P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67	15	40	90	kΩ

Note For P60 to P63, if pull-up resistor is not provided (specifiable by mask option) a low-level input leak current of -200 μA (MAX.) flows only during the 3 clocks (no-wait time) after an instruction has been executed to read out port 6 (P6) or port mode register 6 (PM6). Outside the period of 3 clocks following execution a read-out instruction, the current is -3 μA (MAX.).

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

DC Characteristics ($T_A = -40$ to $+85$ °C, $V_{DD} = 1.8$ to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD1}	10.00 MHz crystal oscillation operation mode	$V_{DD} = 5.0\text{ V} \pm 10\%$ Note 2		9.0	18.0	mA
			$V_{DD} = 3.0\text{ V} \pm 10\%$ Note 3		1.3	2.6	mA
	I _{DD2}	10.00 MHz crystal oscillation HALT mode	$V_{DD} = 5.0\text{ V} \pm 10\%$ Note 2		2.4	4.8	mA
			$V_{DD} = 3.0\text{ V} \pm 10\%$ Note 3		1.2	2.4	mA
	I _{DD3}	32.768 kHz crystal oscillation operation mode Note 4	$V_{DD} = 5.0\text{ V} \pm 10\%$		60	120	μA
			$V_{DD} = 3.0\text{ V} \pm 10\%$		35	70	μA
			$V_{DD} = 2.0\text{ V} \pm 10\%$		24	48	μA
	I _{DD4}	32.768 kHz crystal oscillation HALT mode Note 4	$V_{DD} = 5.0\text{ V} \pm 10\%$		25	50	μA
			$V_{DD} = 3.0\text{ V} \pm 10\%$		5	15	μA
			$V_{DD} = 2.0\text{ V} \pm 10\%$		2	10	μA
	I _{DD5}	XT1 = V_{DD} STOP mode when using feedback resistor	$V_{DD} = 5.0\text{ V} \pm 10\%$		1	30	μA
			$V_{DD} = 3.0\text{ V} \pm 10\%$		0.5	10	μA
$V_{DD} = 2.0\text{ V} \pm 10\%$				0.3	10	μA	
I _{DD6}	XT1 = V_{DD} STOP mode when not using feedback resistor	$V_{DD} = 5.0\text{ V} \pm 10\%$		0.1	30	μA	
		$V_{DD} = 3.0\text{ V} \pm 10\%$		0.05	10	μA	
		$V_{DD} = 2.0\text{ V} \pm 10\%$		0.05	10	μA	

- Notes**
- 1.** This current excludes the A_{VREF} current, port current, and current which flows in the built-in pull-down resistor.
 - 2.** When operating at high-speed mode (when the processor clock control register (PCC) is set to 00H)
 - 3.** When operating at low-speed mode (when the PCC is set to 04H)
 - 4.** When main system clock stopped.

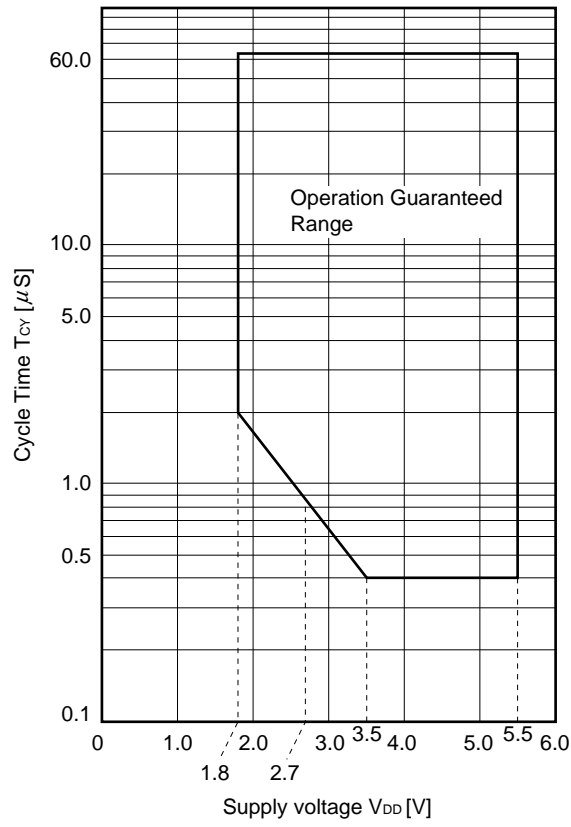
AC Characteristics

(1) Basic Operation (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T _{CY}	Operating on main system clock	3.5 V ≤ V _{DD} ≤ 5.5 V	0.4		64	μs
			2.7 V ≤ V _{DD} < 3.5 V	0.8		64	μs
			1.8 V ≤ V _{DD} < 2.7 V	2.0		64	μs
		Operating on subsystem clock		40	122	125	μs
TI0 input frequency	t _{TIH0}	3.5 V ≤ V _{DD} ≤ 5.5 V		2/f _{sam} + 0.1 Note			μs
	t _{TIL0}	2.7 V ≤ V _{DD} < 3.5 V		2/f _{sam} + 0.2 Note			μs
		1.8 V ≤ V _{DD} < 2.7 V		2/f _{sam} + 0.5 Note			μs
TI1, TI2 input frequency	f _{TI1}	V _{DD} = 4.5 to 5.5 V		0		4	MHz
				0		275	kHz
TI1, TI2 input high/low-level width	t _{TIH1}	V _{DD} = 4.5 to 5.5 V		100			ns
	t _{TIL1}			1.8			μs
Interrupt request input high/low-level width	t _{INTH}	INTP0	3.5 V ≤ V _{DD} ≤ 5.5 V	2/f _{sam} + 0.1 Note			μs
			2.7 V ≤ V _{DD} < 3.5 V	2/f _{sam} + 0.2 Note			μs
			1.8 V ≤ V _{DD} < 2.7 V	2/f _{sam} + 0.5 Note			μs
	t _{INTL}	INTP1 to INTP3, KR0 to KR7	V _{DD} = 2.7 to 5.5 V		10		μs
					20		μs
RESET low level width	t _{RSL}	V _{DD} = 2.7 to 5.5 V		10		μs	
				20		μs	

Note In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f_{sam} is possible between f_X/2^{N+1}, f_X/64 and f_X/128 (when N= 0 to 4).

T_{CY} vs V_{DD} (At main system clock operation)



(2) Read/Write Operation (T_A = -40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t _{ASTH}		0.5t _{cy}		ns
Address setup time	t _{ADS}		0.5t _{cy} - 30		ns
Address hold time	t _{ADH}		50		ns
Data input time from address	t _{ADD1}			(2.5 + 2n) t _{cy} - 50	ns
	t _{ADD2}			(3 + 2n) t _{cy} - 100	ns
Data input time from $\overline{RD}\downarrow$	t _{rDD1}			(1 + 2n) t _{cy} - 25	ns
	t _{rDD2}			(2.5 + 2n) t _{cy} - 100	ns
Read data hold time	t _{RDH}		0		ns
\overline{RD} low-level width	t _{rDL1}		(1.5 + 2n) t _{cy} - 20		ns
	t _{rDL2}		(2.5 + 2n) t _{cy} - 20		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t _{rDWT1}			0.5t _{cy}	ns
	t _{rDWT2}			1.5t _{cy}	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t _{rRWT}			0.5t _{cy}	ns
\overline{WAIT} low-level width	t _{wTL}		(0.5 + 2n) t _{cy} + 10	(2 + 2n) t _{cy}	ns
Write data setup time	t _{wDS}		100		ns
Write data hold time	t _{wDH}	Load resistor ≥ 5 kΩ	20		ns
\overline{WR} low-level width	t _{wRL1}		(2.5 + 2n) t _{cy} - 20		ns
$\overline{RD}\downarrow$ delay time from ASTB \downarrow	t _{ASTRD}		0.5t _{cy} - 30		ns
$\overline{WR}\downarrow$ delay time from ASTB \downarrow	t _{ASTWR}		1.5t _{cy} - 30		ns
ASTB \uparrow delay time from RD \uparrow in external fetch	t _{RDAST}		t _{cy} - 10	t _{cy} + 40	ns
Address hold time from RD \uparrow in external fetch	t _{RDADH}		t _{cy}	t _{cy} + 50	ns
Write data output time from RD \uparrow	t _{rDWD}	V _{DD} = 4.5 to 5.5 V	0.5t _{cy} + 5	0.5t _{cy} + 30	ns
			0.5t _{cy} + 15	0.5t _{cy} + 90	ns
Write data output time from $\overline{WR}\downarrow$	t _{wRWD}	V _{DD} = 4.5 to 5.5 V	5	30	ns
			15	90	ns
Address hold time from $\overline{WR}\uparrow$	t _{wRADH}	V _{DD} = 4.5 to 5.5 V	t _{cy}	t _{cy} + 60	ns
			t _{cy}	t _{cy} + 100	ns
RD \uparrow delay time from $\overline{WAIT}\uparrow$	t _{wTRD}		0.5t _{cy}	2.5t _{cy} + 80	ns
WR \uparrow delay time from $\overline{WAIT}\uparrow$	t _{wTWR}		0.5t _{cy}	2.5t _{cy} + 80	ns

- Remarks**
1. t_{cy} = T_{cy}/4
 2. n indicates number of waits.

(3) Serial Interface (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

(a) Serial Interface Channel 0

(i) 3-wire serial I/O mode ($\overline{\text{SCK0}}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t _{KCY1}	4.5 V ≤ V _{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V _{DD} < 4.5 V	1600			ns
		2.0 V ≤ V _{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{\text{SCK0}}$ high/low-level width	t _{KH1}	V _{DD} = 4.5 to 5.5 V	t _{KCY1} /2 - 50			ns
	t _{KL1}		t _{KCY1} /2 - 100			ns
SIO setup time (to $\overline{\text{SCK0}}\uparrow$)	t _{SIK1}	4.5 V ≤ V _{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V _{DD} < 4.5 V	150			ns
		2.0 V ≤ V _{DD} < 2.7 V	300			ns
			400			ns
SIO hold time (from $\overline{\text{SCK0}}\uparrow$)	t _{KS1}		400			ns
SO0 output delay time from $\overline{\text{SCK0}}\downarrow$	t _{KSO1}	C = 100 pF Note			300	ns

Note C is the load capacitance of $\overline{\text{SCK0}}$ and SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK0}}$... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t _{KCY2}	4.5 V ≤ V _{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V _{DD} < 4.5 V	1600			ns
		2.0 V ≤ V _{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{\text{SCK0}}$ high/low-level width	t _{KH2}	4.5 V ≤ V _{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V _{DD} < 4.5 V	800			ns
	t _{KL2}	2.0 V ≤ V _{DD} < 2.7 V	1600			ns
			2400			ns
SIO setup time (to $\overline{\text{SCK0}}\uparrow$)	t _{SIK2}	V _{DD} = 2.0 to 5.5 V	100			ns
			150			ns
SIO hold time (from $\overline{\text{SCK0}}\uparrow$)	t _{KS2}		400			ns
SO0 output delay time from $\overline{\text{SCK0}}\downarrow$	t _{KSO2}	C = 100 pF Note V _{DD} = 2.0 to 5.5 V			300	ns
					500	ns
$\overline{\text{SCK0}}$ rise, fall time	t _{r2} t _{f2}	When external device expansion function is used			160	ns
		When external device expansion function is not used	When 16-bit timer output function is used		700	ns
			When 16-bit timer output function is not used		1000	ns

Note C is the load capacitance of SO0 output line.

(iii) SBI mode ($\overline{\text{SCK0}}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY3}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$		800			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$		3200			ns
				4800			ns
$\overline{\text{SCK0}}$ high/low-level width	t_{KH3} t_{KL3}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		$t_{\text{KCY3}}/2 - 50$			ns
				$t_{\text{KCY3}}/2 - 150$			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$)	t_{SIK3}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$		100			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$		300			ns
				400			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$)	t_{KS13}			$t_{\text{KCY3}}/2$			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{KSO3}	R = 1 kΩ, C = 100 pF Note	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{\text{SCK0}}\uparrow$	t_{KSB}			t_{KCY3}			ns
$\overline{\text{SCK0}}\downarrow$ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistors and load capacitance of the SB0, SB1 and $\overline{\text{SCK0}}$ output line.

(iv) SBI mode (SCK0... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCK0 cycle time	t _{KCY4}	4.5 V ≤ V _{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V _{DD} < 4.5 V		3200			ns
				4800			ns
SCK0 high/low-level width	t _{KH4}	4.5 V ≤ V _{DD} ≤ 5.5 V		400			ns
	t _{KL4}	2.0 V ≤ V _{DD} < 4.5 V		1600			ns
				2400			ns
SB0, SB1 setup time (to SCK0↑)	t _{SIK4}	4.5 V ≤ V _{DD} ≤ 5.5 V		100			ns
		2.0 V ≤ V _{DD} < 4.5 V		300			ns
				400			ns
SB0, SB1 hold time (from SCK0↑)	t _{KSI4}			t _{KCY4} /2			ns
SB0, SB1 output delay time from SCK0↓	t _{KSO4}	R = 1 kΩ, C = 100 pF Note	V _{DD} = 4.5 to 5.5 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from SCK0↑	t _{KSB}			t _{KCY4}			ns
SCK0↓ from SB0, SB1↓	t _{SBK}			t _{KCY4}			ns
SB0, SB1 high-level width	t _{SBH}			t _{KCY4}			ns
SB0, SB1 low-level width	t _{SBL}			t _{KCY4}			ns
SCK0 rise, fall time	t _{R4} t _{F4}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(v) 2-wire serial I/O mode ($\overline{\text{SCK0}}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{\text{SCK0}}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF Note	$2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	1600			ns
			$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3200			ns
				4800			ns
$\overline{\text{SCK0}}$ high-level width	t_{KH5}		$V_{\text{DD}} = 2.7 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY5}}/2 - 160$			ns
				$t_{\text{KCY5}}/2 - 190$			ns
$\overline{\text{SCK0}}$ low-level width	t_{KL5}		$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY5}}/2 - 50$			ns
				$t_{\text{KCY5}}/2 - 100$			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$)	t_{SIK5}		$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	300			ns
			$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	350			ns
			$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	400			ns
				500			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$)	t_{KS15}		600			ns	
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{KSO5}		0		300	ns	

Note R and C are the load resistors and load capacitance of the $\overline{\text{SCK0}}$, SB0 and SB1 output line.

(vi) 2-wire serial I/O mode (SCK0... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCK0 cycle time	tkCY6	2.7 V ≤ V _{DD} ≤ 5.5 V		1600			ns
		2.0 V ≤ V _{DD} < 2.7 V		3200			ns
				4800			ns
SCK0 high-level width	tkH6	2.7 V ≤ V _{DD} ≤ 5.5 V		650			ns
		2.0 V ≤ V _{DD} < 2.7 V		1300			ns
				2100			ns
SCK0 low-level width	tkL6	2.7 V ≤ V _{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V _{DD} < 2.7 V		1600			ns
				2400			ns
SB0, SB1 setup time (to SCK0↑)	tSIK6	V _{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SB0, SB1 hold time (from SCK0↑)	tkS16			tkCY6/2			ns
SB0, SB1 output delay time from SCK0↓	tkSO6	R = 1 kΩ, C = 100 pF Note	4.5 V ≤ V _{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V _{DD} < 4.5 V	0		500	ns
				0		800	ns
SCK0 rise, fall time	tr6 tf6	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(b) Serial Interface Channel 1

(i) 3-wire serial I/O mode (SCK1... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SCK1 cycle time	t _{KCY7}	4.5 V ≤ V _{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V _{DD} < 4.5 V	1600			ns
		2.0 V ≤ V _{DD} < 2.7 V	3200			ns
			4800			ns
SCK1 high/low-level width	t _{KH7}	V _{DD} = 4.5 to 5.5 V	t _{KCY7} /2 – 50			ns
	t _{KL7}		t _{KCY7} /2 – 100			ns
SI1 setup time (to SCK1↑)	t _{SIK7}	4.5 V ≤ V _{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V _{DD} < 4.5 V	150			ns
		2.0 V ≤ V _{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from SCK1↑)	t _{KSI7}		400			ns
SO1 output delay time from SCK1↓	t _{KSO7}	C = 100 pF Note			300	ns

Note C is the load capacitance of SCK1 and SO1 output line.

(ii) 3-wire serial I/O mode (SCK1... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SCK1 cycle time	t _{KCY8}	4.5 V ≤ V _{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V _{DD} < 4.5 V	1600			ns
		2.0 V ≤ V _{DD} < 2.7 V	3200			ns
			4800			ns
SCK1 high/low-level width	t _{KH8} t _{KL8}	4.5 V ≤ V _{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V _{DD} < 4.5 V	800			ns
		2.0 V ≤ V _{DD} < 2.7 V	1600			ns
			2400			ns
SI1 setup time (to SCK1↑)	t _{SIK8}	V _{DD} = 2.0 to 5.5 V	100			ns
			150			ns
SI1 hold time (from SCK1↑)	t _{KSI8}		400			ns
SO0 output delay time from SCK1↓	t _{KSO8}	C = 100 pF Note V _{DD} = 2.0 to 5.5 V			300	ns
					500	ns
SCK1 rise, fall time	t _{R8} t _{F8}	When external device expansion function is used			160	ns
		When external device expansion function is not used	When 16-bit timer output function is used		700	ns
			When 16-bit timer output function is not used		1000	ns

Note C is the load capacitance of SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{\text{SCK1}}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY9}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3200			ns
			4800			ns
$\overline{\text{SCK1}}$ high/low-level width	t_{KH9}	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY9}}/2 - 50$			ns
	t_{KL9}		$t_{\text{KCY9}}/2 - 100$			ns
SI1 setup time (to $\overline{\text{SCK1}}\uparrow$)	t_{SIK9}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	300			ns
			400			ns
SI1 hold time (from $\overline{\text{SCK1}}\uparrow$)	t_{KS9}		400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	t_{KSO9}	$C = 100 \text{ pF}$ Note			300	ns
$\text{STB}\uparrow$ from $\overline{\text{SCK1}}\uparrow$	t_{SBD}		$t_{\text{KCY9}}/2 - 100$		$t_{\text{KCY9}}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}	$2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	$t_{\text{KCY9}} - 30$		$t_{\text{KCY9}} + 30$	ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	$t_{\text{KCY9}} - 60$		$t_{\text{KCY9}} + 60$	ns
			$t_{\text{KCY9}} - 90$		$t_{\text{KCY9}} + 90$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	200			ns
			300			ns
$\overline{\text{SCK1}}\downarrow$ from busy inactive	t_{SPS}				$2t_{\text{KCY9}}$	ns

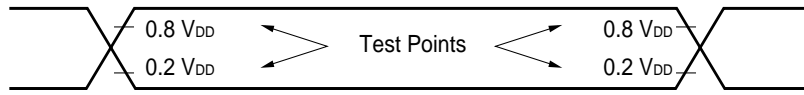
Note C is the load capacitance of $\overline{\text{SCK1}}$ and SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{\text{SCK1}}$... External clock input)

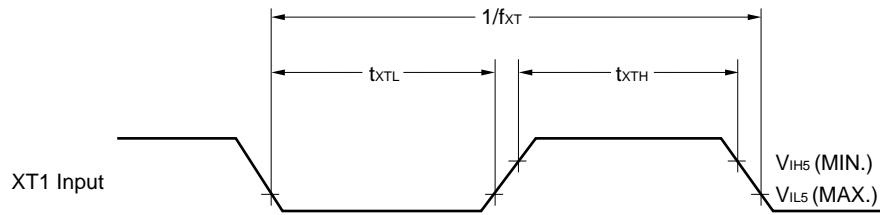
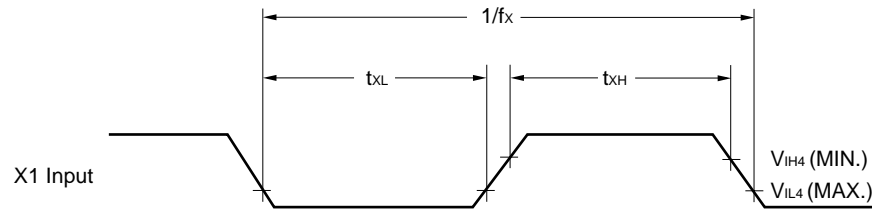
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KC}10}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3200			ns
			4800			ns
$\overline{\text{SCK1}}$ high/low-level width	$t_{\text{KH}10}, t_{\text{KL}10}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	400			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	800			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	1600			ns
			2400			ns
SI1 setup time (to $\overline{\text{SCK1}}\uparrow$)	$t_{\text{SIK}10}$	$V_{\text{DD}} = 2.0 \text{ to } 5.5 \text{ V}$	100			ns
			150			ns
SI1 hold time (from $\overline{\text{SCK1}}\uparrow$)	$t_{\text{KS}10}$		400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	$t_{\text{KSO}10}$	C = 100 pF Note $V_{\text{DD}} = 2.0 \text{ to } 5.5 \text{ V}$			300	ns
					500	ns
$\overline{\text{SCK1}}$ rise, fall time	$t_{\text{R}10}, t_{\text{F}10}$	When external device expansion function is used			160	ns
		When external device expansion function is not used			1000	ns

Note C is the load capacitance of the SO1 output line.

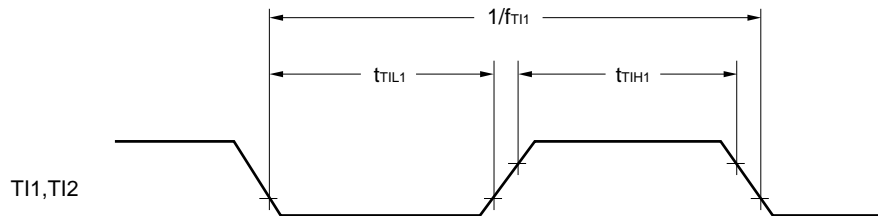
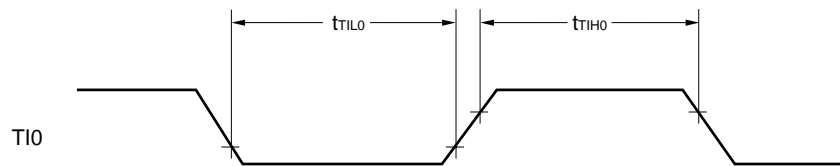
AC Timing Test Point (Excluding X1, XT1 Input)



Clock Timing

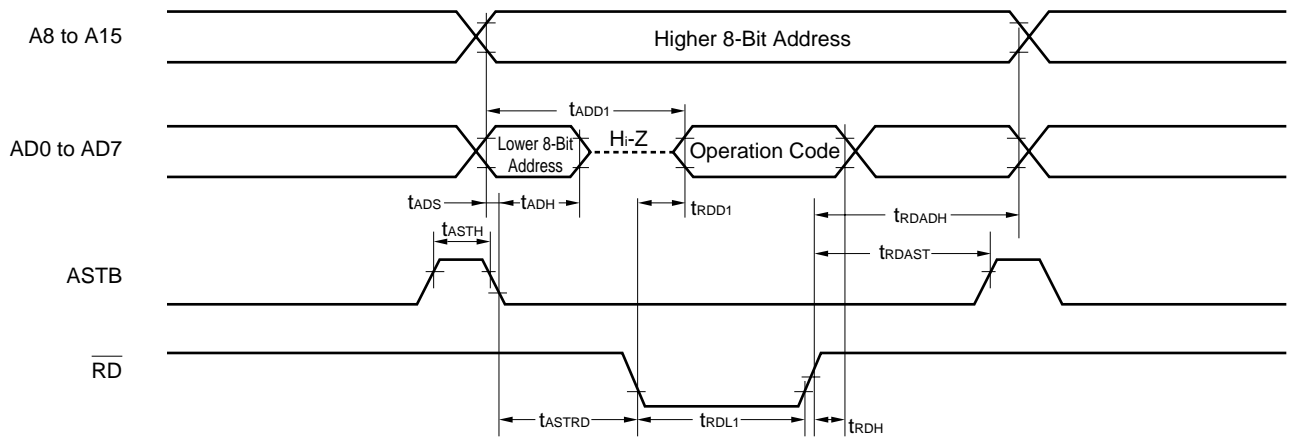


TI Timing

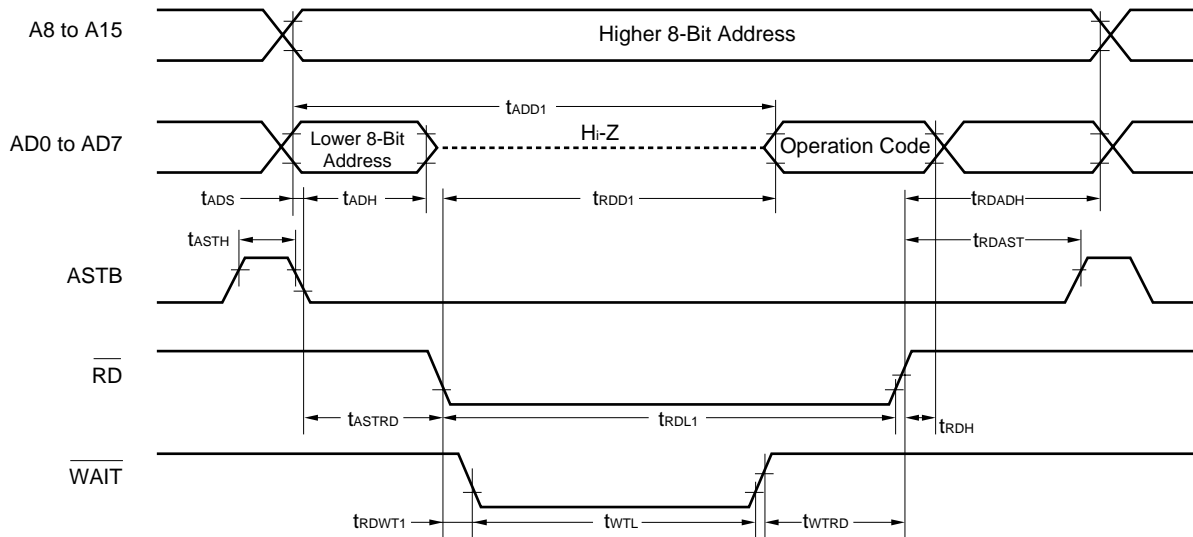


Read/Write Operation

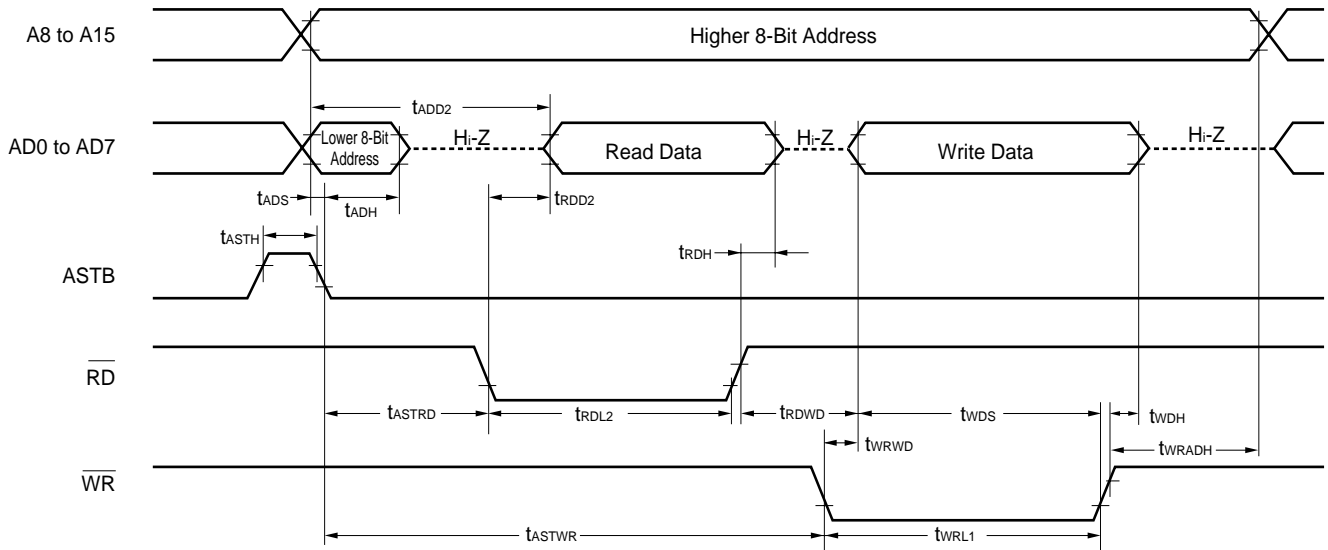
External fetch (No wait):



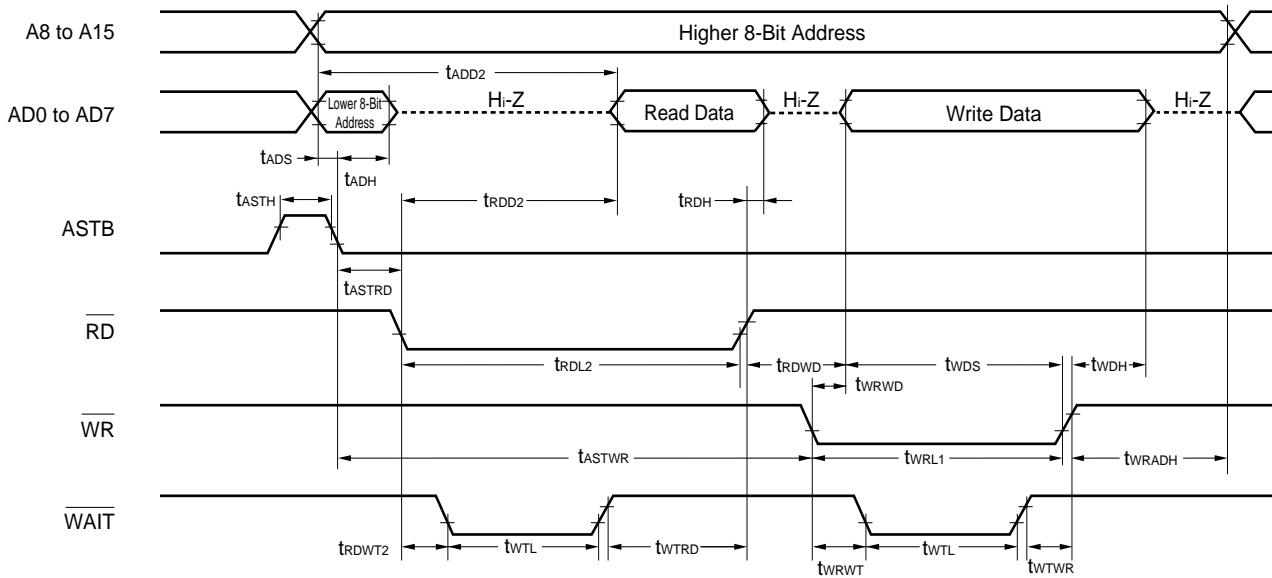
External fetch (Wait insertion):



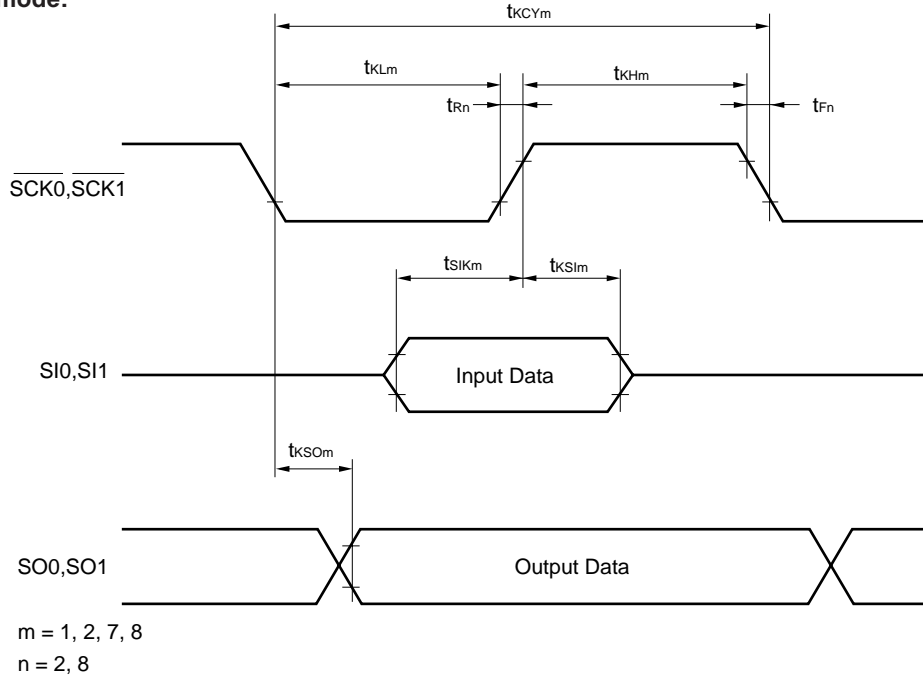
External data access (No wait):



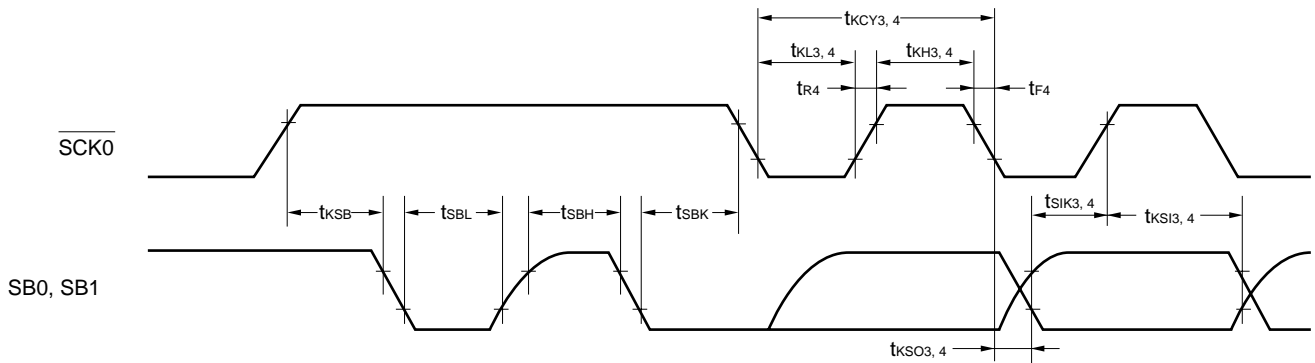
External data access (Wait insertion):



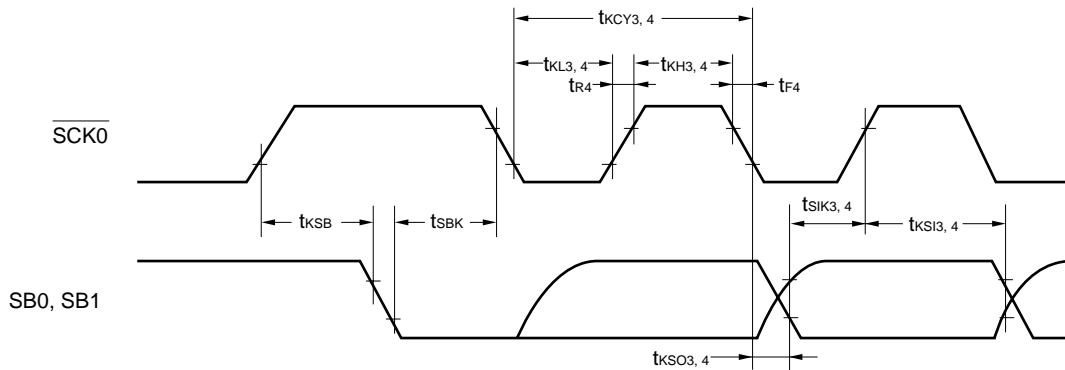
Serial Transfer Timing
3-wire serial I/O mode:



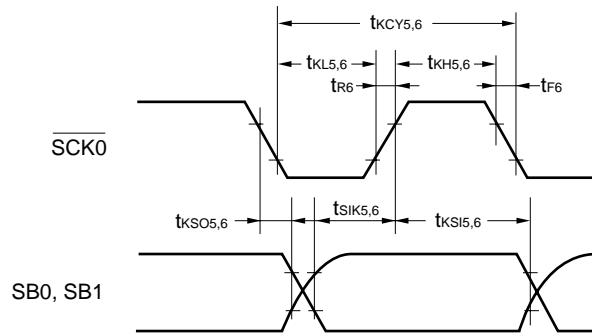
SBI mode (Bus release signal transfer):



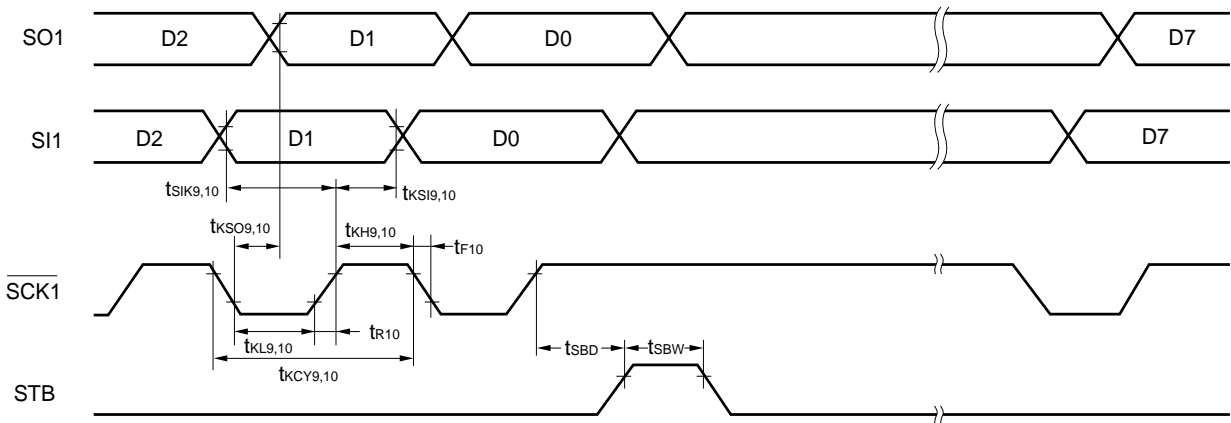
SBI Mode (command signal transfer):



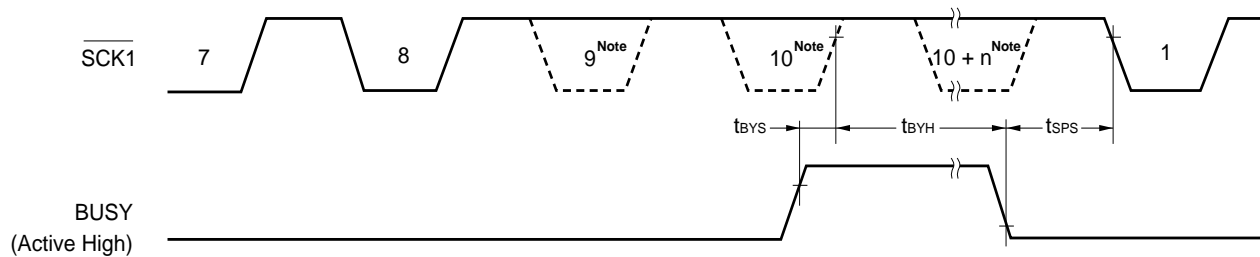
2-wire serial I/O mode:



3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (busy processing):



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

A/D converter characteristics ($T_A = -40$ to $+85$ °C, $AV_{DD} = V_{DD} = 1.8$ to 5.5 V, $AV_{SS} = V_{SS} = 0$ V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error Note		$2.7\text{ V} \leq AV_{REF} \leq AV_{DD}$			0.6	%
		$1.8\text{ V} \leq AV_{REF} < 2.7\text{ V}$			1.4	%
Conversion time	t_{CONV}	$2.0\text{ V} \leq AV_{DD} \leq 5.5\text{ V}$	19.1		200	μs
		$1.8\text{ V} \leq AV_{DD} < 2.0\text{ V}$	38.2		200	μs
Sampling time	t_{SAMP}		$24/f_x$			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
AV_{REF} resistance	RA_{IREF}		4	14		kΩ

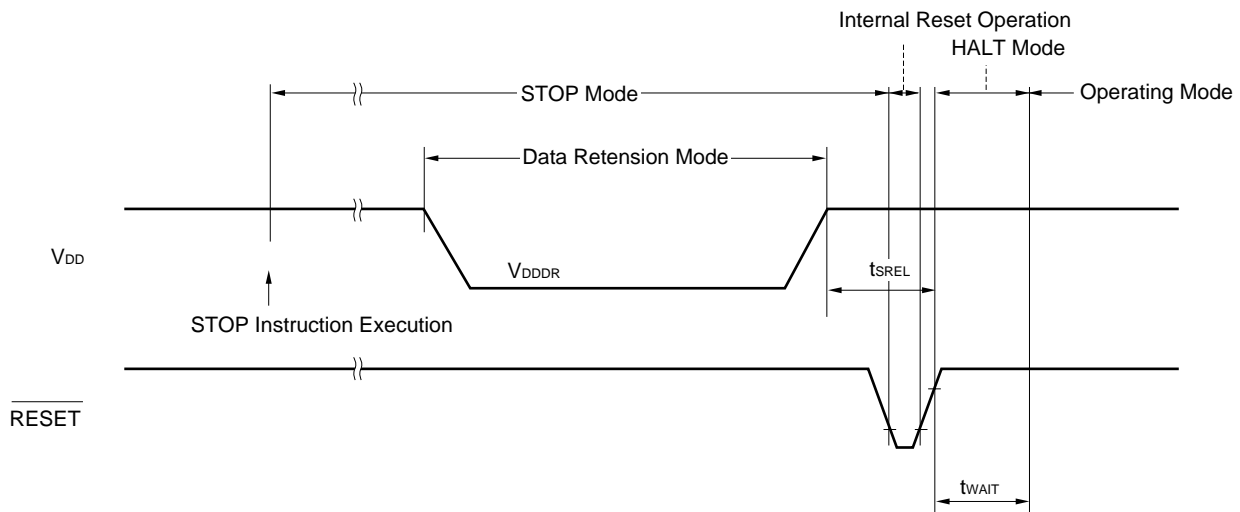
Note Overall error excluding quantization error ($\pm 1/2$ LSB). It is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics ($T_A = -40$ to $+85$ °C)

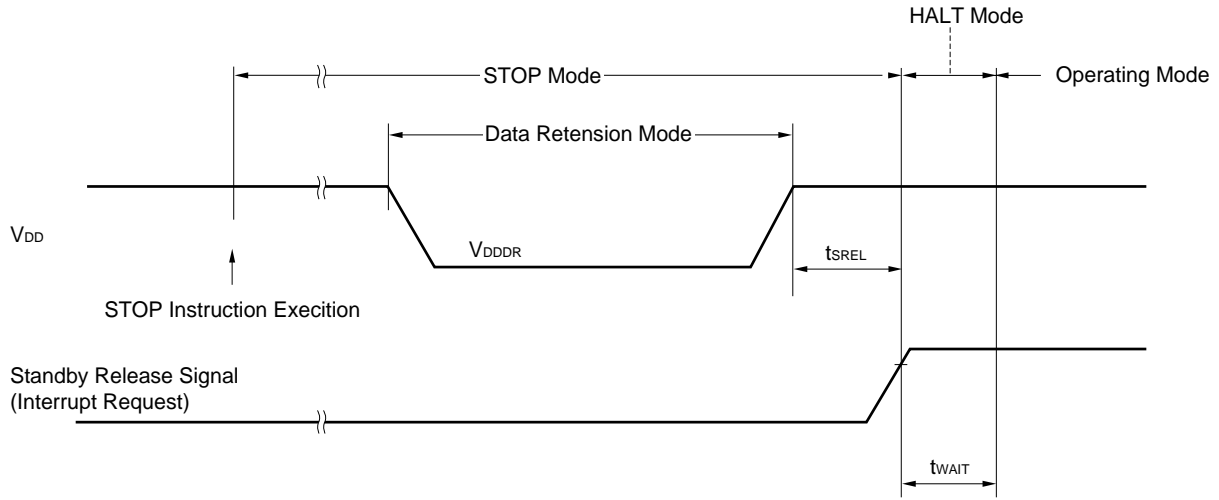
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Data retention supply current	I_{DDDR}	$V_{DDDR} = 1.8\text{ V}$ Subsystem clock stop and feedback resistor disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by \overline{RESET}		$2^{18}/f_x$		ms
		Release by interrupt request		Note		ms

Note In combination with bit 0 to bit 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of $2^{13}/f_x$ and $2^{15}/f_x$ to $2^{18}/f_x$ is possible.

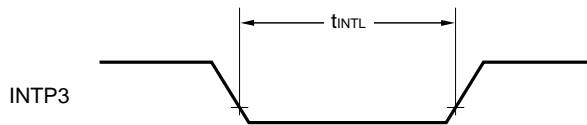
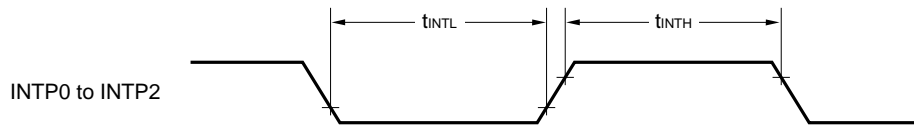
Data Retention Timing (STOP Mode Release by \overline{RESET})



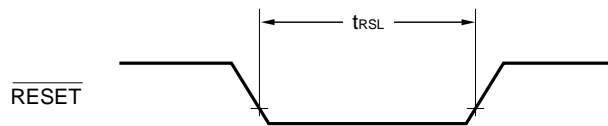
Data Retention Timing (Standby Release Signal : STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing

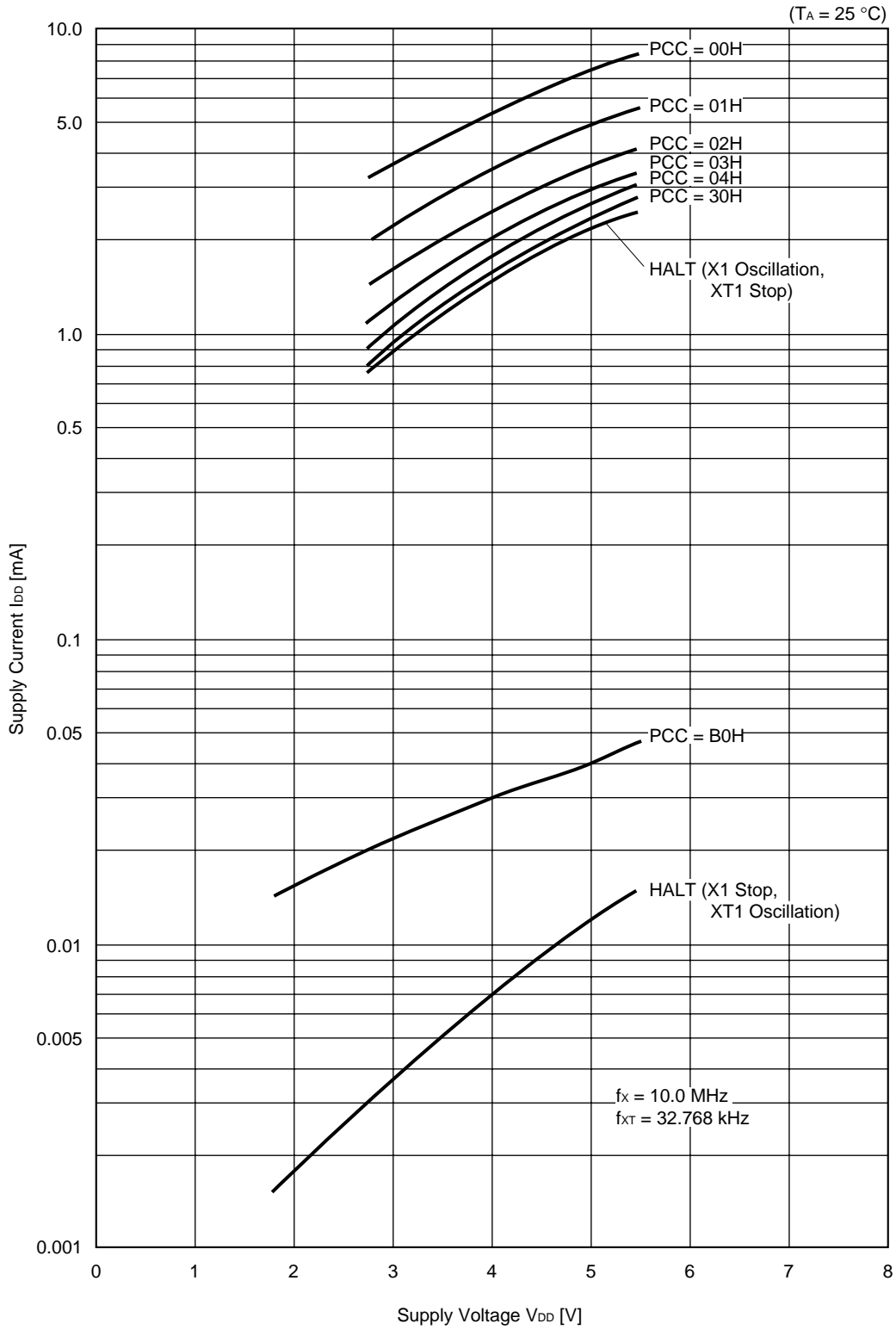


\overline{RESET} Input Timing



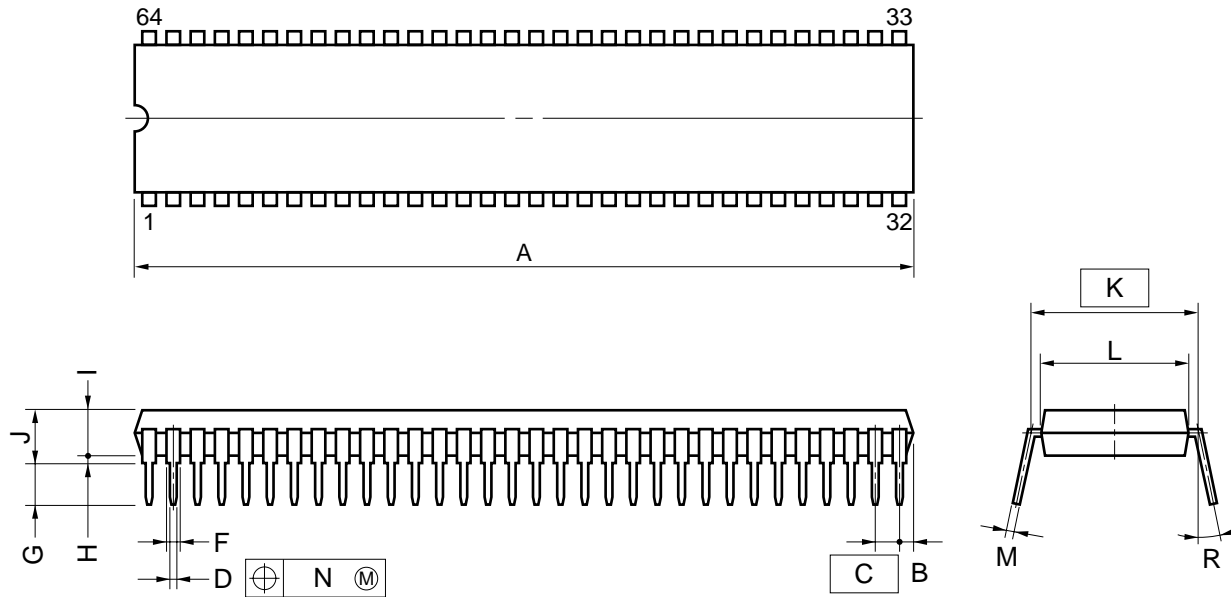
12. CHARACTERISTIC CURVE (REFERENCE VALUES)

I_{DD} vs V_{DD} (Main System Clock: 10.0 MHz)



13. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTE

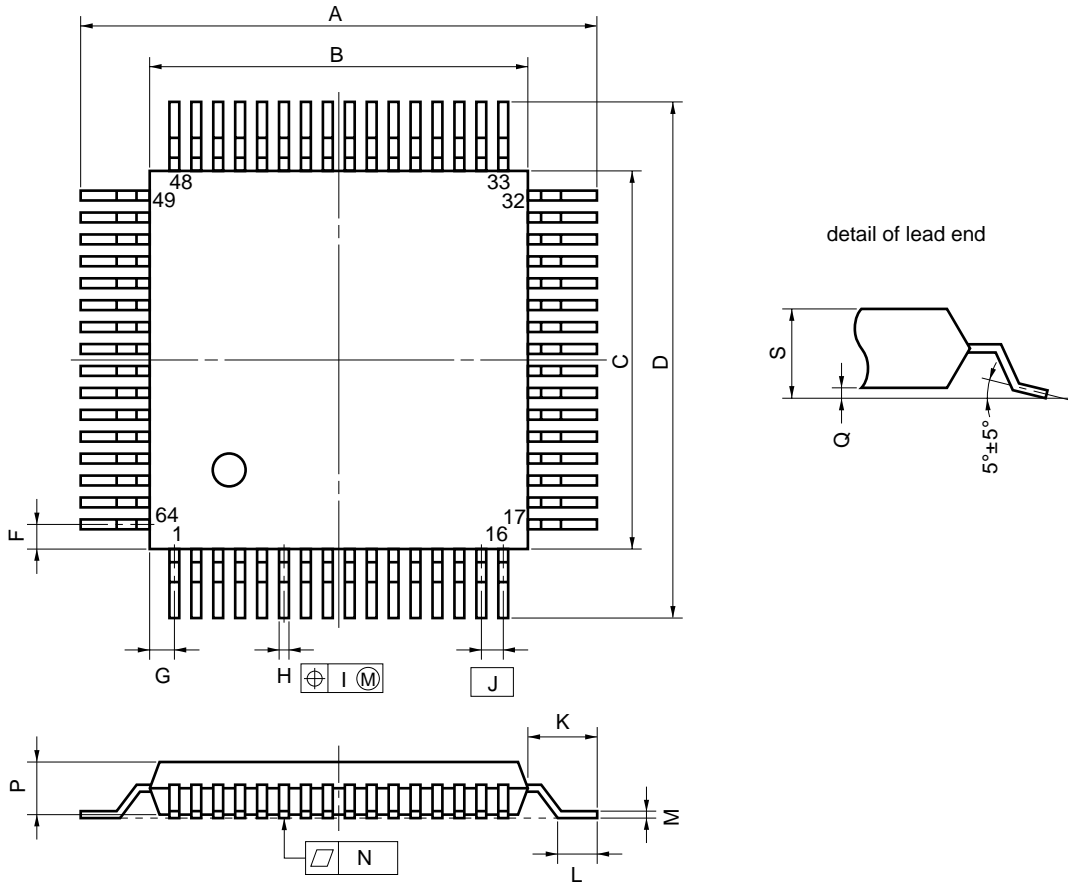
- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 ^{+0.004} _{-0.005}
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

Remark Dimensions and materials of ES products are the same as those of mass-production products.

64 PIN PLASTIC QFP (□14)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

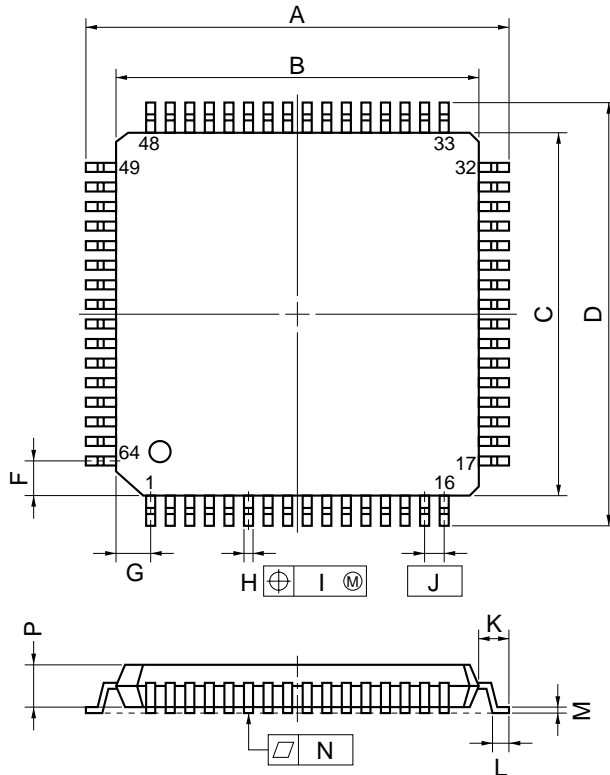
P64GC-80-AB8-2

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	0.551 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	0.014 ^{+0.004} _{-0.005}
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

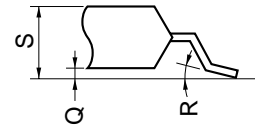
Remark Dimensions and materials of ES products are the same as those of mass-production products.

Phase-out/Discontinued

64 PIN PLASTIC LQFP (□12)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.8±0.4	0.583±0.016
B	12.0±0.2	0.472 ^{+0.009} _{-0.008}
C	12.0±0.2	0.472 ^{+0.009} _{-0.008}
D	14.8±0.4	0.583±0.016
F	1.125	0.044
G	1.125	0.044
H	0.30±0.10	0.012 ^{+0.004} _{-0.005}
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.4±0.2	0.055±0.008
L	0.6±0.2	0.024 ^{+0.008} _{-0.009}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	1.4	0.055
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P64GK-65-8A8-1

Remark Dimensions and materials of ES products are the same as those of mass-production products.

14. RECOMMENDED SOLDERING CONDITIONS

The μPD78011F/78012F/78013F/78014F/78015F/78016F/78018F should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact our salespersonnel.

Table 14-1. Surface Mounting Type Soldering Conditions (1/2)

- (1) μPD78011FGC-xxx-AB8: 64-Pin Plastic QFP (14 × 14 mm)
- μPD78012FGC-xxx-AB8: 64-Pin Plastic QFP (14 × 14 mm)
- μPD78013FGC-xxx-AB8: 64-Pin Plastic QFP (14 × 14 mm)
- μPD78014FGC-xxx-AB8: 64-Pin Plastic QFP (14 × 14 mm)
- μPD78015FGC-xxx-AB8: 64-Pin Plastic QFP (14 × 14 mm)
- μPD78016FGC-xxx-AB8: 64-Pin Plastic QFP (14 × 14 mm)
- ★ μPD78018FGC-xxx-AB8: 64-Pin Plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Three times max.	IR35-00-3
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Three times max.	VP15-00-3
Wave soldering	Solder bath temperature: 260 °C max. Duration: 10 sec. max. Number of times: Once Preheating temperature: 120 °C max. (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)	—

Caution Use more than one soldering method should be avoided (except in the case of partial heating).

Table 14-1. Surface Mounting Type Soldering Conditions (2/2)

- (2) μPD78011FGK-xxx-8A8 : 64-Pin Plastic LQFP (12 × 12 mm)
- μPD78012FGK-xxx-8A8 : 64-Pin Plastic LQFP (12 × 12 mm)
- μPD78013FGK-xxx-8A8 : 64-Pin Plastic LQFP (12 × 12 mm)
- μPD78014FGK-xxx-8A8 : 64-Pin Plastic LQFP (12 × 12 mm)
- μPD78015FGK-xxx-8A8 : 64-Pin Plastic LQFP (12 × 12 mm)
- μPD78016FGK-xxx-8A8 : 64-Pin Plastic LQFP (12 × 12 mm)
- ★ μPD78018FGK-xxx-8A8 : 64-Pin Plastic LQFP (12 × 12 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Twice max., Number of days: 7 days Note (after that, 125 °C prebaking for 10 hours is necessary.) < Precautions > (1) Start the second reflow after the device temperature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	IR35-107-2
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Twice max., Number of days: 7 days Note (after that, 125 °C prebaking for 10 hours is necessary.) < Precautions > (1) Start the second reflow after the device temperature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	VP15-107-2
Wave soldering	Solder bath temperature: 260 °C max. Duration: 10 sec. max. Number of times: Once, Preheating temperature: 120 °C max. (Package surface temperature), Number of days: 7 days Note (after that, 125 °C prebaking for 10 hours is necessary.)	WS60-107-1
Partial heating	Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)	—

Note The number of days the device can be stored at 25 °C, 65% RH MAX. after the dry pack has been opened.

Caution Use more than one soldering method should be avoided (except in the case of partial heating).

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Table 14-2. Insertion Type Soldering Conditions

- μPD78011FCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)**
- μPD78012FCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)**
- μPD78013FCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)**
- μPD78014FCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)**
- μPD78015FCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)**
- μPD78016FCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)**
- μPD78018FCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)**

★

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder bath temperature: 260°C max., Duration: 10 sec. max.
Partial heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per pin)

Caution Wave soldering is only for the lead part in order that jet solder can not contact with the chip directly.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78018F subseries.

Language Processing Software

RA78K/0 Notes 1, 2, 3, 4	78K/0 series common assembler package
CC78K/0 Notes 1, 2, 3, 4	78K/0 series common C compiler package
DF78014 Notes 1, 2, 3, 4	Device file common to μPD78014 subseries
CC78K/0-L Notes 1, 2, 3, 4	78K/0 series common C compiler library source file

PROM Writing Tools

PG-1500	PROM programmer
PA-78P014CW PA-78P018GC PA-78P018GK PA-78P018KK-S	Programmer adapter connected to PG-1500
PG-1500 controller Notes 1, 2	PG-1500 control program

Debugging Tool

IE-78000-R	78K/0 series common in-circuit emulator
★ IE-78000-R-A	78K/0 series common in-circuit emulator (for integrated debugger)
IE-78000-R-BK	78K/0 series common break board
IE-78014-R-EM-A	μPD78018F and 78018FY subseries evaluation emulation board (V _{DD} = 3.0 to 6.0 V)
★ IE-78000-R-SV3	Interface adapter and cable when an EWS is used as the host machine (for IE-78000R-A)
★ IE-70000-98-IF-B	Interface adapter when PC-9800 series (except notebook PC) is used as the host machine (for IE-78000-R-A)
★ IE-70000-98N-IF	Interface adapter and cable when PC-9800 series notebook PC is used as the host machine (for IE-78000-R-A)
★ IE-70000-PC-IF-B	Interface adapter when IBM PC/AT™ is used as the host machine (for IE-78000-R-A)
EP-78240CW-R EP-78240GC-R	Emulation probe common to μPD78244 subseries
EV-78012GK-R	μPD78018F subseries emulation probe
EV-9200GC-64	Socket to be mounted on target system board created for the 64-pin plastic QFP (GC-AB8 type)
★ TGC-064SBW	Conversion adapter to be mounted on a target system board made for 64-pin plastic QFP (GK-8A8 type) TGC-100SDW is a product from Tokyo Eletech Corp. (TEL (03) 5295-1661) When purchasing this product, please consult with our sales offices.
EV-9900	Tools for removing μPD78P018FKK-S from EV-9200GC-64
SM78K0 Notes 5, 6, 7	78K/0 series common system simulator
★ ID78K0 Notes 4, 5, 6, 7	IE-78000-R-A integrated debugger
SD78K/0 Notes 1, 2	IE-78000-R screen debugger
DF78014 Notes 1, 2, 4, 5, 6, 7	Device file common to μPD78014 subseries

Real-Time OS

RX78K/0 Notes 1, 2, 3, 4	78K/0 series real-time OS
MX78K0 Notes 1, 2, 3, 4	78K/0 series OS

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Fuzzy Inference Development Support System

FE9000 Note 1 /FE9200 Note 6	Fuzzy knowledge data creation tool
FT9080 Note 1 /FT9085 Note 2	Translator
FI78K0 Notes 1, 2	Fuzzy inference module
FD78K0 Notes 1, 2	Fuzzy inference debugger

Notes 1. PC-9800 series (MS-DOS™) based

2. IBM PC/AT and compatible (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 series 300™ (HP-UX™) based
4. HP9000 series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS4800 series (EWS-UX/V) based
5. PC-9800 series (MS-DOS + Windows™) based
6. IBM PC/AT and compatible (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based

Remarks 1. For development tools manufactured by a third party, refer to the **78K/0 Series Selection Guide (U11126E)**.

2. RA78K/0, CC78K/0, SM78K0, ID78K0, SD78K/0, and RX78K/0 are used in combination with DF78014.

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

	Document Name	Document No.	
		Japanese	English
★	μPD78018F, 78018FY Subseries User's Manual	U10659J	U10659E
★	78K/0 Series User's Manual - Instruction	U12326J	IEU-1372
★	78K/0 Series Instruction Table	U10903J	—
★	78K/0 Series Instruction Set	U10904J	—
	μPD78018F Subseries Special Function Register Table	IEM-5594	—
	78K/0 Series Application Note	Fundamental (I)	IEA-715
		Floating-Point Arithmetic Program	IEA-718
		IEA-1288	IEA-1289

Development Tools Documents (User's Manual) (1/2)

	Document Name	Document No.	
		Japanese	English
	RA78K Series Assembler Package	Operation	EEU-809
		Language	EEU-815
	RA78K Series Structured Assembler Preprocessor	EEU-817	EEU-1402
★	RA78K0 Assembler Package	Operation	U11802J
		Assembly Language	U11801J
		Structured Assembly Language	U11789J
	CC78K Series C Compiler	Operation	EEU-656
		Language	EEU-655
★	CC78K0 C Compiler	Operation	U11517J
		Language	U11518J
	CC78K/0 C Compiler Application Note	Programming Know-how	EEA-618
★	CC78K Series Library Source File	U12322J	—
★	PG-1500 PROM Programmer	U11940J	EEU-1335
	PG-1500 Controller PC-9800 Series (MS-DOS) Based	EEU-704	EEU-1291
	PG-1500 Controller IBM PC Series (PC DOS) Based	EEU-5008	U10540E
★	IE-78000-R	U11376J	U11376E
★	E-78000-R-A	U10057J	U10057E
	IE-78000-R-BK	EEU-867	EEU-1427
	IE-78014-R-EM-A	EEU-962	U10418E
	EP-78240	EEU-986	EEU-1513
	EP-78012GK-R	EEU-5012	EEU-1538
	SM78K0 System Simulator	Reference	U10181J
			U10181E

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for designing, etc.

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Development Tools Documents (User's Manual) (2/2)

Document Name		Document No.	
		Japanese	English
★ SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
★ ID78K0 Integrated Debugger EWS Based	Reference	U11151J	—
★ ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
★ ID78K0 Integrated Debugger Windows Based	Guide	U11649J	U11649E
★ SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) Based	Introduction	EEU-852	U10539E
	Reference	U10952J	—
★ SD78K/0 Screen Debugger IBM PC/AT (PC DOS) Based	Introduction	EEU-5024	EEU-1414
	Reference	U11279J	U11279E

Embedded Software Documents (User's Manual)

Document Name		Document No.	
		Japanese	English
★ 78K/0 Series Real-Time OS	Fundamental	U11537J	U11537E
	Installation	U11536J	U11536E
★ 78K/0 Series OS MX78K0	Fundamental	U12257J	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System - Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System - Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System - Fuzzy Inference Debugger		EEU-921	EEU-1458

★ **Other Documents**

Document Name		Document No.	
		Japanese	English
IC Package Manual		C10943X	
Semiconductor Device Mounting Technology Manual		C11535J	C10535E
Quality Grades on NEC Semiconductor Device		C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System		C10983J	C10983E
Electrostatic Discharge (ESD) Test		MEM-539	—
Guide to Quality Assurance for Semiconductor Device		C11893J	MEI-1202
Guide for Products Related to Microcomputer: Other Companies		U11416J	—

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for designing, etc.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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NEC Electronics Inc. (U.S.)

Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH

Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.

Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

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Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

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Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

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Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

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Spain Office
Madrid, Spain
Tel: 01-504-2787
Fax: 01-504-2860

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Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.

Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.

Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.

United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.

Taipei, Taiwan
Tel: 02-719-2377
Fax: 02-719-5951

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Cumbica-Guarulhos-SP, Brasil
Tel: 011-6465-6810
Fax: 011-6465-6829

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