

MEMORY

CMOS

2 × 512 K × 16 BIT

SYNCHRONOUS DYNAMIC RAM

MB81F161622C-60/-70/-80/-80L

CMOS 2-Bank × 524,288-Word × 16 Bit Synchronous Dynamic Random Access Memory

■ DESCRIPTION

The Fujitsu MB81F161622C is a CMOS Synchronous Dynamic Random Access Memory (SDRAM) containing 16,777,216 memory cells accessible in an 16-bit format. The MB81F161622C features a fully synchronous operation referenced to a positive edge clock whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence. The MB81F161622C SDRAM is designed to reduce the complexity of using a standard dynamic RAM (DRAM) which requires many control signal timing constraints, and may improve data bandwidth of memory as much as 5 times more than a conventional DRAM.

The MB81F161622C is ideally suited for laser printers, high resolution graphic adapters, accelerators and other applications where an extremely large memory and bandwidth are required and where a simple interface is needed.

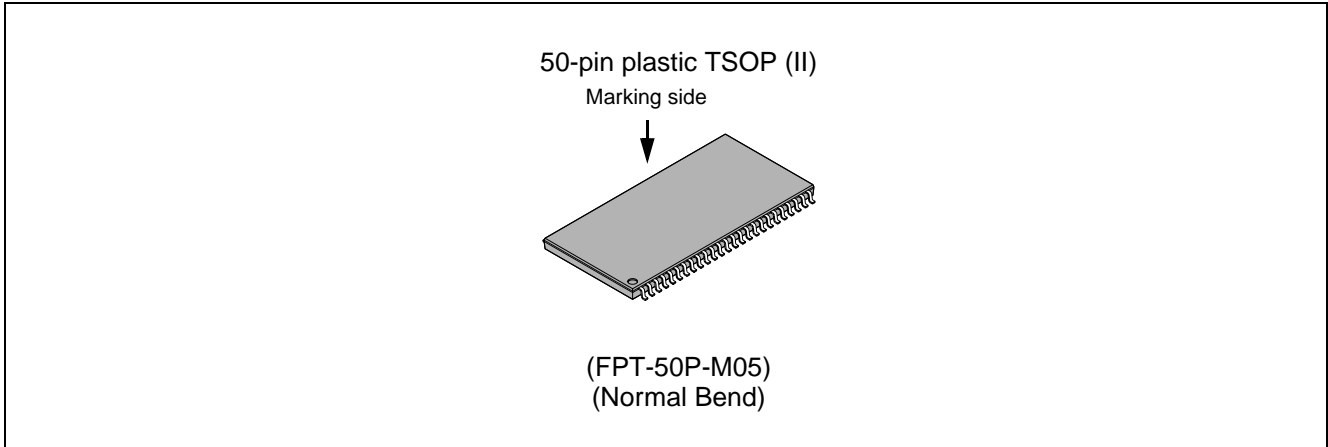
■ PRODUCT LINE & FEATURES

| Parameter | MB81F161622C | | | Reference Spec (100MHz @CL=3) |
|-----------------------------------------------|--------------------|--------------------|--------------------|----------------------------------|
| | -60 | -70 | -80/-80L | |
| CL - t _{RCD} - t _{RP} | 3 - 3 - 3 clk min. | 3 - 3 - 3 clk min. | 3 - 3 - 3 clk min. | 3 - 3 - 3 clk min. |
| Clock Frequency (CL = 3) | 167 MHz max. | 143 MHz max. | 125 MHz max. | 100 MHz max. |
| Burst Mode Cycle Time (CL = 3) | 6.0 ns min. | 7.0 ns min. | 8.0 ns min. | 10 ns min. |
| Access Time From Clock (CL = 3) | 5.5 ns max. | 6 ns max. | 6 ns max. | 6 ns max. |
| Operating Current | 150 mA max. | 130 mA max. | 110 mA max. | 90 mA max. |
| Power Down Mode Current (I _{CC2P}) | 1 mA max. | 1 mA max. | 1 mA max. | 1 mA max. |
| Self Refresh Mode Current (I _{CC6}) | 1 mA max. | 1 mA max. | 1 mA / 400 μA max. | 1 mA max. |

- Single +3.3 V Supply: +0.3 V / -0.15 V tolerance (-60) ±0.3 V tolerance (-70/-80/-80L)
- LVTTTL compatible I/O interface
- 4 K refresh cycles every 64 ms
- Dual banks operation
- Burst read/write operation and burst read/single write operation capability
- Byte control by DQMU/DQML
- Programmable burst type, burst length, and CAS latency
- Auto-and Self-refresh (every 15.6 μs)
- CKE power down mode
- Output Enable and Input Data Mask
- 167 MHz/143MHz/125 MHz clock frequency

MB81F161622C-60/-70/-80/-80L

■ PACKAGE

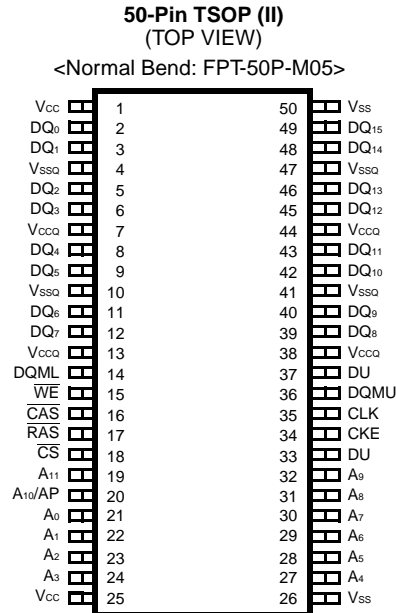


Package and Ordering Information

- 50-pin plastic (400 mil) TSOP-II with normal bend leads, order as MB81F161622C-xxFN (Std. power)
/-xxLFN (Low power)

MB81F161622C-60/-70/-80/-80L

PIN ASSIGNMENTS AND DESCRIPTIONS



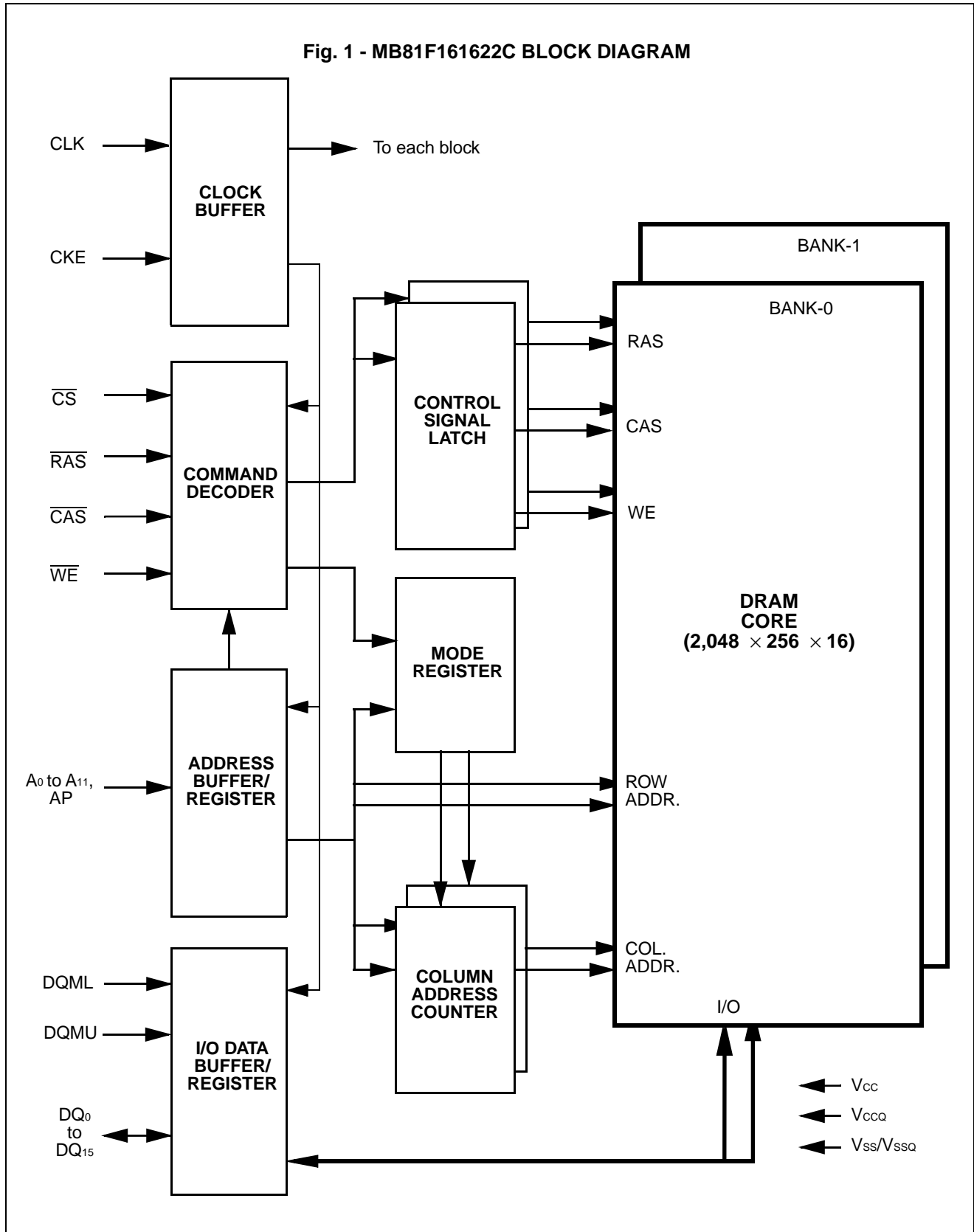
(Marking side)

| Pin Number | Symbol | Description |
|----------------------------------------------------------|--------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 7, 13, 25, 38, 44 | V _{cc} , V _{CCQ} | Supply Voltage |
| 2, 3, 5, 6, 8, 9, 11, 12, 39, 40, 42, 43, 45, 46, 48, 49 | DQ ₀ to DQ ₁₅ | Data I/O <ul style="list-style-type: none"> • Lower Byte: DQ₀ to DQ₇ • Upper Byte: DQ₈ to DQ₁₅ |
| 4, 10, 26, 41, 47, 50 | V _{SS} , V _{SSQ} * | Ground |
| 33, 37 | DU | Don't use (leave open) |
| 15 | WE | Write Enable |
| 16 | CAS | Column Address Strobe |
| 17 | RAS | Row Address Strobe |
| 18 | CS | Chip Select |
| 19 | A ₁₁ (BA) | Bank Select |
| 20 | AP | Auto Precharge Enable |
| 20, 21, 22, 23, 24, 27, 28, 29, 30, 31, 32 | A ₀ to A ₁₀ | Address Input <ul style="list-style-type: none"> • Row: A₀ to A₁₀ • Column: A₀ to A₇ |
| 34 | CKE | Clock Enable |
| 35 | CLK | Clock Input |
| 14, 36 | DQML, DQMU | Input Mask/Output Enable |

* : These pins are connected internally in the chip.

MB81F161622C-60/-70/-80/-80L

■ BLOCK DIAGRAM



MB81F161622C-60/-70/-80/-80L

■ FUNCTIONAL TRUTHAL TABLE (Note *1)

COMMAND TRUTH TABLE Notes *2,*3, and *4

| Function | Notes | Symbol | CKE | | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | A ₁₁ (BA) | A ₁₀ (AP) | A ₉ , A ₈ | A ₇ to A ₀ |
|----------------------------------|-------|--------|-----|---|-----------------|------------------|------------------|-----------------|-------------------------|-------------------------|---------------------------------|-------------------------------------|
| | | | n-1 | n | | | | | | | | |
| Device Deselect | *5 | DESL | H | X | H | X | X | X | X | X | X | X |
| No Operation | *5 | NOP | H | X | L | H | H | H | X | X | X | X |
| Burst Stop | | BST | H | X | L | H | H | L | X | X | X | X |
| Read | *6 | READ | H | X | L | H | L | H | V | L | X | V |
| Read with Auto-precharge | *6 | READA | H | X | L | H | L | H | V | H | X | V |
| Write | *6 | WRIT | H | X | L | H | L | L | V | L | X | V |
| Write with Auto-precharge | *6 | WRITA | H | X | L | H | L | L | V | H | X | V |
| Bank Active (\overline{RAS}) | *7 | ACTV | H | X | L | L | H | H | V | V | V | V |
| Precharge Single Bank | | PRE | H | X | L | L | H | L | V | L | X | X |
| Precharge All Banks | | PALL | H | X | L | L | H | L | X | H | X | X |
| Mode Register Set | *8,*9 | MRS | H | X | L | L | L | L | L | L | V | V |

- Notes:**
- *1. V = Valid, L = Logic Low, H = Logic High, X = either L or H
 - *2. All commands assume no CSUS command on previous rising edge of clock.
 - *3. All commands are assumed to be valid state transitions.
 - *4. All inputs are latched on the rising edge of clock.
 - *5. NOP and DESL commands have the same effect on the part. Unless specifically noted, NOP will represent both NOP and DESL command in later descriptions.
 - *6. READ, READA, WRIT, and WRITA commands should only be issued after the corresponding bank has been activated (ACTV command). Refer to STATE DIAGRAM.
 - *7. ACTV command should only be asserted after corresponding bank has been precharged (PRE or PALL command).
 - *8. Required after power up. Refer to POWER-UP INITIALIZATION in page 19.
 - *9. MRS command should only be issued after all banks have been precharged (PRE or PALL command). Refer to STATE DIAGRAM.

MB81F161622C-60/-70/-80/-80L

DQM TRUTH TABLE

| Function | Command | CKE | | DQML | DQMU |
|-----------------------------------------|---------|-----|---|------|------|
| | | n-1 | n | | |
| Data Write/Output Enable for Lower Byte | ENBL L | H | X | L | X |
| Data Write/Output Enable for Upper Byte | ENBL U | H | X | X | L |
| Data Mask/Output Disable for Lower Byte | MASK L | H | X | H | X |
| Data Mask/Output Disable for Upper Byte | MASK U | H | X | X | H |

CKE TRUTH TABLE

| Current State | Function | Notes | Symbol | CKE | | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | A ₁₁ (BA) | A ₁₀ (AP) | A ₉ to A ₀ |
|--------------------|--------------------------|-------|--------|-----|---|-----------------|------------------|------------------|-----------------|----------------------|----------------------|----------------------------------|
| | | | | n-1 | n | | | | | | | |
| Bank Active | Clock Suspend Mode Entry | *1 | CSUS | H | L | X | X | X | X | X | X | X |
| Any Except to Idle | Clock Suspend Continue | *1 | | L | L | X | X | X | X | X | X | X |
| Clock Suspend | Clock Suspend Mode Exit | | | L | H | X | X | X | X | X | X | X |
| Idle | Auto-refresh Command | *2 | REF | H | H | L | L | L | H | X | X | X |
| Idle | Self-refresh Entry | *2,*3 | SELF | H | L | L | L | L | H | X | X | X |
| Self-refresh | Self-refresh Exit | | SELF | L | H | L | H | H | H | X | X | X |
| | | | | L | H | H | X | X | X | X | X | X |
| Idle | Power Down Entry | *3 | PD | H | L | L | H | H | H | X | X | X |
| | | | | H | L | H | X | X | X | X | X | X |
| Power Down | Power Down Exit | | | L | H | L | H | H | H | X | X | X |
| | | | | L | H | H | X | X | X | X | X | X |

- Notes:** *1. The CSUS command requires that at least one bank is active. Refer to STATE DIAGRAM. NOP or DESL commands should only be issued after CSUS and PRE (or PALL) commands asserted at same time.
- *2. REF and SELF commands should only be issued after all banks have been precharged (PRE or PAL command). Refer to STATE DIAGRAM.
- *3. Self and PD commands should only be issued after the last data have been appeared on DQ.

MB81F161622C-60/-70/-80/-80L

OPERATION COMMAND TABLE (Applicable to single bank) Note *1

| Current State | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | Addr | Command | Function | Notes |
|---------------|-----------------|------------------|------------------|-----------------|------------|------------|-------------------------------------------|-------|
| Idle | H | X | X | X | X | DESL | NOP | |
| | L | H | H | H | X | NOP | NOP | |
| | L | H | H | L | X | BST | NOP | |
| | L | H | L | H | BA, CA, AP | READ/READA | Illegal | *2 |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Illegal | *2 |
| | L | L | H | H | BA, RA | ACTV | Bank Active after t_{RCD} | |
| | L | L | H | L | BA, AP | PRE/PALL | NOP | |
| | L | L | L | H | X | REF/SELF | Auto-refresh or Self-refresh | *3,*6 |
| | L | L | L | L | MODE | MRS | Mode Register Set (Idle after t_{RSC}) | *3,*7 |
| Bank Active | H | X | X | X | X | DESL | NOP | |
| | L | H | H | H | X | NOP | NOP | |
| | L | H | H | L | X | BST | NOP | |
| | L | H | L | H | BA, CA, AP | READ/READA | Begin Read; Determine AP | |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Begin Write; Determine AP | |
| | L | L | H | H | BA, RA | ACTV | Illegal | *2 |
| | L | L | H | L | BA, AP | PRE/PALL | Precharge; Determine Precharge Type | |
| | L | L | L | H | X | REF/SELF | Illegal | |
| | L | L | L | L | MODE | MRS | Illegal | |

(Continued)

MB81F161622C-60/-70/-80/-80L

(Continued)

| Current State | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | Addr | Command | Function | Notes |
|---------------|-----------------|------------------|------------------|-----------------|------------|------------|-------------------------------------------------------------|-------|
| Read | H | X | X | X | X | DESL | NOP (Continue Burst to End → Bank Active) | |
| | L | H | H | H | X | NOP | NOP (Continue Burst to End → Bank Active) | |
| | L | H | H | L | X | BST | Burst Stop → Bank Active | |
| | L | H | L | H | BA, CA, AP | READ/READA | Terminate Burst, New Read; Determine AP | |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Terminate Burst, Start Write; Determine AP | *4 |
| | L | L | H | H | BA, RA | ACTV | Illegal | *2 |
| | L | L | H | L | BA, AP | PRE/PALL | Terminate Burst, Precharge; → Idle Determine Precharge Type | |
| | L | L | L | H | X | REF/SELF | Illegal | |
| | L | L | L | L | MODE | MRS | Illegal | |
| Write | H | X | X | X | X | DESL | NOP (Continue Burst to End → Bank Active) | |
| | L | H | H | H | X | NOP | NOP (Continue Burst to End → Bank Active) | |
| | L | H | H | L | X | BST | Burst Stop → Bank Active | |
| | L | H | L | H | BA, CA, AP | READ/READA | Terminate Burst, Start Read; Determine AP | *4 |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Terminate Burst, New Write; Determine AP | |
| | L | L | H | H | BA, RA | ACTV | Illegal | *2 |
| | L | L | H | L | BA, AP | PRE/PALL | Terminate Burst, Precharge; Determine Precharge Type | |
| | L | L | L | H | X | REF/SELF | Illegal | |
| | L | L | L | L | MODE | MRS | Illegal | |

(Continued)

MB81F161622C-60/-70/-80/-80L

(Continued)

| Current State | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | Addr | Command | Function | Notes |
|---------------------------|-----------------|------------------|------------------|-----------------|------------|------------|------------------------------------------------|-------|
| Read with Auto-precharge | H | X | X | X | X | DESL | NOP (Continue Burst to End → Precharge → Idle) | |
| | L | H | H | H | X | NOP | NOP (Continue Burst to End → Precharge → Idle) | |
| | L | H | H | L | X | BST | Illegal | |
| | L | H | L | H | BA, CA, AP | READ/READA | Illegal | *2 |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Illegal | *2 |
| | L | L | H | H | BA, RA | ACTV | Illegal | *2 |
| | L | L | H | L | BA, AP | PRE/PALL | Illegal | *2 |
| | L | L | L | H | X | REF/SELF | Illegal | |
| | L | L | L | L | MODE | MRS | Illegal | |
| Write with Auto-precharge | H | X | X | X | X | DESL | NOP (Continue Burst to End → Precharge → Idle) | |
| | L | H | H | H | X | NOP | NOP (Continue Burst to End → Precharge → Idle) | |
| | L | H | H | L | X | BST | Illegal | |
| | L | H | L | H | BA, CA, AP | READ/READA | Illegal | *2 |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Illegal | *2 |
| | L | L | H | H | BA, RA | ACTV | Illegal | *2 |
| | L | L | H | L | BA, AP | PRE/PALL | Illegal | *2 |
| | L | L | L | H | X | REF/SELF | Illegal | |
| | L | L | L | L | MODE | MRS | Illegal | |

(Continued)

MB81F161622C-60/-70/-80/-80L

(Continued)

| Current State | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | Addr | Command | Function | Notes |
|-----------------|-----------------|------------------|------------------|-----------------|------------|------------|------------------------------------|-------|
| Precharge | H | X | X | X | X | DESL | NOP (Idle after t_{RP}) | |
| | L | H | H | H | X | NOP | NOP (Idle after t_{RP}) | |
| | L | H | H | L | X | BST | Illegal | |
| | L | H | L | H | BA, CA, AP | READ/READA | Illegal | *2 |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Illegal | *2 |
| | L | L | H | H | BA, RA | ACTV | Illegal | *2 |
| | L | L | H | L | BA, AP | PRE/PALL | NOP (PALL may effect other bank) | *5 |
| | L | L | L | H | X | REF/SELF | Illegal | |
| | L | L | L | L | MODE | MRS | Illegal | |
| Bank Activating | H | X | X | X | X | DESL | NOP (Bank Active after t_{RCD}) | |
| | L | H | H | H | X | NOP | NOP (Bank Active after t_{RCD}) | |
| | L | H | H | L | X | BST | NOP (Bank Active after t_{RCD}) | |
| | L | H | L | H | BA, CA, AP | READ/READA | Illegal | *2 |
| | L | H | L | L | BA, CA, AP | WRIT/WRITA | Illegal | *2 |
| | L | L | H | H | BA, RA | ACTV | Illegal | *2 |
| | L | L | H | L | BA, AP | PRE/PALL | Illegal | *2 |
| | L | L | L | H | X | REF/SELF | Illegal | |
| | L | L | L | L | MODE | MRS | Illegal | |

(Continued)

MB81F161622C-60/-70/-80/-80L

(Continued)

| Current State | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | Addr | Command | Function | Notes |
|-----------------------|-----------------|------------------|------------------|-----------------|------|------------------------------------|-----------------------------|-------|
| Refreshing | H | X | X | X | X | DESL | NOP (Idle after t_{RC}) | |
| | L | H | H | X | X | NOP/BST | NOP (Idle after t_{RC}) | |
| | L | H | L | X | X | READ/READA/ WRIT/WRTA | Illegal | |
| | L | L | H | X | X | ACTV/PRE/ PALL | Illegal | |
| | L | L | L | X | X | REF/SELF/ MRS | Illegal | |
| Mode Register Setting | H | X | X | X | X | DESL | NOP (Idle after t_{RSC}) | |
| | L | H | H | H | X | NOP | NOP (Idle after t_{RSC}) | |
| | L | H | H | L | X | BST | Illegal | |
| | L | H | L | X | X | READ/READA/ WRIT/WRTA | Illegal | |
| | L | L | X | X | X | ACTV/PRE/ PALL/REF/ SELF/MRS | Illegal | |

ABBREVIATIONS:

RA = Row Address BA = Bank Address
 CA = Column Address AP = Auto Precharge

- Notes:**
- *1. All entries assume the CKE was High during the proceeding clock cycle and the current clock cycle. Illegal means don't used command. If used, power up sequence be asserted after power shout down.
 - *2. Illegal to bank in specified state; entry may be legal in the bank specified by BA, depending on the state of that bank.
 - *3. Illegal if any bank is not idle.
 - *4. Must satisfy bus contention, bus turn around, and/or write recovery requirements. Refer to TIMING DIAGRAM - 11 & - 12.
 - *5. NOP to bank precharging or in idle state. May precharge bank specified by BA (and AP).
 - *6. SELF command should only be issued after the last read data have been appeared on DQ.
 - *7. MRS command should only be issued on condition that all DQ are in Hi-Z.

MB81F161622C-60/-70/-80/-80L

COMMAND TRUTH TABLE FOR CKE Note *1

| Current State | CKE _{n-1} | CKE _n | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | Addr | Function | Notes |
|-----------------------|--------------------|------------------|-----------------|------------------|------------------|-----------------|------|----------------------------------------------------------------------------|-------|
| Self-refresh | H | X | X | X | X | X | X | Invalid | |
| | L | H | H | X | X | X | X | Exit Self-refresh (Self-refresh Recovery → Idle after t _{RC}) | |
| | L | H | L | H | H | H | X | Exit Self-refresh (Self-refresh Recovery → Idle after t _{RC}) | |
| | L | H | L | H | H | L | X | Illegal | |
| | L | H | L | H | L | X | X | Illegal | |
| | L | H | L | L | X | X | X | Illegal | |
| | L | L | X | X | X | X | X | NOP (Maintain Self-refresh) | |
| Self-refresh Recovery | L | X | X | X | X | X | X | Invalid | |
| | H | H | H | X | X | X | X | Idle after t _{RC} | |
| | H | H | L | H | H | H | X | Idle after t _{RC} | |
| | H | H | L | H | H | L | X | Illegal | |
| | H | H | L | H | L | X | X | Illegal | |
| | H | H | L | L | X | X | X | Illegal | |
| | H | H | X | X | X | X | X | Illegal | |
| | H | L | X | X | X | X | X | Illegal | *2 |

(Continued)

MB81F161622C-60/-70/-80/-80L

(Continued)

| Current State | CKE _{n-1} | CKE _n | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | Addr | Function | Notes |
|-----------------|--------------------|------------------|-----------------|------------------|------------------|-----------------|------|--------------------------------------|-------|
| Power Down | H | X | X | X | X | X | X | Invalid | |
| | L | H | H | X | X | X | X | Exit Power Down Mode → Idle | |
| | L | H | L | H | H | H | X | Exit Power Down Mode → Idle | |
| | L | L | X | X | X | X | X | NOP (Maintain Power Down Mode) | |
| | L | H | L | L | X | X | X | Illegal | |
| | L | H | L | H | L | X | X | Illegal | |
| Both Banks Idle | H | H | H | X | X | X | MODE | Refer to the Operation Command Table | |
| | H | H | L | H | X | X | MODE | Refer to the Operation Command Table | |
| | H | H | L | L | H | X | MODE | Refer to the Operation Command Table | |
| | H | H | L | L | L | H | X | Auto-refresh | |
| | H | H | L | L | L | L | MODE | Refer to the Operation Command Table | |
| | H | L | H | X | X | X | X | Power Down | |
| | H | L | L | H | H | H | X | Power Down | |
| | H | L | L | H | H | L | X | Illegal | |
| | H | L | L | H | L | X | X | Illegal | |
| | H | L | L | L | H | X | X | Illegal | |
| | H | L | L | L | L | H | X | Self-refresh | *3 |
| | H | L | L | L | L | L | X | Illegal | |
| | L | X | X | X | X | X | X | Invalid | |

(Continued)

MB81F161622C-60/-70/-80/-80L

(Continued)

| Current State | CKE _{n-1} | CKE _n | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | Addr | Function | Notes |
|----------------------------------------|--------------------|------------------|-----------------|------------------|------------------|-----------------|------|--------------------------------------|-------|
| Bank Active Bank Activating Read/Write | H | H | X | X | X | X | X | Refer to the Operation Command Table | |
| | H | L | X | X | X | X | X | Begin Clock Suspend Next Cycle | |
| | L | X | X | X | X | X | X | Invalid | |
| Clock Suspend | H | X | X | X | X | X | X | Invalid | |
| | L | H | X | X | X | X | X | Exit Clock Suspend Next Cycle | |
| | L | L | X | X | X | X | X | Maintain Clock Suspend | |
| Any State Other Than Listed Above | H | H | X | X | X | X | X | Refer to the Operation Command Table | |
| | H | L | X | X | X | X | X | Illegal | |
| | L | X | X | X | X | X | X | Invalid | |

- Notes:**
- *1. All entries in COMMAND TRUTH TABLE FOR CKE are specified at CKE(n) state and CKE input from CKE(n-1) to CKE(n) state must satisfy corresponding set up and hold time for CKE.
 - *2. CKE should be held High for t_{RC} period.
 - *3. SELF command should only be issued after the last data have been appeared on DQ.

■ FUNCTIONAL DESCRIPTION

SDRAM BASIC FUNCTION

Three major differences between this SDRAM and conventional DRAMs are: synchronized operation, burst mode, and mode register.

The **synchronized operation** is the fundamental difference. An SDRAM uses a clock input for the synchronization, where the DRAM is basically asynchronous memory although it has been using two clocks, \overline{RAS} and \overline{CAS} . Each operation of DRAM is determined by their timing phase differences while each operation of SDRAM is determined by commands and all operations are referenced to a positive clock edge. Fig.2 shows the basic timing diagram differences between SDRAMs and DRAMs.

The **burst mode** is a very high speed access mode utilizing an internal column address generator. Once a column addresses for the first access is set, following addresses are automatically generated by the internal column address counter.

The **mode register** is to justify the SDRAM operation and function into desired system conditions. MODE REGISTER TABLE shows how SDRAM can be configured for system requirement by mode register programming.

CLOCK (CLK) AND CLOCK ENABLE (CKE)

All input and output signals of SDRAM use register type buffers. A CLK is used as a trigger for the register and internal burst counter increment. All inputs are latched by a positive edge of CLK. All outputs are validated by the CLK. CKE is a high active clock enable signal. When CKE = Low is latched at a clock input during active cycle, the next clock will be internally masked. During idle state (all banks have been precharged), the Power Down mode(standby) is entered with CKE = Low and this will make extremely low standby current.

CHIP SELECT (\overline{CS})

\overline{CS} enables all commands inputs, \overline{RAS} , \overline{CAS} , and \overline{WE} , and address input. When \overline{CS} is High, command signals are negated but internal operation such as burst cycle will not be suspended. If such a control isn't needed, \overline{CS} can be tied to ground level.

COMMAND INPUTS (\overline{RAS} , \overline{CAS} and \overline{WE})

Unlike a conventional DRAM, \overline{RAS} , \overline{CAS} , and \overline{WE} do not directly imply SDRAM operation, such as Row address strobe by \overline{RAS} . Instead, each combination of \overline{RAS} , \overline{CAS} , and \overline{WE} input in conjunction with \overline{CS} input at a rising edge of the CLK determines SDRAM operation. Refer to FUNCTIONAL TRUTH TABLE in page 5.

ADDRESS INPUTS (A_0 to A_{10})

Address input selects an arbitrary location of a total of 524,288 words of each memory cell matrix. A total of 19 address input signals are required to decode such a matrix. SDRAM adopts an address multiplexer in order to reduce the pin count of the address line. At a Bank Active command (ACTV), 11 Row addresses are initially latched and the remainder of 8 Column addresses are then latched by a Column address strobe command of either a Read command (READ or READA) or Write command (WRIT or WRITA).

BANK SELECT (A_{11})

This SDRAM has two banks and each bank is organized as 512 K words by 16-bit. Bank selection by A_{11} occurs at Bank Active command (ACTV) followed by read (READ or READA), write (WRIT or WRITA), and precharge command (PRE).

MB81F161622C-60/-70/-80/-80L

DATA INPUTS AND OUTPUTS (DQ₀ to DQ₁₅)

Input data is latched and written into the memory at the clock following the write command input. Data output is obtained by the following conditions followed by a read command input:

- t_{RAC} : from the bank active command when t_{RCD} (min) is satisfied. (This parameter is reference only.)
- t_{CAC} : from the read command when t_{RCD} is greater than t_{RCD} (min). (This parameter is reference only.)
- t_{AC} : from the clock edge after t_{RAC} and t_{CAC}.

The polarity of the output data is identical to that of the input. Data is valid between access time (determined by the three conditions above) and the next positive clock edge (t_{OH}).

DATA I/O MASK (DQML/DQMU)

DQML and DQMU are active high enable inputs and have an output disable and input mask function. During burst cycle and when DQML/DQMU = High is latched by a clock, input is masked at the same clock and output will be masked at the second clock later while internal burst counter will increment by one or will go to the next stage depending on burst type.

DQML controls lower byte (DQ₀ to DQ₇) and DQMU controls upper byte (DQ₈ to DQ₁₅).

BURST MODE OPERATION AND BURST TYPE

The burst mode provides faster memory access. The burst mode is implemented by keeping the same Row address and by automatic strobing column address. Access time and cycle time of Burst mode is specified as t_{AC} and t_{CK}, respectively. The internal column address counter operation is determined by a mode register which defines burst type and burst count length of 1,2,4 or 8 bits of boundary. In order to terminate or to move from the current burst mode to the next stage while the remaining burst count is more than 1, the following combinations will be required:

| Current Stage | Next Stage | Method (Assert the following command) | |
|---------------|-------------|---------------------------------------|----------------------------------------|
| Burst Read | Burst Read | Read Command | |
| Burst Read | Burst Write | 1st Step | Mask Command (Normally 3 clock cycles) |
| | | 2nd Step | Write Command after LOWD |
| Burst Write | Burst Write | Write Command | |
| Burst Write | Burst Read | Read Command | |
| Burst Read | Precharge | Precharge Command | |
| Burst Write | Precharge | Precharge Command | |

The burst type can be selected either sequential or interleave mode if burst length is 2,4 or 8. The sequential mode is an incremental decoding scheme within a boundary address to be determined by count length, it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to least significant address(=0). The interleave mode is a scrambled decoding scheme for A₀ and A₂. If the first access of column address is even (0), the next address will be odd (1), or vice-versa.

(Continued)

MB81F161622C-60/-70/-80/-80L

(Continued)

When the full burst operation is executed at single write mode, Auto-precharge command is valid only at write operation.

The burst type can be selected either sequential or interleave mode. But only the sequential mode is usable to the full column burst. The sequential mode is an incremental decoding scheme within a boundary address to be determined by burst length, it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to least significant address(=0).

| Burst Length | Stating Column Address | Sequential Mode | Interleave |
|--------------|----------------------------------------------|-------------------------------|-------------------------------|
| | A ₂ A ₁ A ₀ | | |
| 2 | X X 0 | 0 - 1 | 0 - 1 |
| | X X 1 | 1 - 0 | 1 - 0 |
| 4 | X 0 0 | 0 - 1 - 2 - 3 | 0 - 1 - 2 - 3 |
| | X 0 1 | 1 - 2 - 3 - 0 | 1 - 0 - 3 - 2 |
| | X 1 0 | 2 - 3 - 0 - 1 | 2 - 3 - 0 - 1 |
| | X 1 1 | 3 - 0 - 1 - 2 | 3 - 2 - 1 - 0 |
| 8 | 0 0 0 | 0 - 1 - 2 - 3 - 4 - 5 - 6 - 7 | 0 - 1 - 2 - 3 - 4 - 5 - 6 - 7 |
| | 0 0 1 | 1 - 2 - 3 - 4 - 5 - 6 - 7 - 0 | 1 - 0 - 3 - 2 - 5 - 4 - 7 - 6 |
| | 0 1 0 | 2 - 3 - 4 - 5 - 6 - 7 - 0 - 1 | 2 - 3 - 0 - 1 - 6 - 7 - 4 - 5 |
| | 0 1 1 | 3 - 4 - 5 - 6 - 7 - 0 - 1 - 2 | 3 - 2 - 1 - 0 - 7 - 6 - 5 - 4 |
| | 1 0 0 | 4 - 5 - 6 - 7 - 0 - 1 - 2 - 3 | 4 - 5 - 6 - 7 - 0 - 1 - 2 - 3 |
| | 1 0 1 | 5 - 6 - 7 - 0 - 1 - 2 - 3 - 4 | 5 - 4 - 7 - 6 - 1 - 0 - 3 - 2 |
| | 1 1 0 | 6 - 7 - 0 - 1 - 2 - 3 - 4 - 5 | 6 - 7 - 4 - 5 - 2 - 3 - 0 - 1 |
| | 1 1 1 | 7 - 0 - 1 - 2 - 3 - 4 - 5 - 6 | 7 - 6 - 5 - 4 - 3 - 2 - 1 - 0 |

FULL COLUMN BURST AND BURST STOP COMMAND (BST)

The full column burst is an option of burst length and available only at sequential mode of burst type. This full column burst mode is repeatedly access to the same column. If burst mode reaches end of column address, then it wraps round to first column address (=0) and continues to count until interrupted by the news Read (READ) /Write (WRIT), Precharge (PRE), or Burst Stop (BST) command. The selection of Auto-precharge option is illegal during the full column burst operation except write command at BURST READ & SINGLE WRITE mode.

The BST command is applicable to terminated burst operation. If the BST command is asserted burst mode, its operation is terminated immediately and the internal state moves to Bank Active.

When read mode is interrupted by BST command, the output will be in High-Z.

For the detail rule, please refer to TIMING DIAGRAM-8.

When write mode is interrupted by BST command, the data to be applied at the same time with BST command will be ignored.

BURST READ & SINGLE WRITE

The burst read and single write mode provides single word write operation regardless of its burst length. In this mode, burst read operation does not affected by this mode.

MB81F161622C-60/-70/-80/-80L

PRECHARGE AND PRECHARGE OPTION (PRE, PALL)

SDRAM memory core is the same as conventional DRAMs', requiring precharge and refresh operations. Precharge rewrites the bit line and to reset the internal Row address line and is executed by the Precharge command (PRE). With the Precharge command, SDRAM will automatically be in standby state after precharge time (t_{RP}).

The precharged bank is selected by combination of AP and A_{11} when Precharge command is asserted. If AP = High, both banks are precharged regardless of A_{11} (PALL). If AP = Low, a bank to be selected by A_{11} is precharged (PRE). The Auto-precharge enters precharge mode at the end of burst mode of read or write without Precharge command assertion. This Auto-precharge is entered by AP = High when a read or write command is asserted. Refer to FUNCTION TRUTH TABLE.

AUTO-REFRESH (REF)

Auto-refresh uses the internal refresh address counter. The SDRAM Auto-refresh command (REF) generates Precharge command internally. All banks of SDRAM should be precharged prior to the Auto-refresh command. The Auto-refresh command should also be asserted every 15.6 μ s or a total 4096 refresh commands within a 64 ms period.

SELF-REFRESH ENTRY (SELF)

Self-refresh function provides automatic refresh by an internal timer as well as Auto-refresh and will continue the refresh function until cancelled by SELFX.

The Self-refresh is entered by applying an Auto-refresh command in conjunction with CKE = Low (SELF). Once SDRAM enters the self-refresh mode, all inputs except for CKE will be "don't care" (either logic high or low level state) and outputs will be in a High-Z state. During a Self-refresh mode, CKE = Low should be maintained. SELF command should only be issued after last read data has been appeared on DQ.

Note: When the burst refresh method is used, a total of 4096 auto-refresh commands within 4 ms must be asserted prior to the self-refresh mode entry.

SELF-REFRESH EXIT (SELFX)

To exit Self-Refresh mode, apply minimum t_{CKSP} after CKE brought high, and then the NOP command (NOP) or the Deselect command (DESL) should be asserted within minimum t_{RC} . Refer to Timing Diagram for the detail.

It is recommended to assert an Auto-refresh command just after the t_{RC} period to avoid the violation of refresh period.

Note: When the burst refresh method is used, a total of 4096 auto-refresh commands within 4 ms must be asserted after the self-refresh exit.

MODE REGISTER SET (MRS)

The mode register of SDRAM provides a variety of different operations. The register consists of four operation fields; Burst Length, Burst Type, CAS latency, and Operation Code. Refer to MODE REGISTER TABLE in page 33.

The mode register can be programmed by the Mode Register Set command (MRS). Each field is set by the address line. Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command (or part loses power). MRS command should only be issued on condition that all DQ is in Hi-Z.

The condition of the mode register is undefined after the power-up stage. It is required to set each field after initialization of SDRAM. Refer to POWER-UP INITIALIZATION below.

POWER-UP INITIALIZATION

The SDRAM internal condition after power-up will be undefined. It is required to follow the following Power On Sequence to execute read or write operation.

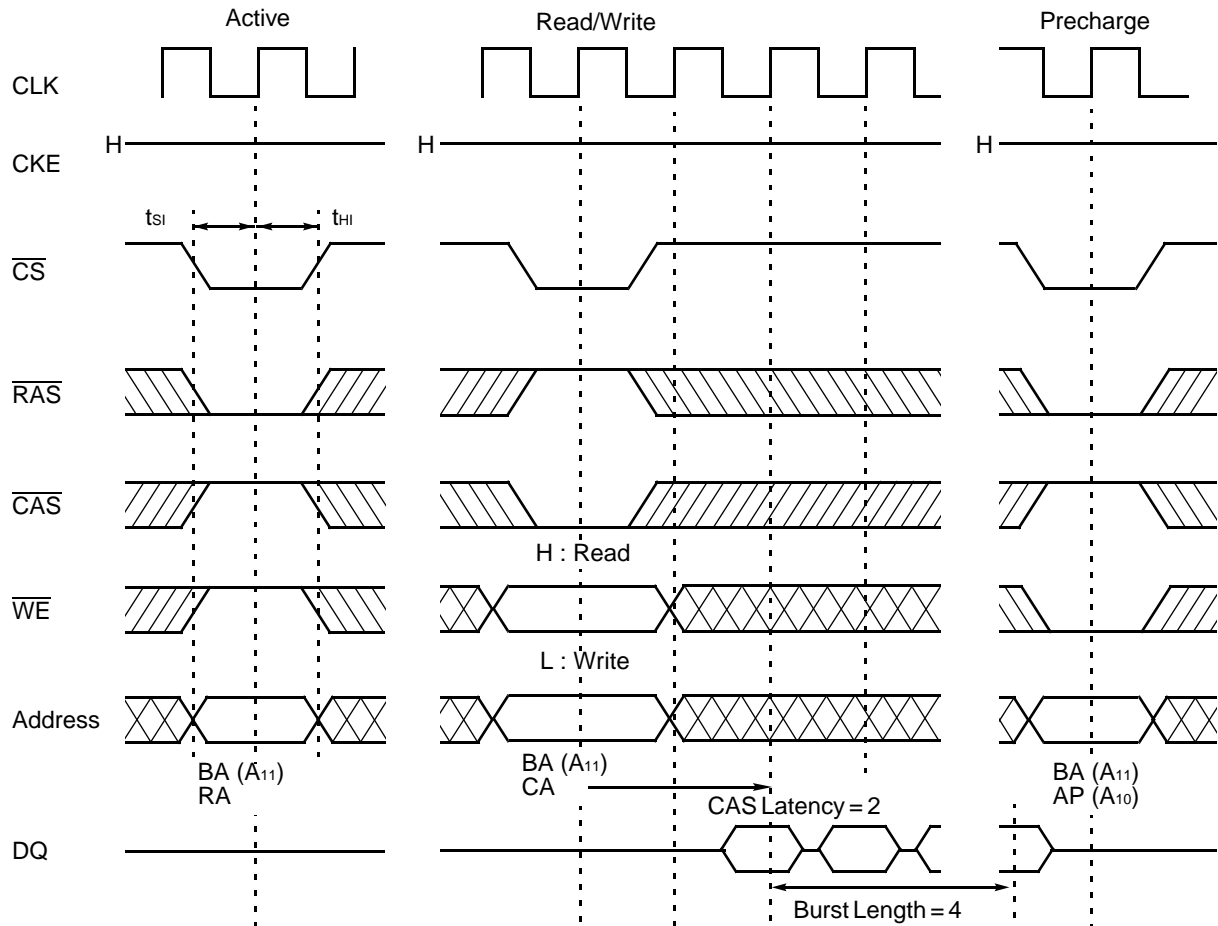
1. Apply power and start clock. Attempt to maintain either NOP or DESL command at the input.
2. Maintain stable power, stable clock, and NOP condition for a minimum of 200 μ s.
3. Precharge all banks by Precharge (PRE) or Precharge All command (PALL).
4. Assert minimum of 2 Auto-refresh command(REF).
5. Program the mode register by Mode Register Set command(MRS).

In addition, it is recommended DQML/DQMU and CKE to track V_{CC} to insure that output is High-Z state. The Mode Register Set command (MRS) can be set before 2 Auto-refresh command (REF).

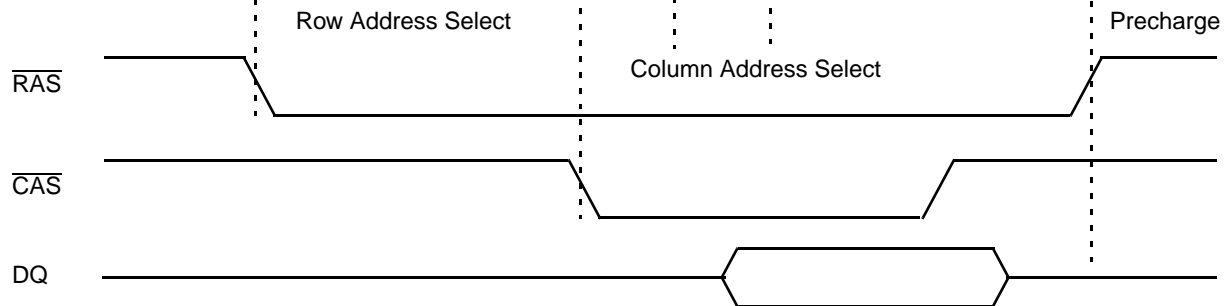
MB81F161622C-60/-70/-80/-80L

Fig. 2 – BASIC TIMING FOR CONVENTIONAL DRAM vs. SYNCHRONOUS DYNAMIC RAM

<SDRAM>

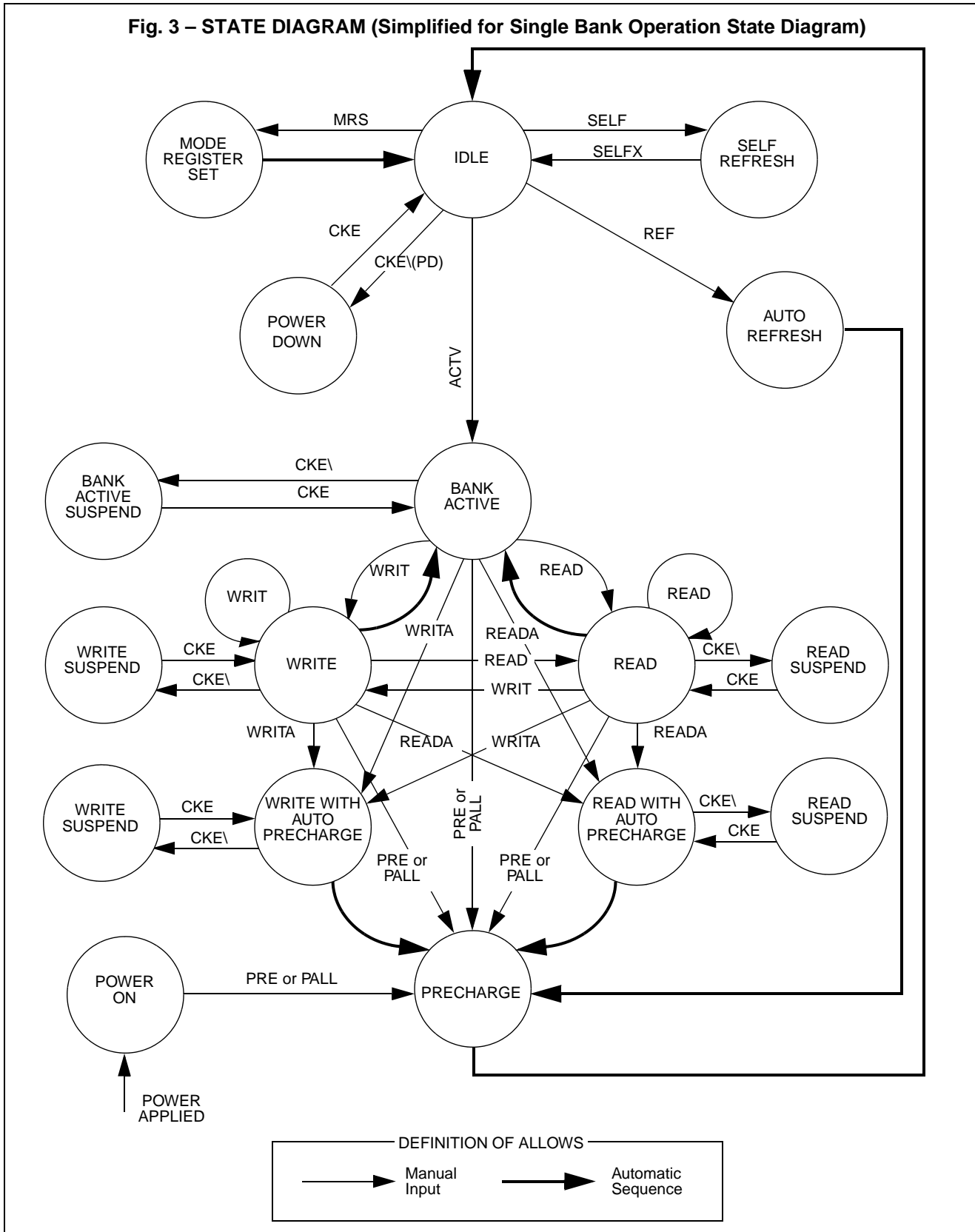


<Conventional DRAM>



MB81F161622C-60/-70/-80/-80L

Fig. 3 – STATE DIAGRAM (Simplified for Single Bank Operation State Diagram)




MB81F161622C-60/-70/-80/-80L

■ 1 BANK OPERATION COMMAND TABLE

MINIMUM CLOCK LATENCY OR DELAY TIME FOR 1 BANK OPERATION

| First command \ Second command (same bank) | MRS | ACTV | READ | READA | WRIT | WRITA | PRE | PALL | REF | SELF |
|--------------------------------------------|------------------------------------|------------------------------------|------------------|--------------------------------|------------------|--------------------------------|------------------|------------------|------------------------------------|------------------------------------|
| MRS | t _{RSC} | t _{RSC} | | | | | t _{RSC} | t _{RSC} | t _{RSC} | t _{RSC} |
| ACTV | | | t _{RCD} | t _{RCD} ^{*4} | t _{RCD} | t _{RCD} ^{*4} | t _{RAS} | t _{RAS} | | |
| READ | | | 1 | 1 | 1 ^{*1} | 1 ^{*1} | 1 | 1 | | |
| READA | BL + t _{RP} ^{*2} | BL + t _{RP} ^{*2} | | | | | | | BL + t _{RP} ^{*2} | BL + t _{RP} ^{*2} |
| WRIT | | | t _{WR} | t _{WR} | 1 | 1 | t _{DPL} | t _{DPL} | | |
| WRITA | t _{DAL} | t _{DAL} | | | | | | | t _{DAL} | t _{DAL} |
| PRE | t _{RP} ^{*3} | t _{RP} ^{*3} | | | | | t _{RP} | t _{RP} | t _{RP} ^{*3} | t _{RP} ^{*3} |
| PALL | t _{RP} ^{*3} | t _{RP} ^{*3} | | | | | t _{RP} | t _{RP} | t _{RP} ^{*3} | t _{RP} ^{*3} |
| REF | t _{RC} | t _{RC} | | | | | t _{RC} | t _{RC} | t _{RC} | t _{RC} |
| SELF | t _{RC} | t _{RC} | | | | | | | t _{RC} | t _{RC} |

- Notes:** *1. Assume no I/O conflict.
 *2. If $t_{RP} \leq t_{CK}$, minimum latency is a sum of BL + CL.
 *3. Assume Output is in High-Z state.
 *4. Assume t_{RAS} is satisfied.

 Illegal Command

MB81F161622C-60/-70/-80/-80L

■ MULTI BANK OPERATION COMMAND TABLE

MINIMUM CLOCK LATENCY OR DELAY TIME FOR 2 BANK OPERATION

| Second command (opposite bank) \ First command | MRS | ACTV | READ | READA | WRIT | WRITA | PRE | PALL | REF | SELF |
|------------------------------------------------|--------------------------------------------------|--------------------------------|-----------------|-----------------|-------------------------------|-------------------------------|------------------|------------------|--------------------------------------------------|--------------------------------------------------|
| MRS | t _{RSC} | t _{RSC} | | | | | t _{RSC} | t _{RSC} | t _{RSC} | t _{RSC} |
| ACTV | | ^{*1} t _{RRD} | ^{*2} 1 | ^{*2} 1 | ^{*2} 1 | ^{*2} 1 | ^{*7} 1 | t _{RAS} | | |
| READ | | ^{*1} 1 | ^{*2} 1 | ^{*2} 1 | ^{*2} ^{*3} 1 | ^{*2} ^{*3} 1 | ^{*7} 1 | ^{*8} 1 | | |
| READA ^{*9} | ^{*1} ^{*4} BL + t _{RP} | ^{*1} 1 | ^{*2} 1 | ^{*2} 1 | ^{*2} 1 | ^{*2} 1 | ^{*7} 1 | | ^{*1} ^{*4} BL + t _{RP} | ^{*1} ^{*4} BL + t _{RP} |
| WRIT | | ^{*1} 1 | ^{*2} 1 | ^{*2} 1 | ^{*2} 1 | ^{*2} 1 | ^{*7} 1 | ^{*8} 1 | | |
| WRITA ^{*9} | ^{*1} ^{*4} BL + t _{RP} | ^{*1} 1 | ^{*2} 1 | ^{*2} 1 | ^{*2} 1 | ^{*2} 1 | ^{*7} 1 | | ^{*1} BL + 1 + t _{RP} | ^{*1} BL + 1 + t _{RP} |
| PRE | ^{*1} t _{RP} | ^{*1} 1 | ^{*2} 1 | ^{*2} 1 | ^{*2} 1 | ^{*2} 1 | ^{*7} 1 | t _{RAS} | ^{*1} t _{RP} | ^{*1} t _{RP} |
| PALL | t _{RP} | ^{*1} t _{RP} | | | | | ^{*7} 1 | ^{*8} 1 | ^{*1} ^{*6} t _{RP} | ^{*1} ^{*6} t _{RP} |
| REF | t _{RC} | t _{RC} | | | | | t _{RC} | t _{RC} | t _{RC} | t _{RC} |
| SELF | t _{RC} | t _{RC} | | | | | | | t _{RC} | t _{RC} |

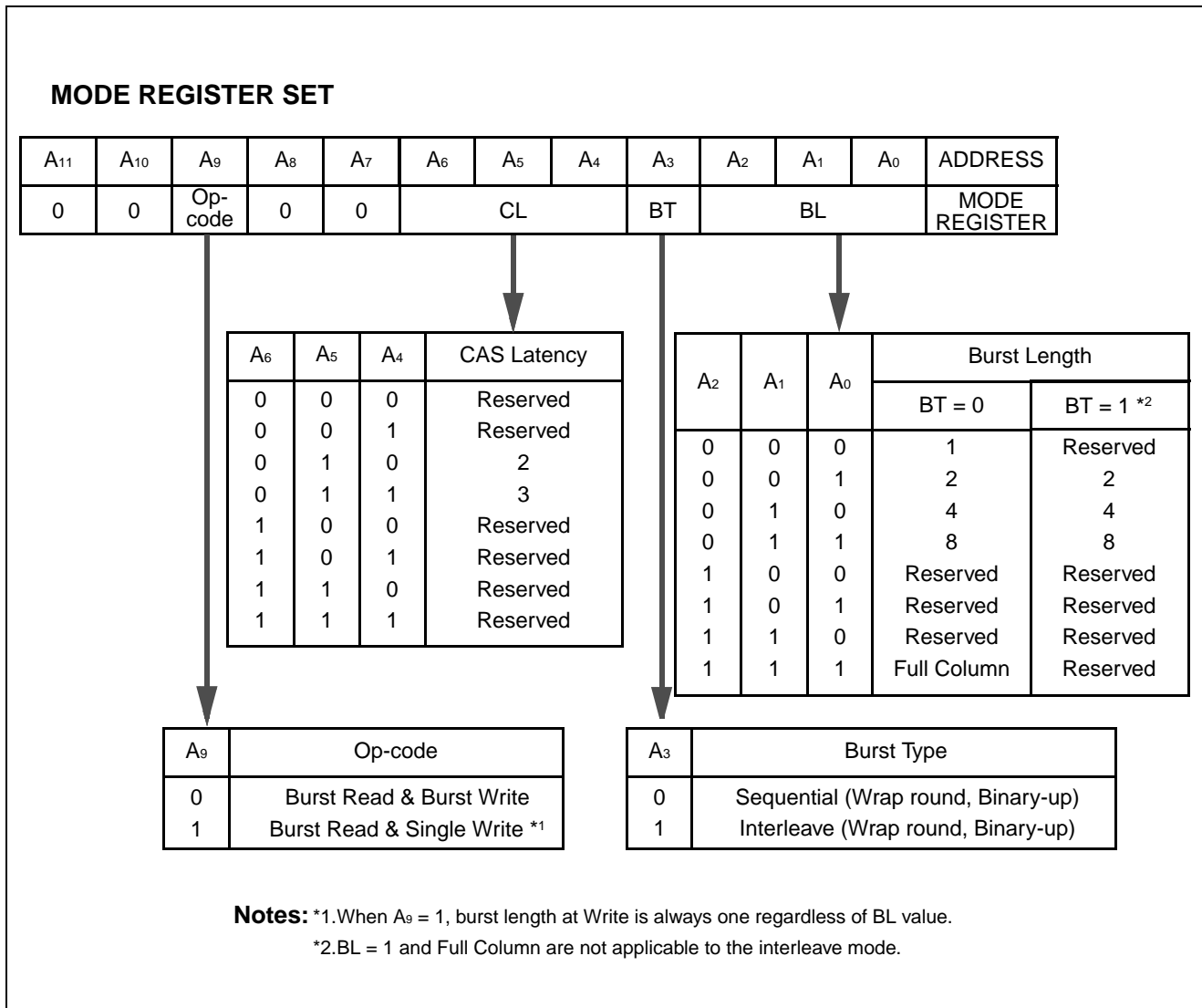
- Notes:**
- *1. Assume opposite bank is in idle state.
 - *2. Assume opposite bank is in active state.
 - *3. Assume no I/O conflict.
 - *4. If t_{RP} ≤ t_{CK}, minimum latency is a sum of BL + CL.
 - *5. Assume PALL command dose not affect any operation on opposite bank.
 - *6. Assume Output is in High-Z state.
 - *7. Assume t_{RAS} of opposite bank is satisfied.
 - *8. Assume t_{RAS}(ACTV to PALL) is satisfied.
 - *9. If opposite bank should be interrupted, t_{RAS} of own bank is satisfied..



Illegal Command

MB81F161622C-60/-70/-80/-80L

MODE REGISTER TABLE



MB81F161622C-60/-70/-80/-80L

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

| Parameter | Symbol | Value | Unit |
|-------------------------------------------------|-------------------|--------------|------|
| Voltage of V_{CC} Supply Relative to V_{SS} | V_{CC} | -0.5 to +4.6 | V |
| Voltage at Any Pin Relative to V_{SS} | V_{IN}, V_{OUT} | -0.5 to +4.6 | V |
| Short Circuit Output Current | I_{OUT} | -50 to +50 | mA |
| Power Dissipation | P_D | 1.3 | W |
| Storage Temperature | T_{STG} | -55 to +125 | °C |

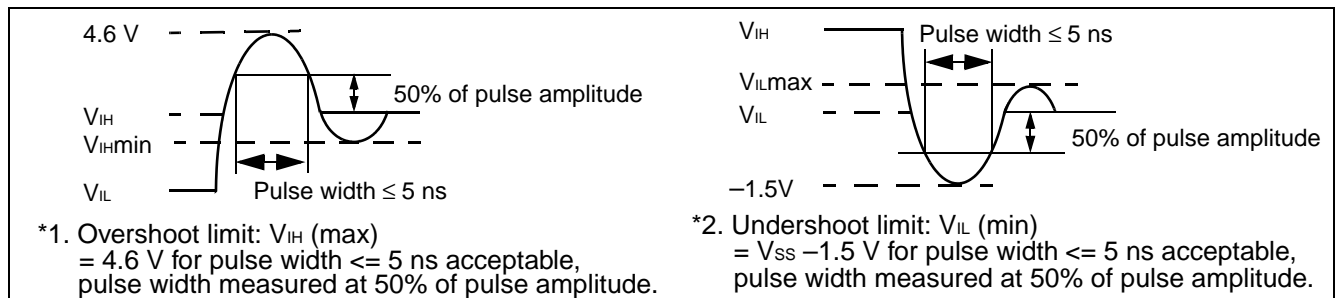
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

| Parameter | Notes | Symbol | Min. | Typ. | Max. | Unit |
|---------------------|--------------|-------------------|------|------|----------------|------|
| Supply Voltage | -60 | V_{CC}, V_{CCQ} | 3.15 | 3.3 | 3.6 | V |
| | -70/-80/-80L | V_{CC}, V_{CCQ} | 3.0 | 3.3 | 3.6 | V |
| | | V_{SS}, V_{SSQ} | 0 | 0 | 0 | V |
| Input High Voltage | *1 | V_{IH} | 2.0 | — | $V_{CC} + 0.5$ | V |
| Input Low Voltage | *2 | V_{IL} | -0.5 | — | 0.8 | V |
| Ambient Temperature | | T_A | 0 | — | 70 | °C |

Notes:



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within these recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ CAPACITANCE

($T_A = 25^\circ\text{C}$, $f = 1$ MHz)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|-----------------------------------|-----------|------|------|------|------|
| Input Capacitance, Except for CLK | C_{IN1} | 2.5 | — | 5 | pF |
| Input Capacitance for CLK | C_{IN2} | 2.5 | — | 4 | pF |
| I/O Capacitance | $C_{I/O}$ | 4.0 | — | 6.5 | pF |

MB81F161622C-60/-70/-80/-80L

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes *1, *2, and *3

| Parameter | | Symbol | Conditions | Value | | Unit | |
|-----------------------------------------------------------|----------------------------------------|----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|---------------|----|
| | | | | Min. | Max. | | |
| Output High Voltage | | $V_{OH(DC)}$ | $I_{OH} = -2 \text{ mA}$ | 2.4 | — | V | |
| Output Low Voltage | | $V_{OL(DC)}$ | $I_{OL} = 2 \text{ mA}$ | — | 0.4 | V | |
| Input Leakage Current (Any Input) | | I_{LI} | $0 \text{ V} \leq V_{IN} \leq V_{CC}$; All other pins not under test = 0 V | -5 | 5 | μA | |
| Output Leakage Current | | I_{LO} | $0 \text{ V} \leq V_{IN} \leq V_{CC}$; Data out disabled | -5 | 5 | μA | |
| Operating Current (Average Power Supply Current) | MB81F161622C-60 | I_{CC1S} | Burst: Length = 4, $t_{RC} = \text{min}$ for BL = 4, $t_{CK} = \text{min}$, One bank active, Outputs open, Addresses changed up to 3-times during $t_{RC}(\text{min})$, $0 \text{ V} \leq V_{IN} \leq V_{CC}$ V_{CCQ} current is included. | — | 150 | mA | |
| | MB81F161622C-70 | | | | 130 | | |
| | MB81F161622C-80/-80L | | | | 110 | | |
| | Reference Spec (100MHz @CL=3) *4 | | | | 90 | | |
| Precharge Standby Current (Power Supply Current) | | I_{CC2P} | CKE = V_{IL} , All banks idle, $t_{CK} = \text{min}$, Power down mode, $0 \text{ V} \leq V_{IN} \leq V_{CC}$ | — | 1 | mA | |
| | | I_{CC2PS} | MB81F161622C -60/-70/-80 | CKE = V_{IL} , All banks idle, CLK = H or L, Power down mode, $0 \text{ V} \leq V_{IN} \leq V_{CC}$ | — | 1 | mA |
| | | | MB81F161622C-80L | — | 400 | μA | |
| | | I_{CC2N} | MB81F161622C-60 | CKE = V_{IH} , All banks idle, $t_{CK} = \text{min}$, NOP commands only, Input signals (except to CMD) are changed one times during 3 clock cycles, $0 \text{ V} \leq V_{IN} \leq V_{CC}$ | — | 20 | mA |
| | | | MB81F161622C-70 | — | 20 | | |
| | | | MB81F161622C-80/-80L | — | 20 | | |
| | | Reference Spec (100MHz @CL=3) *4 | — | 15 | | | |
| | | I_{CC2NS} | CKE = V_{IH} , All banks idle, CLK = H or L, Input signals are stable, $0 \text{ V} \leq V_{IN} \leq V_{CC}$ | — | 2 | | |

(Continued)

MB81F161622C-60/-70/-80/-80L

(Continued)

| Parameter | Symbol | Conditions | Value | | Unit |
|------------------------------------------------------|----------------------------------|-------------|-------|------|---------|
| | | | Min. | Max. | |
| Active Standby Current (Power Supply Current) | MB81F161622C-60/-70/-80 | I_{CC3P} | — | 1 | mA |
| | MB81F161622C-80L | I_{CC3PS} | — | 400 | μ A |
| Active Standby Current (Power Supply Current) | MB81F161622C-60 | I_{CC3N} | — | 35 | mA |
| | MB81F161622C-70 | | | 30 | mA |
| | MB81F161622C-80/-80L | | | 30 | mA |
| | Reference Spec (100MHz @CL=3) *4 | | | 20 | mA |
| | | I_{CC3NS} | — | 2 | mA |
| Burst mode Current (Average Power Supply Current) | MB81F161622C-60 | I_{CC4} | — | 185 | mA |
| | MB81F161622C-70 | | | 160 | |
| | MB81F161622C-80/-80L | | | 145 | |
| | Reference Spec (100MHz @CL=3) *4 | | | 120 | |
| Refresh Current #1 (Average Power Supply Current) | MB81F161622C-60 | I_{CC5} | — | 80 | mA |
| | MB81F161622C-70 | | | 70 | |
| | MB81F161622C-80/-80L | | | 60 | |
| | Reference Spec (100MHz @CL=3) *4 | | | 55 | |
| Refresh Current #2 (Average Power Supply Current) | MB81F161622C-60/-70/-80 | I_{CC6} | — | 1 | mA |
| | MB81F161622C-80L | | | 400 | μ A |

- Notes:**
- *1. All voltages are referred to V_{SS} .
 - *2. DC characteristics are measured after following the POWER-UP INITIALIZATION procedure.
 - *3. I_{CC} depends on the output termination or load condition, clock cycle rate, signal clocking rate. The specified values are obtained with the output open and no termination register.
 - *4. This value is for reference only.

MB81F161622C-60/-70/-80/-80L

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes *1, *2, and *3

| Parameter | Notes | Symbol | MB81F161622C -60 | | MB81F161622C -70 | | MB81F161622C -80/-80L | | Reference Spec (100MHz@CL=3) ^{*4} | | Unit |
|-----------------------------------------------------------------|-----------------|-------------------|---------------------|------|---------------------|------|--------------------------|------|-----------------------------------------------|------|------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Clock Period | CAS Latency = 2 | t _{CK2} | — | — | 10.5 | — | 12 | — | 15 | — | ns |
| | CAS Latency = 3 | t _{CK3} | 6.0 | — | 7.0 | — | 8 | — | 10 | — | ns |
| Clock High Time | *5 | t _{CH} | 2.5 | — | 2.5 | — | 3 | — | 3 | — | ns |
| Clock Low Time | *5 | t _{CL} | 2.5 | — | 2.5 | — | 3 | — | 3 | — | ns |
| Input Setup Time | *5 | t _{SI} | 2 | — | 2 | — | 2.5 | — | 2.5 | — | ns |
| Input Hold Time | *5 | t _{HI} | 1 | — | 1 | — | 1 | — | 1 | — | ns |
| Access Time from Clock (t _{CK} =min) *5,*6,*7 | CAS Latency = 2 | t _{AC2} | — | — | — | 7 | — | 7 | — | 7 | ns |
| | CAS Latency = 3 | t _{AC3} | — | 5.5 | — | 6 | — | 6 | — | 6 | ns |
| Output in Low-Z | *5 | t _{LZ} | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| Output in High-Z *5,*8 | CAS Latency = 2 | t _{HZ2} | — | — | 2 | 7 | 2 | 7 | 2 | 7 | ns |
| | CAS Latency = 3 | t _{HZ3} | 2 | 5.5 | 2 | 6 | 2 | 6 | 2 | 6 | ns |
| Output Hold Time *5,*7 | CAS Latency = 2 | t _{OH} | — | — | 2 | — | 2 | — | 2 | — | ns |
| | CAS Latency = 3 | | 2 | — | 2 | — | 2 | — | 2 | — | ns |
| Time between Auto-refresh command Interval | *4 | t _{REFI} | — | 15.6 | — | 15.6 | — | 15.6 | — | 15.6 | μs |
| Transition Time | | t _T | 0.5 | 10 | 0.5 | 10 | 0.5 | 10 | 0.5 | 10 | ns |
| CKE Setup time for Power Down Exit | *5 | t _{CKSP} | 3 | — | 3 | — | 3 | — | 3 | — | ns |

MB81F161622C-60/-70/-80/-80L

BASE VALUES FOR CLOCK COUNT/LATENCY

| Parameter | Notes | Symbol | MB81F161622C -60 | | MB81F161622C -70 | | MB81F161622C -80/-80L | | Reference Spec ^{#4} (100MHz@CL=3) | | Unit |
|------------------------------------------|-----------------|-------------------|----------------------|--------|----------------------|--------|--------------------------|--------|-----------------------------------------------|--------|------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| RAS Cycle Time | *9 | t _{RC} | 54.0 | — | 63.0 | — | 72 | — | 80 | — | ns |
| RAS Precharge Time | | t _{RP} | 18.0 | — | 21.0 | — | 24 | — | 30 | — | ns |
| RAS Active Time | | t _{RAS} | 36 | 100000 | 42 | 100000 | 48 | 100000 | 50 | 100000 | ns |
| RAS to CAS Delay Time | | t _{RCD} | 18.0 | — | 21.0 | — | 24 | — | 30 | — | ns |
| Write Recovery Time | | t _{WR} | 6.0 | — | 7.0 | — | 8 | — | 10 | — | ns |
| Data-in to Precharge Lead Time | | t _{DPL} | 6.0 | — | 7.0 | — | 8 | — | 10 | — | ns |
| Data-in to Active/Refresh Command Period | CAS Latency = 2 | t _{DAL2} | — | — | 1cyc+t _{RP} | — | 1cyc+t _{RP} | — | 1cyc+t _{RP} | — | ns |
| | CAS Latency = 3 | t _{DAL3} | 2cyc+t _{RP} | — | 2cyc+t _{RP} | — | 2cyc+t _{RP} | — | 2cyc+t _{RP} | — | ns |
| Mode Register Set Cycle Time | | t _{RSC} | 12 | — | 14 | — | 16 | — | 20 | — | ns |
| RAS to RAS Bank Active Delay Time | | t _{RBD} | 12 | — | 14 | — | 16 | — | 20 | — | ns |

CLOCK COUNT FORMULA Note *10

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \quad (\text{Round off a whole number})$$

MB81F161622C-60/-70/-80/-80L

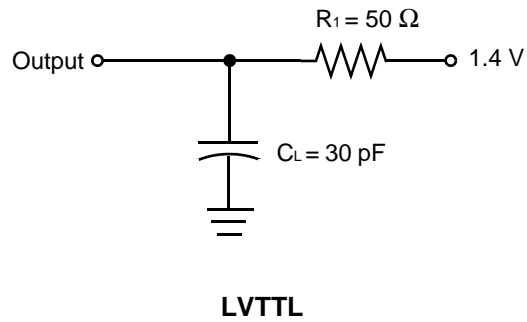
LATENCY-FIXED VALUES

(The latency values on these parameters are fixed regardless of clock period.)

| Parameter | Notes | Sym- bol | MB81F161622C -60 | MB81F161622C -70 | MB81F161622C -80/-80L | Reference Spec ^{*4} (100MHz@CL=3) | Unit |
|----------------------------------------------|--------|-------------------|---------------------|---------------------|--------------------------|-----------------------------------------------|-------|
| CKE to Clock Disable | | l _{CKE} | 1 | 1 | 1 | 1 | cycle |
| DQM to Output in High-Z | | l _{DQZ} | 2 | 2 | 2 | 2 | cycle |
| DQM to Input Data Delay | | l _{DQD} | 0 | 0 | 0 | 0 | cycle |
| Last Output to Write Command Delay | | l _{OWD} | 2 | 2 | 2 | 2 | cycle |
| Write Command to Input Data Delay | | l _{DWD} | 0 | 0 | 0 | 0 | cycle |
| Precharge to Output in High-Z Delay | CL = 2 | l _{ROH2} | — | 2 | 2 | 2 | cycle |
| | CL = 3 | l _{ROH3} | 3 | 3 | 3 | 3 | cycle |
| Burst Stop Command to Output in High-Z Delay | CL = 2 | l _{BSH2} | — | 2 | 2 | 2 | cycle |
| | CL = 3 | l _{BSH3} | 3 | 3 | 3 | 3 | cycle |
| CAS to CAS Delay (min) | | l _{CCD} | 1 | 1 | 1 | 1 | cycle |
| CAS Bank Delay (min) | | l _{CBD} | 1 | 1 | 1 | 1 | cycle |

- Notes:**
- *1. AC characteristics are measured after following the POWER-UP INITIALIZATION procedure.
 - *2. AC characteristics assume $t_r = 1$ ns and 30 pF of terminated load.
 - *3. 1.4 V is the reference level for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).
 - *4. This value is for reference only.
 - *5. If input signal transition time (t_r) is longer than 1 ns; $[(t_r/2) - 0.5]$ ns should be added to t_{AC} (max), t_{HZ} (max), and t_{CKSP} (min) spec values, $[(t_r/2) - 0.5]$ ns should be subtracted from t_{LZ} (min), t_{HZ} (min), and t_{OH} (min) spec values, and $(t_r - 1.0)$ ns should be added to t_{CH} (min), t_{CL} (min), t_{SI} (min), and t_{HI} (min) spec values.
 - *6. t_{AC} also specifies the access time at burst mode.
 - *7. t_{AC} and t_{OH} are the spec value under AC test load circuit shown in Fig. 4.
 - *8. Specified where output buffer is no longer driven.
 - *9. Actual clock count of t_{RC} (l_{RC}) will be sum of clock count of t_{RAS} (l_{RAS}) and t_{RP} (l_{RP}).
 - *10. All base values are measured from the clock edge at the command input to the clock edge for the next command input. All clock counts are calculated by a simple formula: clock count equals base value divided by clock period (round off to a whole number).

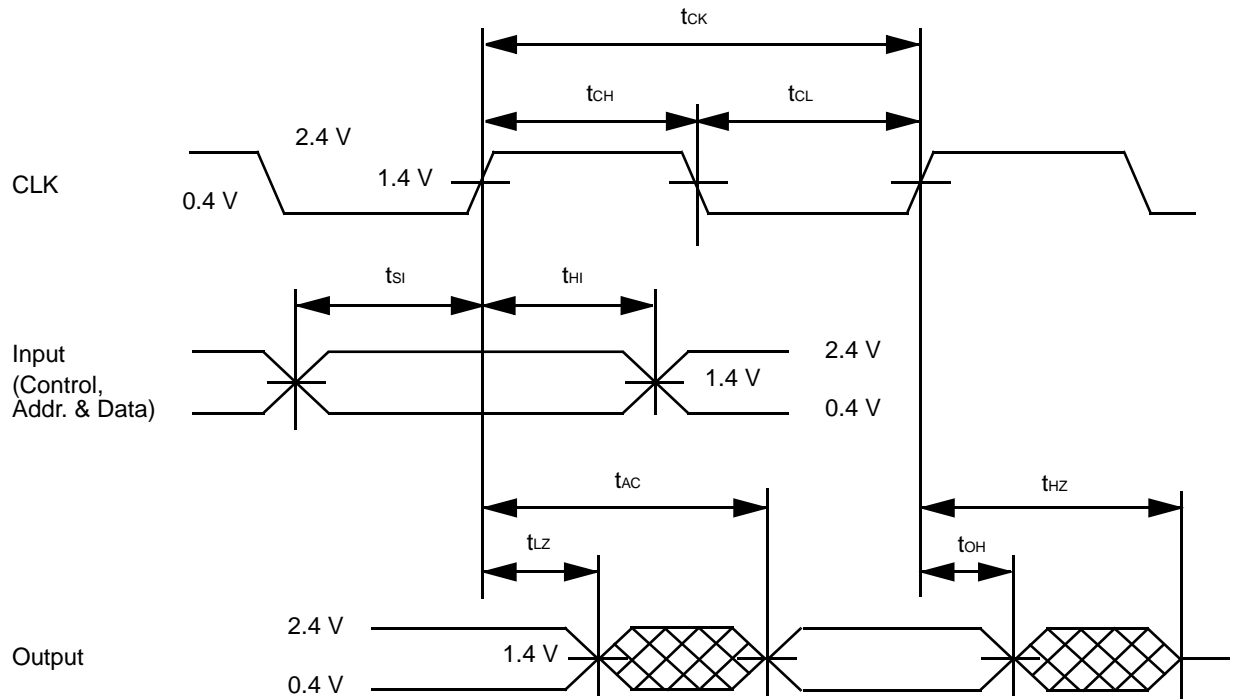
Fig. 4 – EXAMPLE OF AC TEST LOAD CIRCUIT



Note: AC characteristics are measured in this condition. This load circuits are not applicable for V_{OH} and V_{OL} .

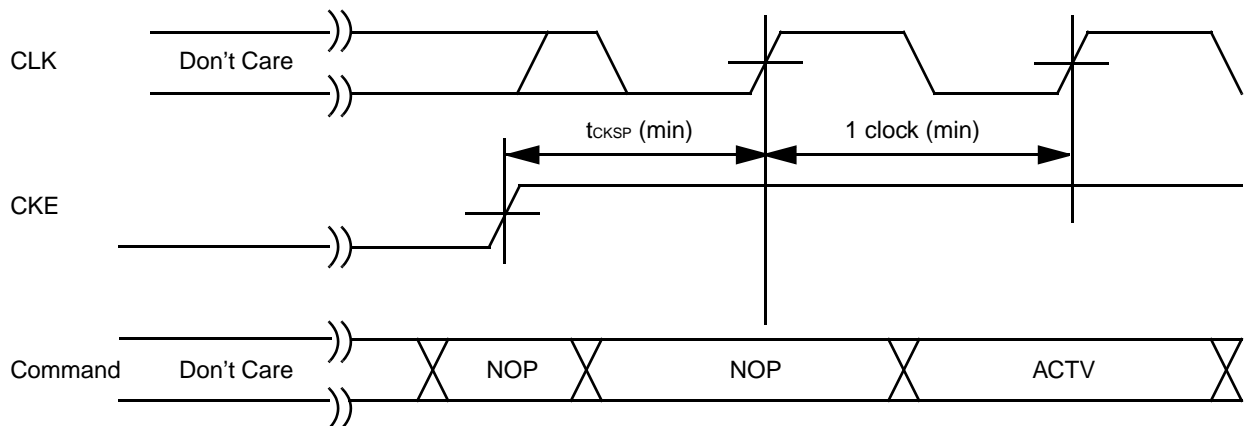
MB81F161622C-60/-70/-80/-80L

Fig. 5 – TIMING DIAGRAM, SETUP, HOLD AND DELAY TIME



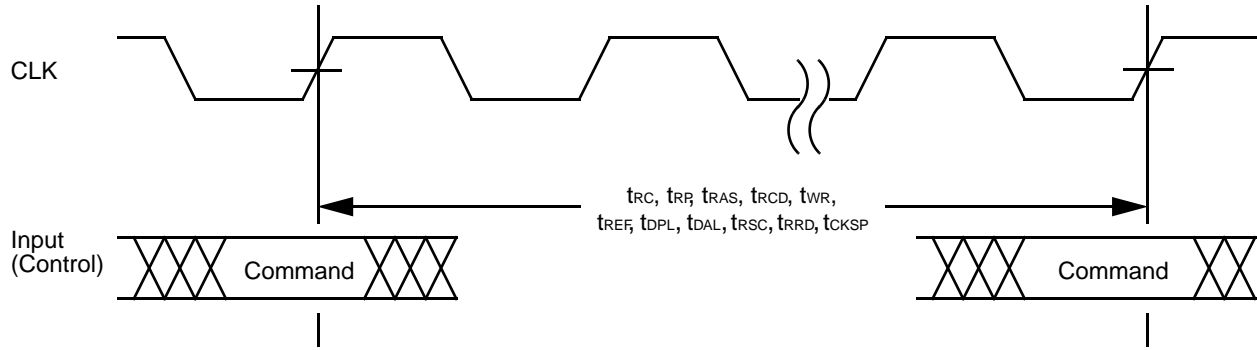
Note: Reference level of input signal is 1.4 V for LVTTTL.
Access time is measured at 1.4 V for LVTTTL.

Fig. 6 – TIMING DIAGRAM, DELAY TIME FOR POWER DOWN EXIT



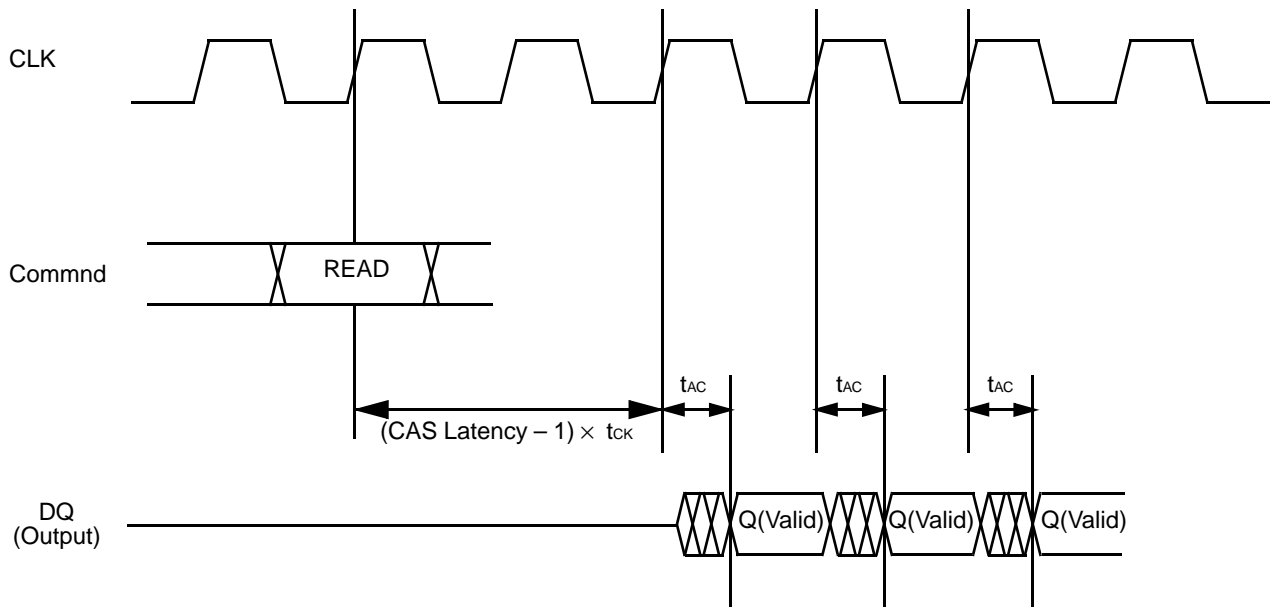
MB81F161622C-60/-70/-80/-80L

Fig. 7 – TIMING DIAGRAM, PULSE WIDTH



Note: These parameter are a limit value of the rising edge of the clock from one command input to next input. t_{CKSP} is the latency value from the rising edge of CKE. Measurement reference voltage is 1.4 V.

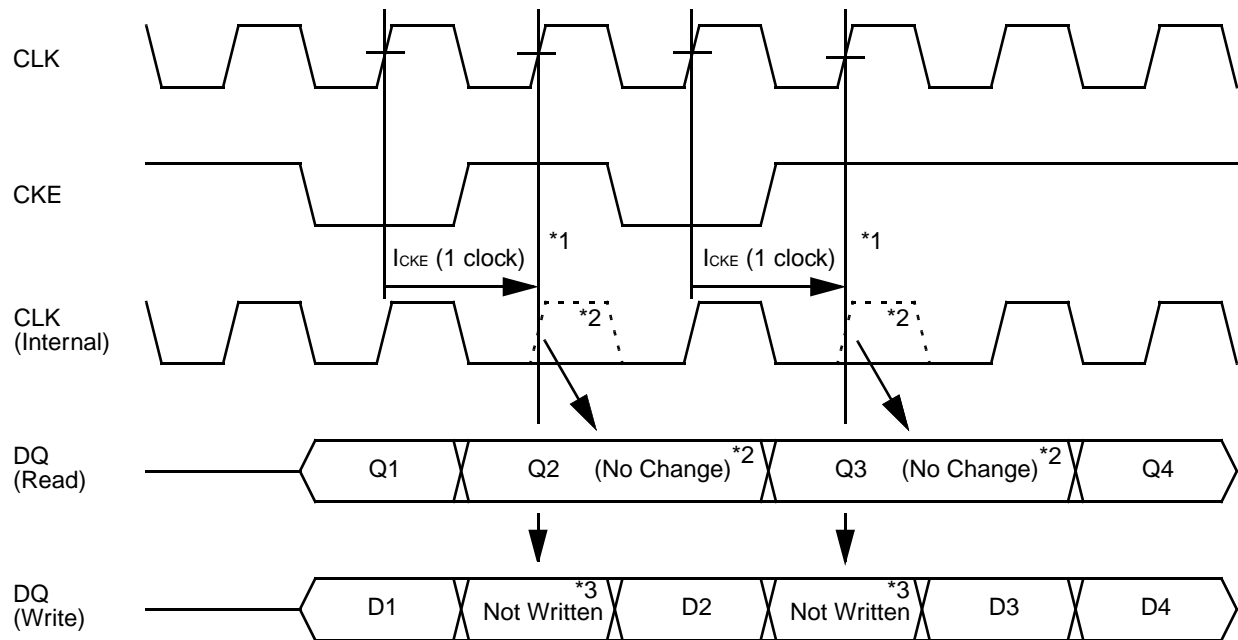
Fig. 8 – TIMING DIAGRAM, ACCESS TIME



MB81F161622C-60/-70/-80/-80L

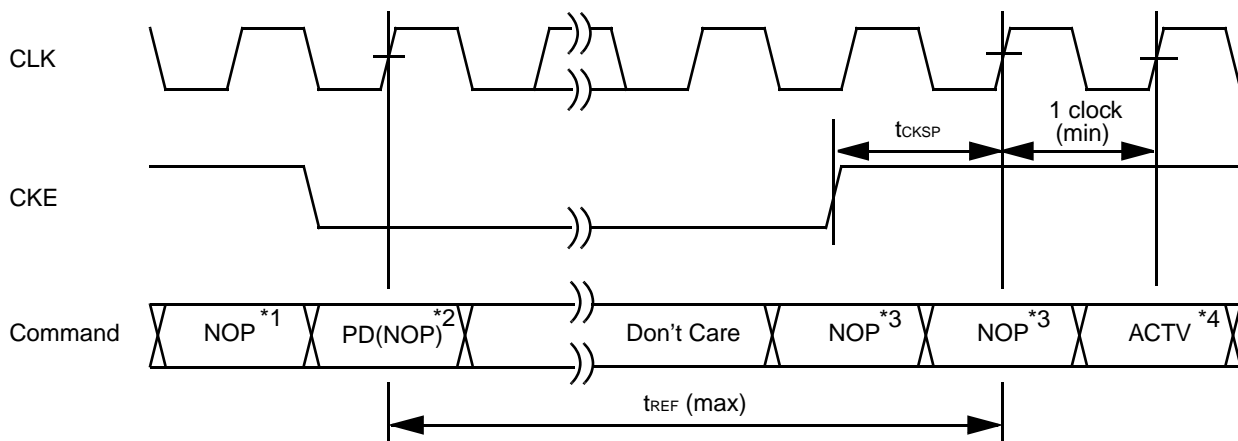
TIMING DIAGRAMS

TIMING DIAGRAM - 1 : CLOCK ENABLE - READ AND WRITE SUSPEND (@ BL = 4)



- Notes:**
- *1. The latency of CKE (l_{CKE}) is one clock.
 - *2. During read mode, burst counter will not be incremented/decremented at the next clock of CSUS command. Output remain the same data.
 - *3. During the write mode, data at the next clock of CSUS command is ignored.

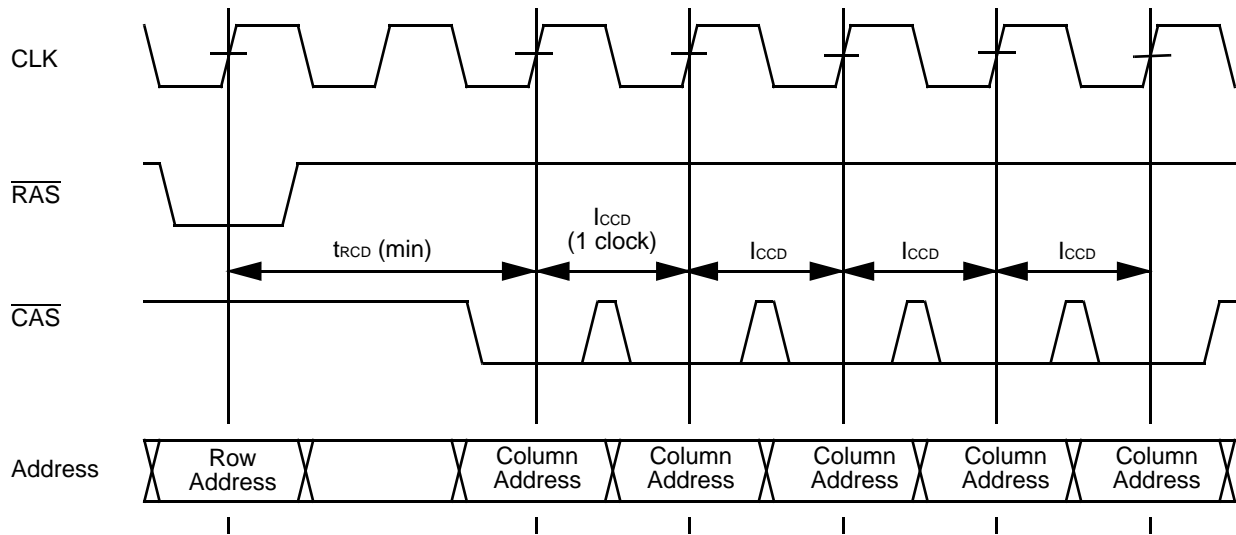
TIMING DIAGRAM - 2 : CLOCK ENABLE - POWER DOWN ENTRY AND EXIT



- Notes:**
- *1. Precharge command (PRE or PALL) should be asserted if any bank is active and in the burst mode.
 - *2. Precharge command can be posted in conjunction with CKE when burst mode is ended at this clock.
 - *3. The ACTV command can be latched after $t_{CKSP}(\text{min}) + 1 \text{ clock}(\text{min})$. It should be asserted NOP command in conjunction with CKE.
 - *4. The ACTV command can be latched after $t_{CKSP}(\text{min.}) + 1 \text{ clock}(\text{min.})$.

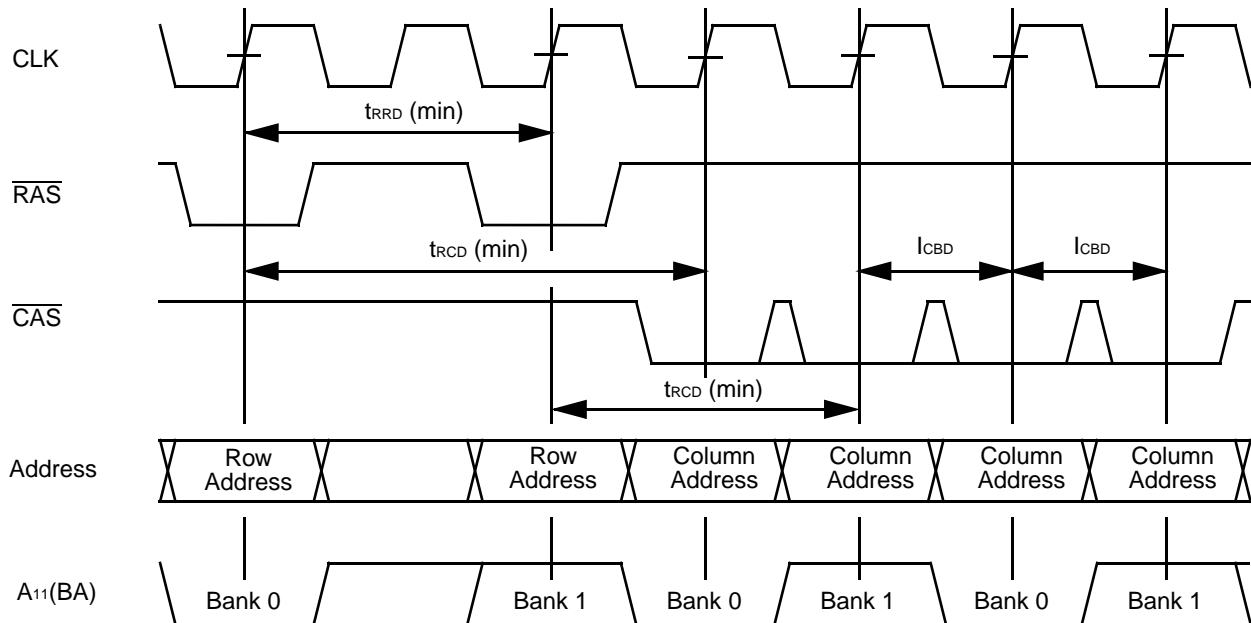
MB81F161622C-60/-70/-80/-80L

TIMING DIAGRAM - 3 : COLUMN ADDRESS TO COLUMN ADDRESS INPUT DELAY



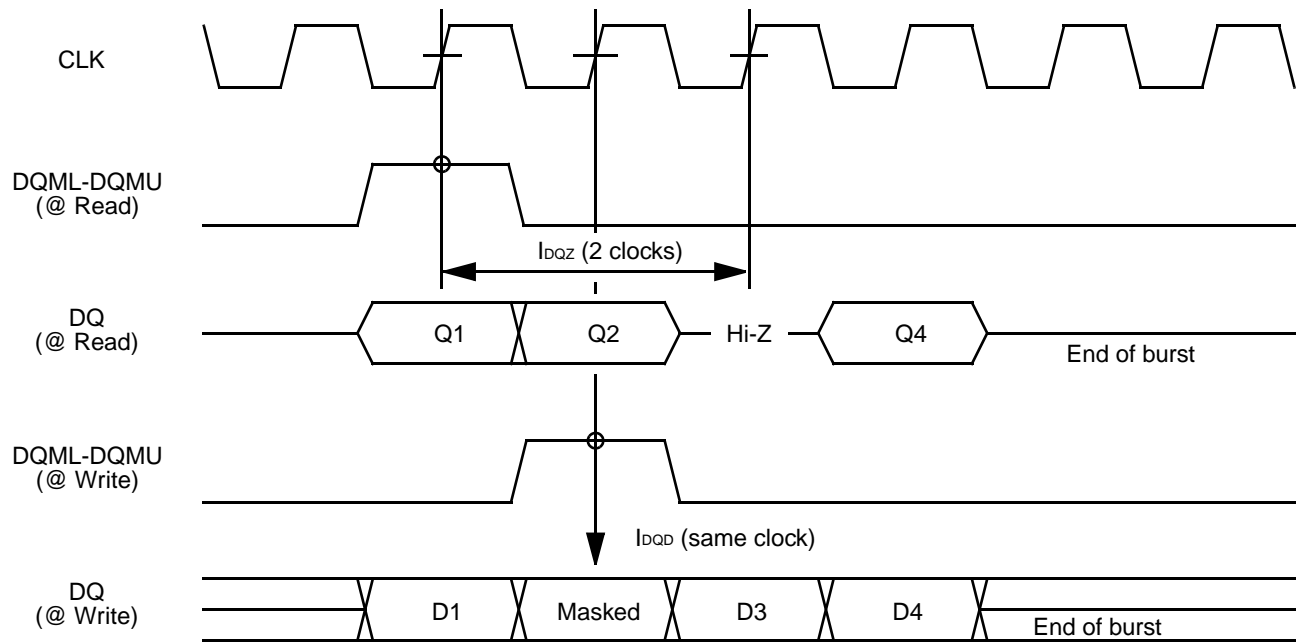
Note: \overline{CAS} to \overline{CAS} address delay can be one or more clock period.

TIMING DIAGRAM - 4 : DIFFERENT BANK ADDRESS INPUT DELAY

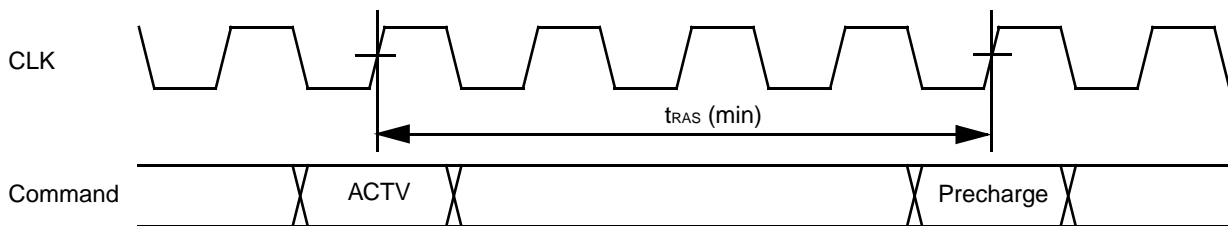


MB81F161622C-60/-70/-80/-80L

TIMING DIAGRAM - 5 : DQM-INPUT MASK AND OUTPUT DISABLE (@ BL = 4)



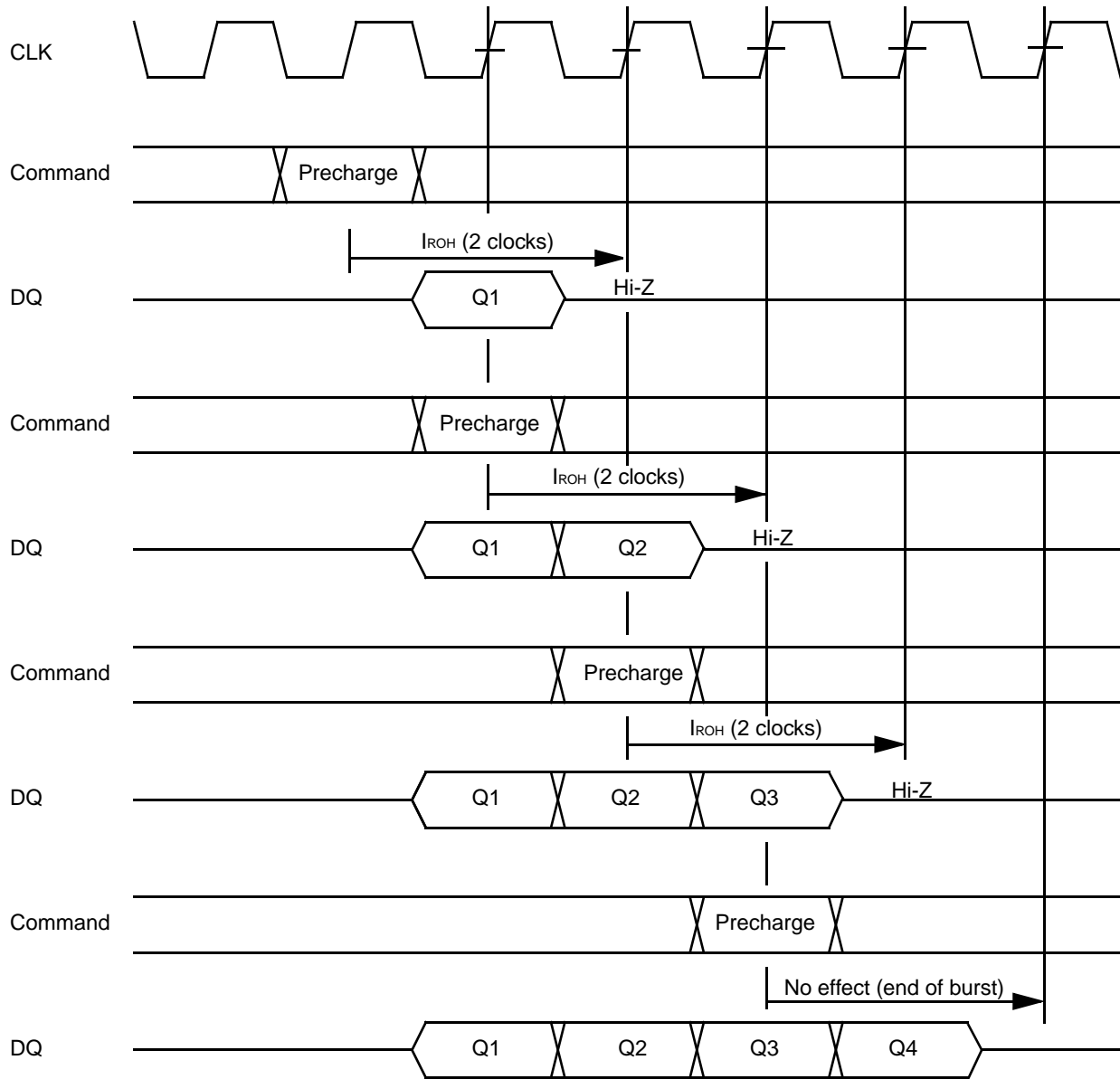
TIMING DIAGRAM - 6 : PRECHARGE TIMING (APPLIED TO THE SAME BANK)



Note: Precharge means 'PRE' or 'PALL'.

MB81F161622C-60/-70/-80/-80L

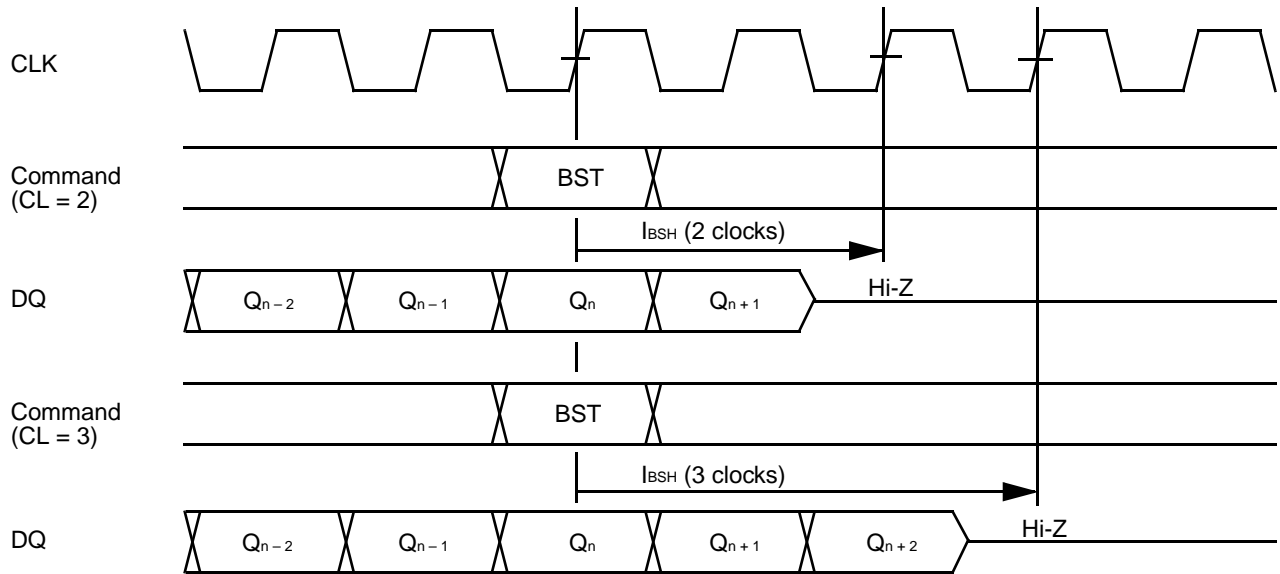
TIMING DIAGRAM - 7 : READ INTERRUPTED BY PRECHARGE (Example @ CL = 2, BL = 4)



Note: In case of CL = 2, the t_{ROH} is 2 clock.
 In case of CL = 3, the t_{ROH} is 3 clock.
 Precharge means 'PRE' or 'PALL'.

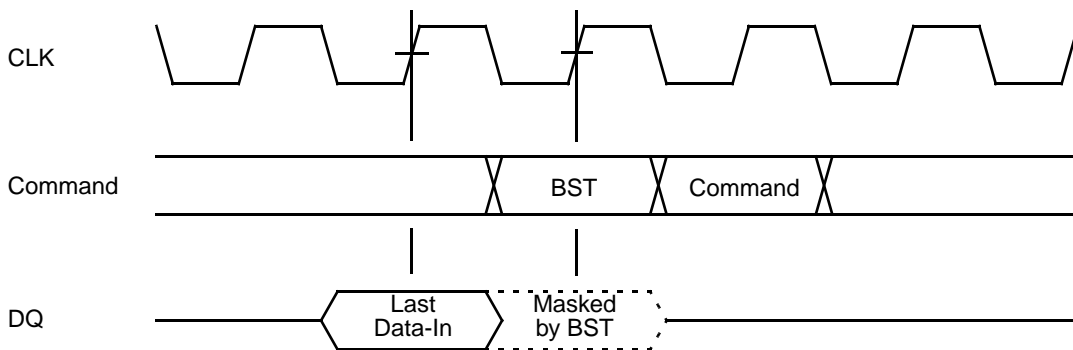
MB81F161622C-60/-70/-80/-80L

TIMING DIAGRAM - 8 : READ INTERRUPTED BY BURST STOP (Example @ BL = Full Column)



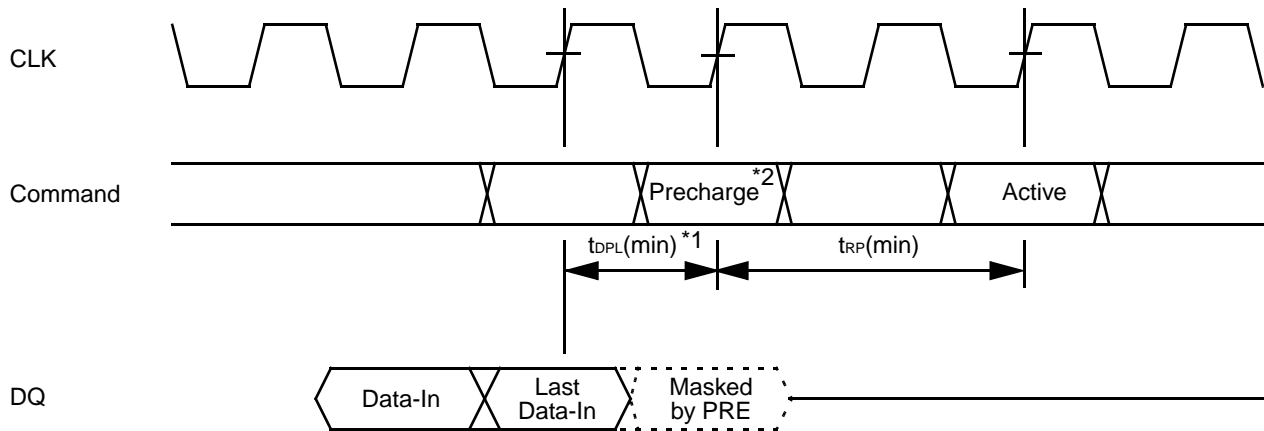
Note: The selection of Auto-precharge option is illegal during the full column burst operation except Write command at BURST READ & SINGLE WRITE mode.

TIMING DIAGRAM - 9 : WRITE INTERRUPT BY BURST STOP (Example @ CL = 2)



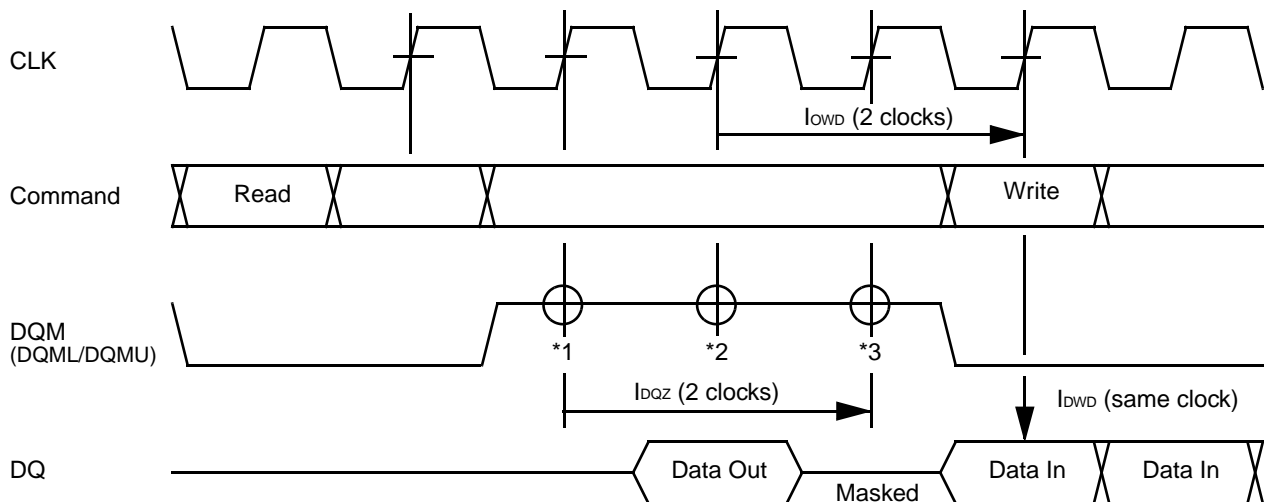
MB81F161622C-60/-70/-80/-80L

TIMING DIAGRAM - 10 : WRITE INTERRUPTED BY PRECHARGE (Example @ CL = 3)



- Notes:**
- *1. The precharge command (PRE) should only be issued after the t_{DPL} of final data input, is satisfied.
 - *2. Precharge means 'PRE' or 'PALL'.

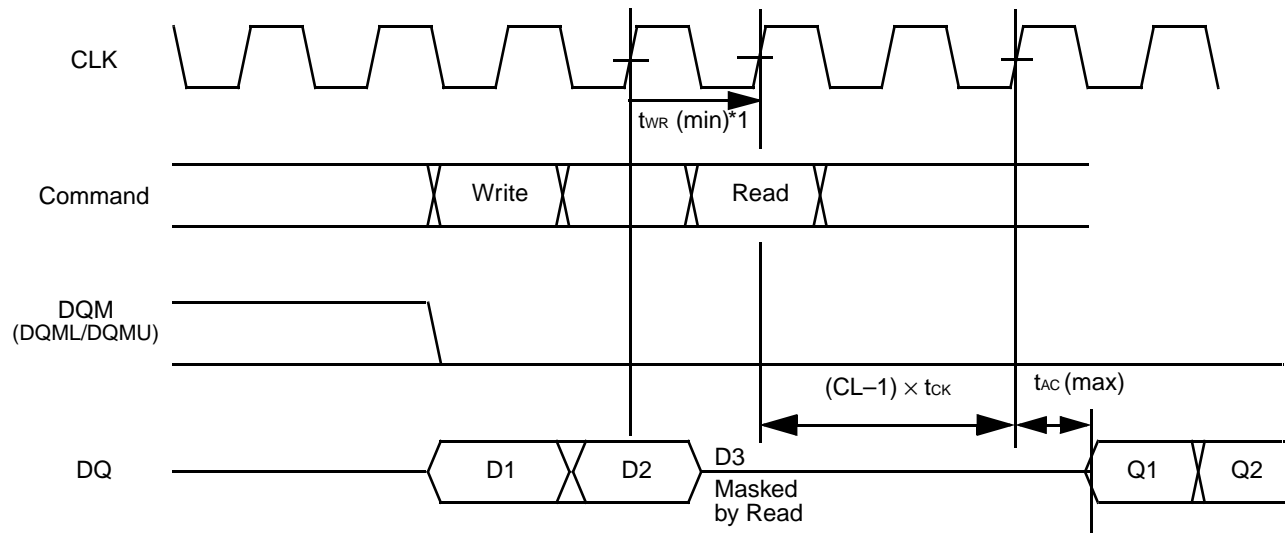
TIMING DIAGRAM - 11 : READ INTERRUPTED BY WRITE (Example @ CL = 3, BL = 4)



- Notes:**
- *1. First DQM makes high-impedance state High-Z between last output and first input data.
 - *2. Second DQM makes internal output data mask to avoid bus contention.
 - *3. Third DQM in illustrated above also makes internal output data mask. If burst read ends (final data output) at or after the second clock of burst write, this third DQM is required to avoid internal bus contention.

MB81F161622C-60/-70/-80/-80L

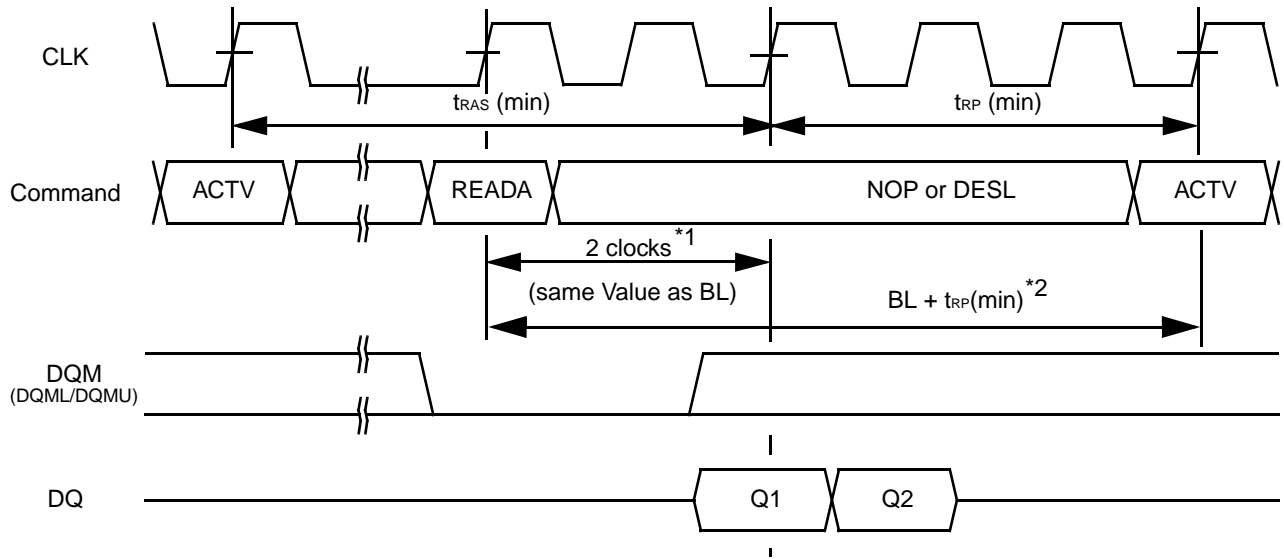
TIMING DIAGRAM - 12 : WRITE TO READ TIMING (Example @ CL = 3, BL = 4)



Note: *1. Read command should be issued after t_{WR} of final data input is satisfied if read command is applied to the same bank.

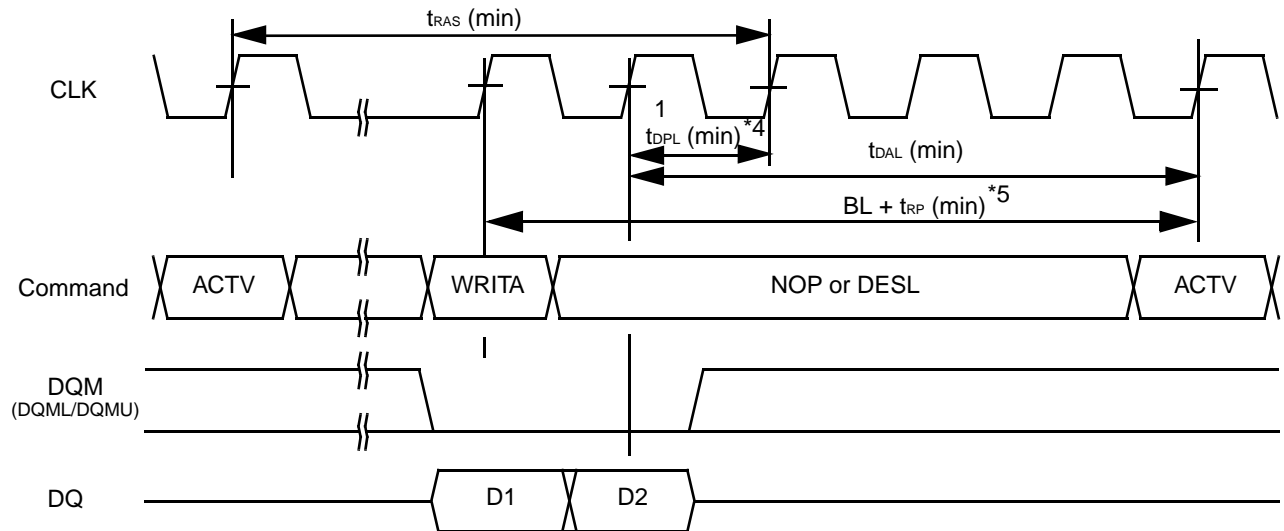
MB81F161622C-60/-70/-80/-80L

TIMING DIAGRAM - 13 : READ WITH AUTO-PRECHARGE
(Example @ CL = 2, BL = 2 Applied to same bank)



- Notes:** *1. Precharge at Read with Auto-precharge command (READA) is started from number of clocks that is the same as Burst Length (BL) after READA command is asserted.
*2. Next ACTV command should be issued after $BL + t_{RP}(\text{min})$ from READA command.

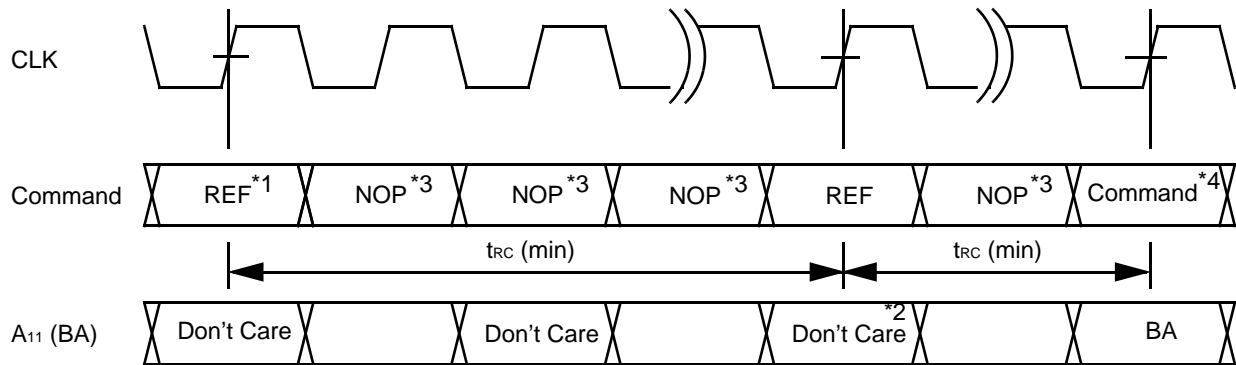
TIMING DIAGRAM - 14 : WRITE WITH AUTO-PRECHARGE *1,*2,*3
(Example @ CL = 2, BL = 2 Applied to same bank)



- Notes:** *1. Precharge at write with Auto-precharge is started after the t_{DPL} from the end of burst.
*2. Even if the final data is masked by DQM, the precharge does not start the clock of final data input.
*3. Once auto precharge command is asserted, no new command within the same bank can be issued.
*4. Auto-precharge command doesn't affect at full column burst operation except Burst Read & Single Write mode.
*5. Next command should be issued after $BL + t_{RP}(\text{min})$ at CL = 2, $BL + 1 + t_{RP}(\text{min})$ at CL = 3 from WRITEA command.

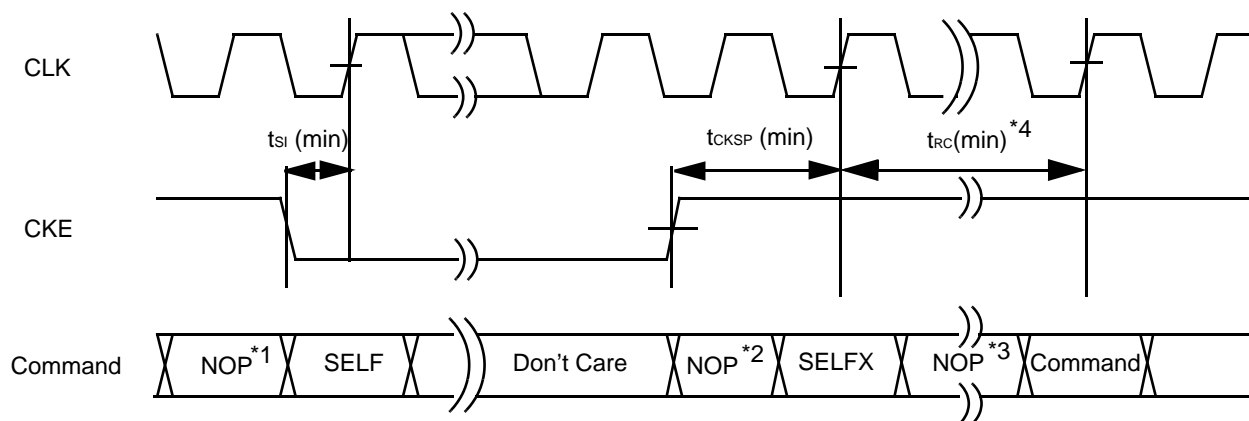
MB81F161622C-60/-70/-80/-80L

TIMING DIAGRAM - 15 : AUTO-REFRESH TIMING



- Notes:**
- *1. All banks should be precharged prior to the first Auto-refresh command (REF).
 - *2. Bank select is ignored at REF command. The refresh address and bank select are selected by internal refresh counter.
 - *3. Either NOP or DESL command should be asserted during t_{RRD} and t_{RC} period while Auto-refresh mode.
 - *4. Any activation command such as ACTV or MRS command other than REF command should be asserted after t_{RC} from the last REF command.

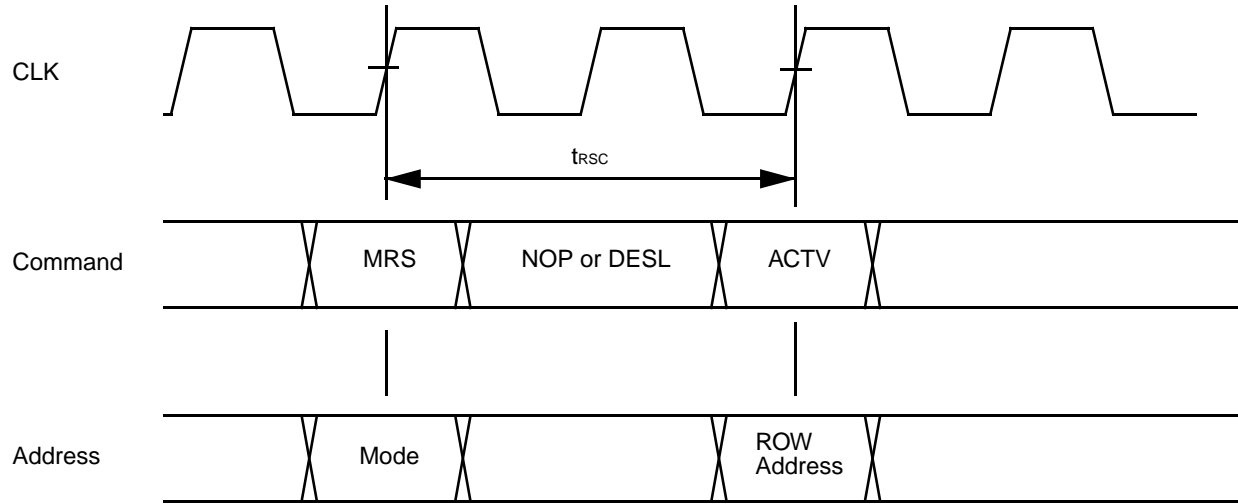
TIMING DIAGRAM - 16 : SELF-REFRESH ENTRY AND EXIT TIMING



- Notes:**
- *1. Precharge command (PRE or PALL) should be asserted if any bank is active prior to Self-refresh Entry command (SELF).
 - *2. The Self-refresh Exit command (SELFX) is latched after t_{CKSP} (min). It is recommended to apply NOP command in conjunction with CKE. It is also recommended to apply minimum of 4 clocks to stabilize external clock prior to SELFX command.
 - *3. Either NOP or DESL command can be used during t_{RC} period.
 - *4. CKE should be held High within t_{RC}(min) period after t_{CKSP}

MB81F161622C-60/-70/-80/-80L

TIMING DIAGRAM - 17 : MODE REGISTER SET TIMING



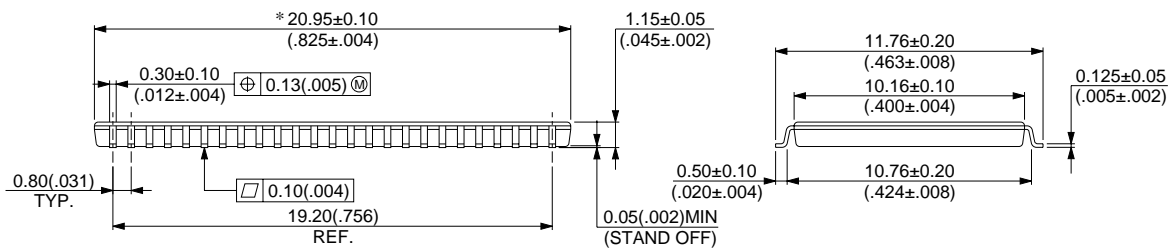
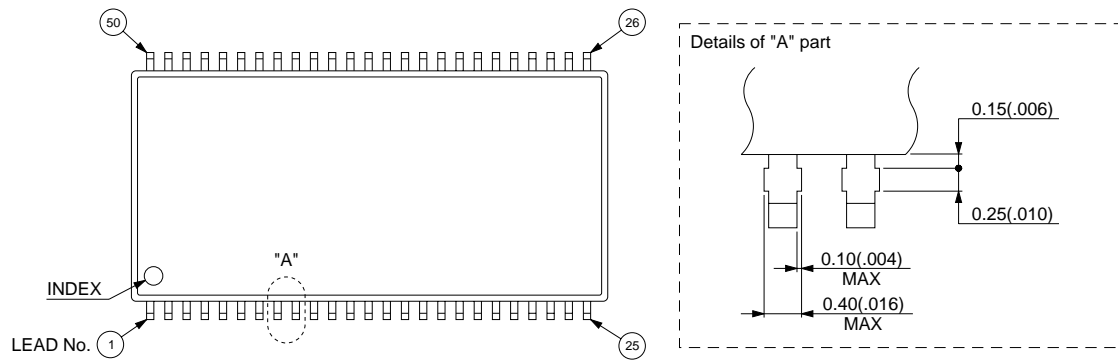
Note: The Mode Register Set command (MRS) should be only asserted after all banks have been precharged.

MB81F161622C-60/-70/-80/-80L

■ PACKAGE DIMENSION

50-pin plastic TSOP (II)
(FPT-50P-M05)

* Resin protrusion. (Each side: 0.15 (.006) Max)



© 1995 FUJITSU LIMITED F50005S-2C-1

Dimensions in mm (inches)

MB81F161622C-60/-70/-80/-80L

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-8588, Japan
Tel: 81(44) 754-3763
Fax: 81(44) 754-3329

<http://www.fujitsu.co.jp/>

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, USA
Tel: (408) 922-9000
Fax: (408) 922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: (800) 866-8608
Fax: (408) 922-9179

<http://www.fujitsumicro.com/>

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Am Siebenstein 6-10
D-63303 Dreieich-Buchsschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

<http://www.fujitsu-edc.com/>

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE LTD
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

<http://www.fmap.com.sg/>

F9910

© FUJITSU LIMITED Printed in Japan

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION:

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.