SONY

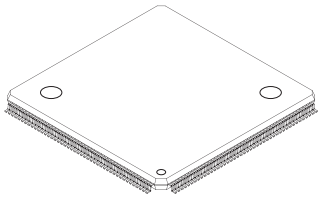
CXD3531R

Digital Signal Driver/Timing Generator

Description

The CXD3531R incorporates digital signal processor type RGB driver, color shading correction and timing generator functions onto a single IC. Operation is possible with a system clock up to 100 [MHz] (max.). This IC can process video signals in bands up to 100MHz, and can output the timing signals for driving various Sony LCD panels.

176 pin LQFP (Plastic)



Features

- Various picture quality adjustment functions such as user adjustment, white balance adjustment and gamma correction
- OSD MIX, black frame processing, mute and limiter functions
- LCD panel color shading correction function
- LCD panel vertical stripe correction function
- Drives various Sony data projector LCD panels
- Drives Sony dot/line inversion drive panel
- Controls the CXA3562AR and CXA7004R sample-and-hold drivers
- Line inversion and field inversion signal generation
- Supports AC drive of LCD panels during no signal
- On-chip serial interface
- The data of gamma correction and color shading correction can be downloaded automatically from the external EEPROM.

Applications

LCD projectors and other video equipment

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (V_{SS} = 0V)

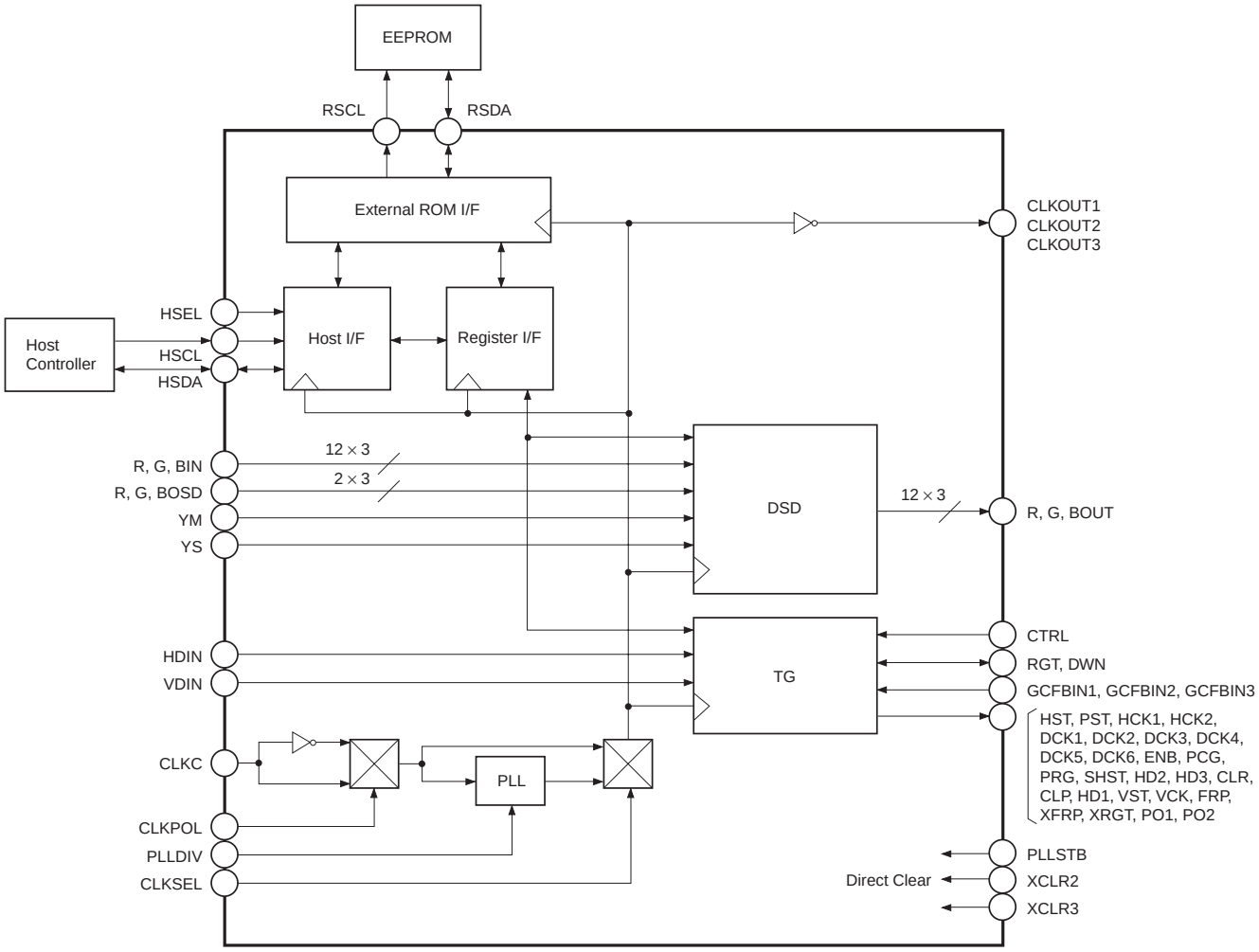
• Supply voltage	V_{DD}	V_{SS} – 0.5 to +2.5	V
	V_{DE}	V_{SS} – 0.5 to +4.5	V
	V_{DDA}	V_{SS} – 0.5 to +4.5	V
• Input voltage	V_I	V_{SS} – 0.3 to V_{DE} + 0.3	V
• Output voltage	V_O	V_{SS} – 0.3 to V_{DE} + 0.3	V
• Storage temperature	Tstg	–55 to +125	°C
• Junction temperature	Tj	125	°C

Recommended Operating Conditions

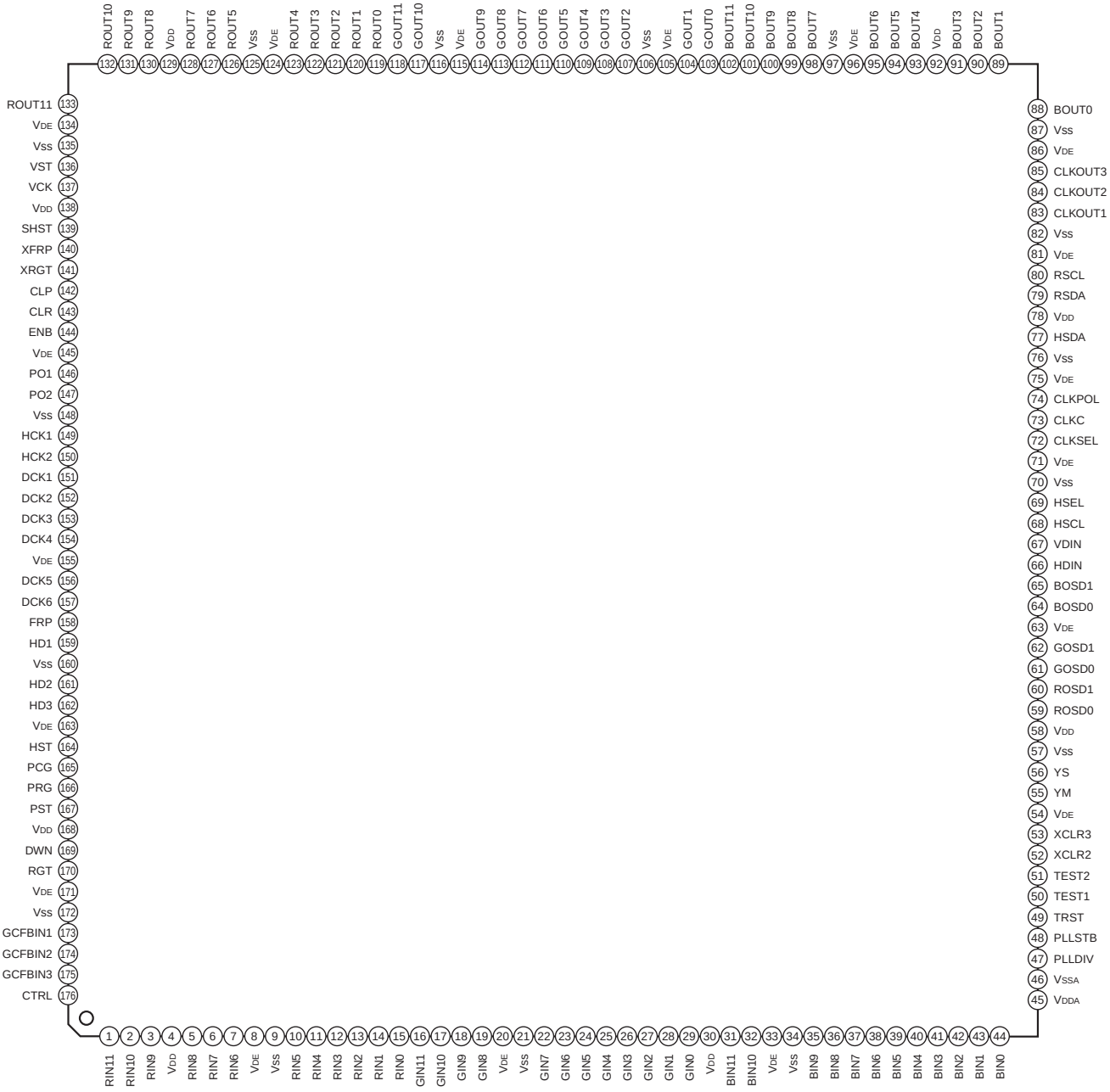
• Supply voltage	V_{DD}	1.65 to 1.95	V
	V_{DE}	3.0 to 3.6	V
	V_{DDA}	3.0 to 3.6	V
• Operating temperature	Topr	–20 to +75	°C

E02Y60-PS

Block Diagram



Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	I/O	Description	Input pin processing for open status
1	RIN11	I	Red data input	—
2	RIN10	I	Red data input	—
3	RIN9	I	Red data input	—
4	V_{DD}	—	Internal operation power supply	—
5	RIN8	I	Red data input	—
6	RIN7	I	Red data input	—
7	RIN6	I	Red data input	—
8	V_{DE}	—	I/O power supply	—
9	V_{SS}	—	GND	—
10	RIN5	I	Red data input	—
11	RIN4	I	Red data input	—
12	RIN3	I	Red data input	—
13	RIN2	I	Red data input	—
14	RIN1	I	Red data input	—
15	RIN0	I	Red data input	—
16	GIN11	I	Green data input	—
17	GIN10	I	Green data input	—
18	GIN9	I	Green data input	—
19	GIN8	I	Green data input	—
20	V_{DE}	—	I/O power supply	—
21	V_{SS}	—	GND	—
22	GIN7	I	Green data input	—
23	GIN6	I	Green data input	—
24	GIN5	I	Green data input	—
25	GIN4	I	Green data input	—
26	GIN3	I	Green data input	—
27	GIN2	I	Green data input	—
28	GIN1	I	Green data input	—
29	GIN0	I	Green data input	—
30	V_{DD}	—	Internal operation power supply	—
31	BIN11	I	Blue data input	—
32	BIN10	I	Blue data input	—
33	V_{DE}	—	I/O power supply	—
34	V_{SS}	—	GND	—
35	BIN9	I	Blue data input	—
36	BIN8	I	Blue data input	—
37	BIN7	I	Blue data input	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
38	BIN6	I	Blue data input	—
39	BIN5	I	Blue data input	—
40	BIN4	I	Blue data input	—
41	BIN3	I	Blue data input	—
42	BIN2	I	Blue data input	—
43	BIN1	I	Blue data input	—
44	BIN0	I	Blue data input	—
45	V_{DDA}	—	PLL power supply	—
46	V_{SSA}	—	PLL GND	—
47	PLLDIV	I	PLL operation mode selection (H: 50MHz or less, L: 50MHz or more)	L
48	PLLSTB	I	PLL standby pin (H: PLL standby)	—
49	TRST	I	Test pin (Connect to GND.)	L
50	TEST1	I	Test pin (Connect to GND.)	L
51	TEST2	I	Test pin (Connect to GND.)	L
52	XCLR2	I	External clear (L: reset)	L
53	XCLR3	I	External clear (L: reset)	L
54	V_{DE}	—	I/O power supply	—
55	YM	I	OSD YM input	L
56	YS	I	OSD YS input	L
57	V_{SS}	—	GND	—
58	V_{DD}	—	Internal operation power supply	—
59	ROSD0	I	OSD red data input	—
60	ROSD1	I	OSD red data input	—
61	GOSD0	I	OSD green data input	—
62	GOSD1	I	OSD green data input	—
63	V_{DE}	—	I/O power supply	—
64	BOSD0	I	OSD blue data input	—
65	BOSD1	I	OSD blue data input	—
66	HDIN	I	Horizontal sync signal input	—
67	VDIN	I	Vertical sync signal input	—
68	HSCL	I	Serial bus clock (host I/F)	—
69	HSEL	I	Serial bus slave address selection signal input	—
70	V_{SS}	—	GND	—
71	V_{DE}	—	I/O power supply	—
72	CLKSEL	I	Internal clock selection (H: PLL through, L: PLL oscillation)	L
73	CLKC	I	Clock input (CMOS input)	—
74	CLKPOL	I	Internal clock polarity selection (H: inverted, L: non-inverted)	L

Pin No.	Symbol	I/O	Description	Input pin processing for open status
75	V_{DE}	—	I/O power supply	—
76	V_{SS}	—	GND	—
77	HSDA	I/O	Serial bus data I/O (host I/F)	—
78	V_{DD}	—	Internal operation power supply	—
79	RSDA	I/O	Serial bus data I/O (external ROM I/F)	—
80	RSCL	O	Serial bus clock I/O (external ROM I/F)	—
81	V_{DE}	—	I/O power supply	—
82	V_{SS}	—	GND	—
83	CLKOUT1	O	Internal clock output (inverted output)	—
84	CLKOUT2	O	Internal clock output (inverted output)	—
85	CLKOUT3	O	Internal clock output (inverted output)	—
86	V_{DE}	—	I/O power supply	—
87	V_{SS}	—	GND	—
88	BOUT0	O	Blue data output	—
89	BOUT1	O	Blue data output	—
90	BOUT2	O	Blue data output	—
91	BOUT3	O	Blue data output	—
92	V_{DD}	—	Internal operation power supply	—
93	BOUT4	O	Blue data output	—
94	BOUT5	O	Blue data output	—
95	BOUT6	O	Blue data output	—
96	V_{DE}	—	I/O power supply	—
97	V_{SS}	—	GND	—
98	BOUT7	O	Blue data output	—
99	BOUT8	O	Blue data output	—
100	BOUT9	O	Blue data output	—
101	BOUT10	O	Blue data output	—
102	BOUT11	O	Blue data output	—
103	GOUT0	O	Green data output	—
104	GOUT1	O	Green data output	—
105	V_{DE}	—	I/O power supply	—
106	V_{SS}	—	GND	—
107	GOUT2	O	Green data output	—
108	GOUT3	O	Green data output	—
109	GOUT4	O	Green data output	—
110	GOUT5	O	Green data output	—
111	GOUT6	O	Green data output	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
112	GOUT7	O	Green data output	—
113	GOUT8	O	Green data output	—
114	GOUT9	O	Green data output	—
115	V_{DE}	—	I/O power supply	—
116	V_{SS}	—	GND	—
117	GOUT10	O	Green data output	—
118	GOUT11	O	Green data output	—
119	ROUT0	O	Red data output	—
120	ROUT1	O	Red data output	—
121	ROUT2	O	Red data output	—
122	ROUT3	O	Red data output	—
123	ROUT4	O	Red data output	—
124	V_{DE}	—	I/O power supply	—
125	V_{SS}	—	GND	—
126	ROUT5	O	Red data output	—
127	ROUT6	O	Red data output	—
128	ROUT7	O	Red data output	—
129	V_{DD}	—	Internal operation power supply	—
130	ROUT8	O	Red data output	—
131	ROUT9	O	Red data output	—
132	ROUT10	O	Red data output	—
133	ROUT11	O	Red data output	—
134	V_{DE}	—	I/O power supply	—
135	V_{SS}	—	GND	—
136	VST	O	Vertical display start timing pulse output	—
137	VCK	O	Vertical display transfer clock output	—
138	V_{DD}	—	Internal operation power supply	—
139	SHST	O	SHST output	—
140	XFRP	O	AC drive inversion timing pulse output (reversed polarity of FRP)	—
141	XRGT	O	Horizontal scan direction switching signal output (reversed polarity of RGT)	—
142	CLP	O	CLP pulse output	—
143	CLR	O	CLR pulse output	—
144	ENB	O	Gate enable pulse output	—
145	V_{DE}	—	I/O power supply	—
146	PO1	O	Parallel output 1	—
147	PO2	O	Parallel output 2	—
148	V_{SS}	—	GND	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
149	HCK1	O	Horizontal display transfer clock output 1	—
150	HCK2	O	Horizontal display transfer clock output 2	—
151	DCK1	O	DCK1 pulse output	—
152	DCK2	O	DCK2 pulse output	—
153	DCK3	O	DCK3 pulse output	—
154	DCK4	O	DCK4 pulse output	—
155	V_{DE}	—	I/O power supply	—
156	DCK5	O	DCK5 pulse output	—
157	DCK6	O	DCK6 pulse output	—
158	FRP	O	AC drive inversion timing pulse output	—
159	HD1	O	Horizontal auxiliary pulse output 1	—
160	V_{SS}	—	GND	—
161	HD2	O	Horizontal auxiliary pulse output 2	—
162	HD3	O	Horizontal auxiliary pulse output 3	—
163	V_{DE}	—	I/O power supply	—
164	HST	O	Horizontal display start timing pulse	—
165	PCG	O	Collective precharge timing pulse output	—
166	PRG	O	2-step precharge timing pulse output	—
167	PST	O	Dot sequential precharge start timing pulse output	—
168	V_{DD}	—	Internal operation power supply	—
169	DWN	I/O	Vertical scan direction switching signal I/O	—
170	RGT	I/O	Horizontal scan direction switching signal I/O	—
171	V_{DE}	—	I/O power supply	—
172	V_{SS}	—	GND	—
173	GCFBIN1	I	GCFBIN pulse input 1	—
174	GCFBIN2	I	GCFBIN pulse input 2	—
175	GCFBIN3	I	GCFBIN pulse input 3	—
176	CTRL	I	Scan direction control method switching (L: internal register, H: external)	L

Electrical Characteristics

DC Characteristics

(Topr = –20 to +75°C, V_{SS} = 0V)

Item	Symbol	Applicable pins	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	—	—	1.65	1.8	1.95	V
	V_{DE}	—	—	3.0	3.3	3.6	
Input voltage 1	V_{IH1}	*1	CMOS input cell	2.0	—	—	
	V_{IL1}			—	—	0.8	
Input voltage 2	V_{IH2}	HDIN, VDIN, HSCL, HSDA, RSCL, RSDA	CMOS Schmitt trigger input cell	0.7V_{DE}	—	V_{DE} + 0.3	
	V_{IL2}			–0.3	—	0.2V_{DE}	
Output voltage	V_{OH}	All output pins	—	V_{DE} – 0.4	—	—	
	V_{OL}		—	—	—	0.4	
Power consumption	PD*2	—	CLKC = 100MHz	—	—	1100	mW

*1 Input pins other than those indicated in items Input voltage 2 and Input voltage 3.

*2 Tj [°C] ≥ Toprmax [°C] + θja [°C/W] × PD [W].

AC Characteristics

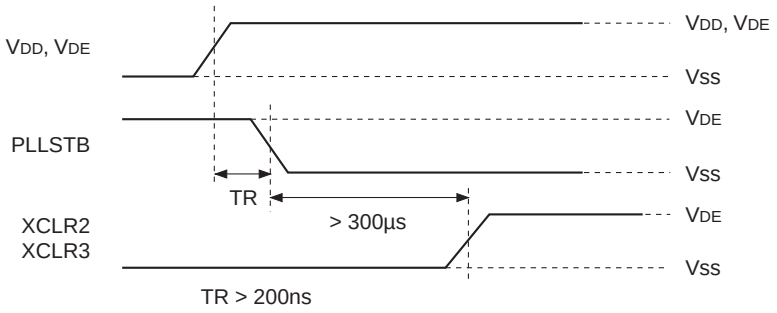
(Topr = –20 to +75°C, V_{DD} = 1.8 ± 0.15V, V_{DE} = 3.3 ± 0.3V, V_{SS} = 0V)

Item	Symbol	Applicable pins	Conditions	Min.	Typ.	Max.	Unit
Clock input period	—	CLKC	—	10.0	—	—	ns
Input setup time	tis	RGB input, OSD input, HDIN, VDIN	—	2.0	—	—	
Input hold time	tih		—	2.0	—	—	
Input setup time	tis	HSCL, HSDA, RSDA	—	5.0	—	—	
Input hold time	tih		—	5.0	—	—	
Output rise/fall delay time	tor/tof	*3	CL = 20pF	1.0	—	7.0	
Output rise/fall delay time	tor/tof	FRP, XFRP, SHST, PRG	CL = 50pF	1.0	—	7.0	
Cross-point time difference	Δt	HCK1, HCK2, DCK1, DCK2, DCK3, DCK4, DCK5, DCK6	CL = 20pF	–5.0	—	5.0	
HCK1 duty	th/(th + tl)	HCK1	CL = 20pF	48	50	52	%
HCK2 duty	tl/(th + tl)	HCK2	CL = 20pF	48	50	52	
Phase compensation PLL operating frequency	—	—	PLLDIV = V	50	—	100	MHz
			PLLDIV = H	25	—	55	

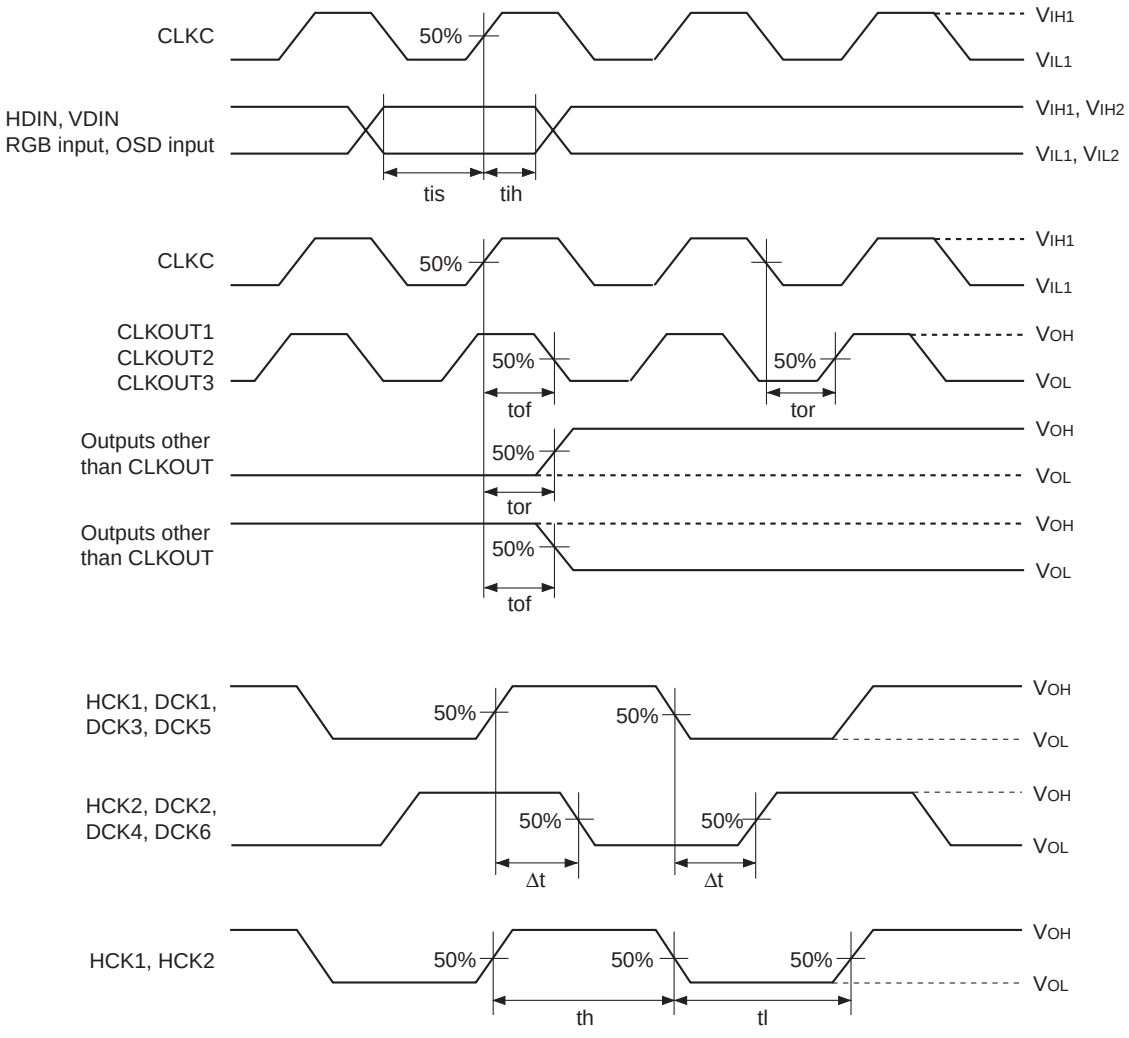
*3 Output pins other than FRP, XFRP, SHST and PRG.

Power-on and Initialization of Internal Circuit

As for this IC, two systems of supply voltage should be turned on simultaneously. The initialization of the internal circuit should be also performed by maintaining the system clear pin at low during the specified time after setting the supply voltage in the range of recommended operating conditions and stabilizing as shown in the figure below. Keep in mind that the internal circuit may not be initialized correctly if system clear cancellation is performed before the supply voltage is set in the range of the recommended operating conditions.



Timing Definition



Description of Operation

1. Description of Input Pins

(a) Initializing pins (PLLSTB, XCLR2 and XCLR3)

Internal PLL is initialized by setting PLLSTB (Pin 48) to 1 and internal circuit is initialized by setting XCLR2 (Pin 52) to 0. In addition, RGB output is initialized (preset) by setting XCLR3 (Pin 53) to 0.
Initialization should be performed when power is turned on. Be sure to perform power supply on according to an initialization procedure.

(b) Sync signal input pins (HDIN and VDIN)

Horizontal and vertical separate sync signals are input to HDIN (Pin 66) and VDIN (Pin 67), respectively. The CXD3531R supports only non-interlace sync signals with a dot clock of 100MHz or less.

(c) Master clock input pins (CLKC, CLKSEL and CLKPOL)

Phase comparison is performed by an external circuit and a clock synchronized to the sync signal is input. The master clock input pin has CLKC (Pin 73) for CMOS level input.

CLKPOL: 0 = Input clock is non-inverted; 1 = Input clock is inverted
CLKSEL: 0 = PLL oscillation; 1 = PLL through

(d) PLL setting pin (PLLDIV)

PLLDIV (Pin 47) sets the divider setting of the internal phase compensation PLL circuit. The setting values for master clock frequency are as follows.

PLLDIV: 0 = 55 to 100MHz; 1 = 25 to 50MHz

Note that the frequency of the clock input to the CXD3531R must be within the phase compensation PLL operating range, even during free running.

(e) RGB signal input pins (RIN, GIN and BIN)

These pins input RGB digital signals in 12 bits. The Red signal is input to RIN (Pins 1 to 3, 5 to 7 and 10 to 15), the Green signal to GIN (Pins 16 to 19 and 22 to 29), and the Blue signal to BIN (Pins 31, 32 and 35 to 44) respectively.
RIN0, GIN0 and BIN0 are LSB, and RIN11, GIN11 and BIN11are MSB respectively.

(f) OSD signal input pins (ROSD, GOSD, BOSD, YS and YM)

These pins input OSD signals. The Red signal is input to ROSD (Pins 59 and 60), the Green signal to GOSD (Pins 61 and 62), and the Blue signal to BOSD (Pins 64 and 65) respectively. In addition, the YM signal is input to YM (Pin 55), and the YS signal to YS (Pin 56).

(g) Host serial clock input pin (HSCL)

HSCL (Pin 68) is the clock input pin used to set the I/O timing for serial data from the host. Data is taken from the HSDA pin when the clock signal rises, and data is output to the HSDA pin when the clock signal falls.

(h) Host serial I/O pin (HSDA)

This is the I/O pin for serial data from the host. The output is an open drain, so this pin must be pulled up using an external resistor. It is necessary to switch the input to the HSDA (Pin 77) while the signal level of HSCL is low.

(i) Device address input pin (HSEL)

Simultaneous connection of this IC can be made up to two ICs on the same serial bus. Since a device address is used to identify each of these devices, this pin should be connected to 1 or 0 externally. This 1 and 0 setting drives the device which matches the slave address input from the HSDA pin. When two ICs are used simultaneously, choose a different device address. The slave addresses of this IC used for the HSEL (Pin 69) setting are as follows.

HSEL: 0 = 74h; 1 = 76h

(j) External EEPROM serial clock output pin (RSCL)

RSCL (Pin 80) is the clock output pin used to set the I/O timing of serial data sent to the external EEPROM. The output is an open drain, so this pin must be pulled up using an external resistor. Data is taken from the RSDA pin when the clock signal rises, and data is output to the RSDA pin when the clock signal falls.

(k) External EEPROM serial I/O pin (RSDA)

This is the I/O pin for serial data sent to the external EEPROM. The output is an open drain, so this pin must be pulled up using an external resistor. Also, it is necessary to switch the input to the RSDA (Pin 79) while the signal level of RSCL is low.

(l) Scan direction control system switching pins (RGT, DWN, CTRL)

The I/O direction of the LCD panel scan direction switching pins RGT (Pin 170) and DWN (Pin 169) is set by CTRL (Pin 176).

CTRL: 0 = RGT and DWN are output pins, 1 = RGT and DWN are input pins

When CTRL = 0, RGT and DWN output the respective register setting values. When CTRL = 1, the externally set values are input to RGT and DWN and reflected to the internal operation.

(m) GCFB pulse input pins (GCFBIN)

The GCFBIN (Pins 173, 174 and 175) input the LCD panel internal signal latch pulse.
Set these pins according to the register setting procedure during power-on and at set intervals.

(n) Test pins (TRST, TEST)

TRST (Pin 49) and TEST (Pins 50 and 51) are test pins. Leave these pins open, or connect them to GND.

2. Pipeline Delay of the RGB and OSD Signals

The pipeline delay for the I/O of the RGB signals is 46 clock cycles of the master clock. In addition, the pipeline delay for the OSD, YS and YM signals is 39 clock cycles of the master clock.

3. Serial Bus

The serial bus of this IC consists of a host I/F, external ROM I/F and register I/F.

3-1. Host I/F

With this IC, each register setting and data set to built-in RAM are performed over a serial bus. Bus protocol conforms to I^2C bus specifications. Also, when accessing gamma RAM, always access memory address from odd addresses in 2-byte units. The following restrictions are placed on the host I/F of this IC.

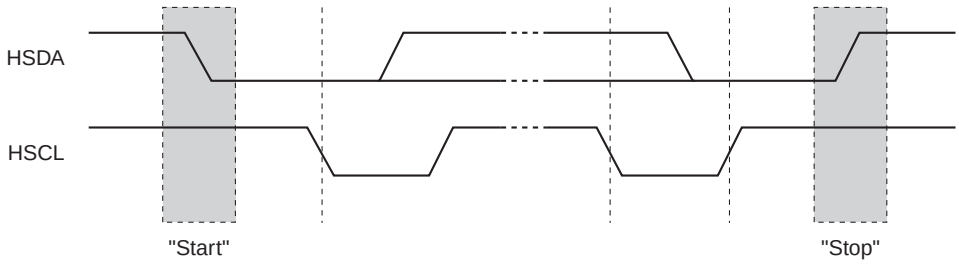
- Only I^2C bus slave operations are performed.
- Standard mode and fast mode are supported. Hs mode is not supported.
- The general call address and start byte of the slave address are not acknowledged.
- C bus compatibility is not supported.
- Acknowledgment is not performed for 10-bit slave addresses.
- Low is not asserted for HSCL. (Wait control is not performed.)

(1) "Start" conditions

Read and write operations enter "Start" status by switching HSDA input from high to low level while HSCL input is high.

(2) "Stop" conditions

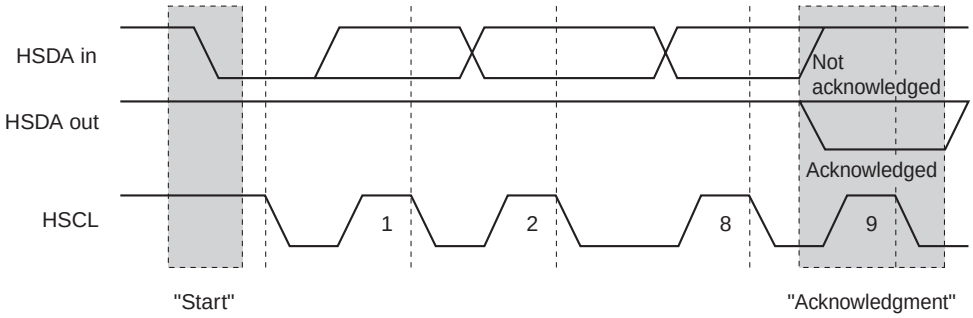
"Stop" results by switching HSDA input from low to high while HSCL input is high. Setting "Stop" status causes read processing to terminate during read operations, and causes the input of write data to terminate during write operations.



"Start" Conditions and "Stop" Conditions

(3) Acknowledgment (ACK)

Acknowledgment is used to indicate whether or not data has been sent/received normally. The "Acknowledgment" of a data transfer is performed after that data transfer when the sender releases the bus on the 9th clock of HSCL and the receiver drives low. If the host is the receiver, the IC is informed by the host that data has ended by the fact that "Acknowledgment" is not generated for the last data sent from the IC.



Acknowledgment on the I²C Bus

(4) Device address specification

After "Start" is sent, a 7-bit slave address and 1-bit read/write code is sent. Read/write operations with this IC start if the input slave address matches the device address set using HSEL. If the device address does not match, "Acknowledgment" is not generated and the system does nothing.

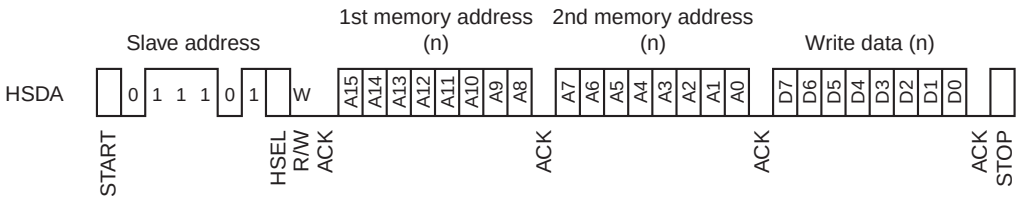
Device Address Word (8 bits)							
Device Code (fixed)						Device Select	R/W Code
0	1	1	1	0	1	HSEL	R/W

* If R/W = 1, read results, if R/W = 0, write results.

Device Address Specification

(5) Byte write operation

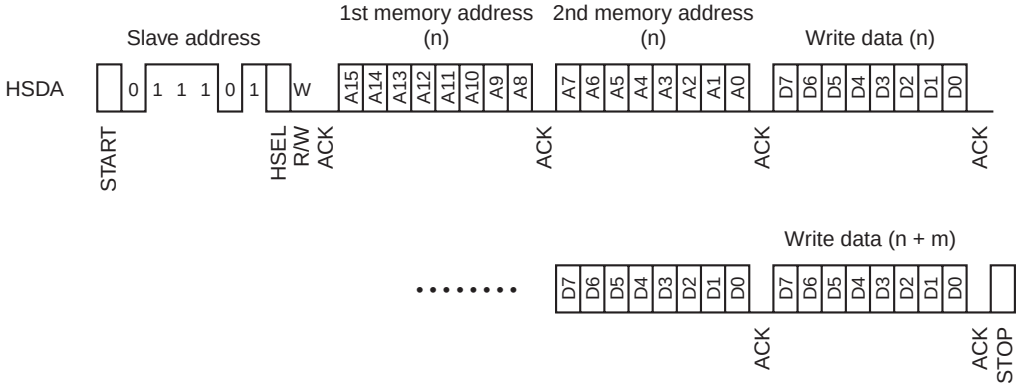
After "Start" is sent, the R/W code is set to low and an 8-bit device address word is input. The IC outputs "Acknowledgment" on the 9th bit and enters write mode. After this, "Acknowledgment" is output every 8 bits after each of the two 8-bit memory addresses are input. Next, "Acknowledgment" is output after 8 bits of write data is input and written to the IC.



Byte Write Operation

(6) Continuous write operation

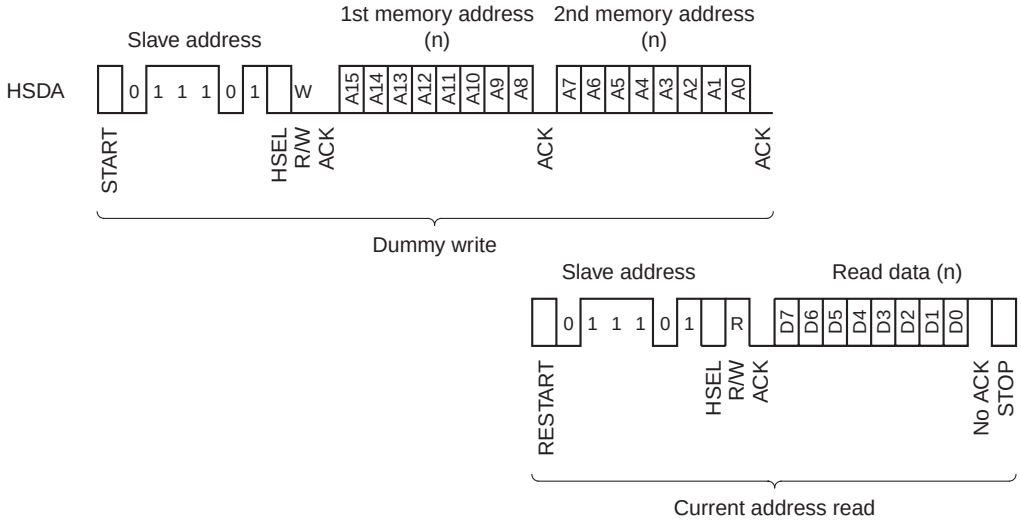
This IC possesses a function which can write data continuously. With the continuous write operation, write data is written in a manner similar to the byte write operation. Continuous write is possible by sending write data continuously before sending "Stop". The address used to write data during the continuous write operation is automatically incremented when each separate write operation terminates.
There is no limit on the number of continuous transfers that are possible to write continuously with this IC.



Continuous Write Operation

(7) Byte read operation

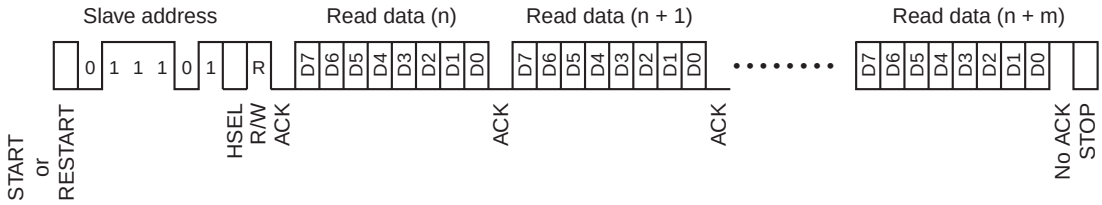
After "Start" is sent, the R/W code is set to low and an 8-bit device address word is input. The IC outputs "Acknowledgment" to the 9th bit and enters write mode. After this, "Acknowledgment" is output every 8 bits after each of the two 8-bit memory addresses are input. Once the addresses are acknowledgment, "Restart" is input, and the R/W code is set to high, an 8-bit device address word is input, and the IC outputs "Acknowledgment" to the 9th bit and enters read mode. Next, 8 bits of read data are output using the address used for the dummy write, and the read operation terminates if "Stop" is input without inputting "Acknowledgment".



Byte Read Operation

(8) Continuous read operation

This IC possesses a function which can read data continuously. With the continuous read operation, data up to the current address is read in a manner similar to the byte read operation. Continuous read is possible by receiving continuous read data and perform "Acknowledgment" before sending "Stop". The address used for reading data during the continuous read operation is automatically incremented when each separate read operation terminates.
There is no limit on the number of continuous transfers that are possible to read continuously with this IC.



Continuous Read Operation

3-2. Conditions for Accessing Gamma RAM and Color Shading RAM

With this IC, there are two way to access the internal RAM: by the host I/F using the I^2C bus and refresh/write-back for sending/receiving data via external ROM I/F. In the case of Gamma RAM, internal RAM must be accessed by the host I/F in 2-byte units, and memory address must be read from or written to even memory addresses. Color shading RAM can be accessed in 1-byte units and there is no restriction on which addresses can be read or written.

It is possible to access internal RAM from each I/F when the conditions given in the following table are established.

GAM_ON	Vertical blanking period	Gamma RAM access
0	—	Yes
1	Vertical blanking period	Yes
1	Outside vertical blanking period	No

* GAM_ON represents the setting value of the DSD register.
* Gamma correction is not performed when GAM_ON is "0", and is performed when GAM_ON is "1".

Conditions for Accessing Gamma RAM

CSC_ON	Vertical blanking period	Color shading RAM access
0	—	Yes
1	Vertical blanking period	Yes
1	Outside vertical blanking period	No

* CSC_ON represents the setting value of the color shading register.
* Color shading correction is not performed when CSC_ON is "0", and is performed when CSC_ON is "1".

Conditions for Accessing Color Shading RAM

GAM_ON must be set to "0" when performing a write-back or forced refresh operation for Gamma RAM. Similarly, CSC_ON must be set to "0" when performing a write-back or forced refresh operation for color shading RAM.
In the case of a self-refresh operation, the start of vertical blanking period is automatically detected and operations start automatically at that time, regardless of how GAM_ON and CSC_ON are set. Therefore, be sure to set the external I^2C ROM transfer count register ROM_TRAN to fit within the vertical blanking period. Furthermore, the vertical blanking period for gamma is set using CSC_HP, CSC_VP, CSC_HNUM, CSC_VNUM, CSC_HINT and CSC_VINT. Make all settings in accordance with the specifications of the video signal attempting to be displayed.

3-3. External ROM I/F

When operating the external ROM I/F, operations start by setting the serial bus register from the host I/F. The serial bus on the ROM side is used to access the external EEPROM that comforms to I^2C bus. Bus protocol conforms to I^2C bus specifications. Also, the following restrictions are placed on the external EEPROM I/F of this IC.

- Only master operations are performed.
- Standard mode and fast mode are supported. Hs mode is not supported.
- Multi-master functions are not supported.
- The general call address and start byte of the slave address are not generated.
- C bus compatibility is not supported.
- A memory address space of up to 512K bytes is supported.
- Wait control by RSCL is not supported.
- 10-bit slave addresses are not supported.

(1) External ROM I/F clock settings

The frequency of the clock signal supplied to the external EEPROM by the RSCL pin is set using RSCL_SEL of the serial bus control registers. Set this value based on the operating frequency of the IC as given in the table below so that the frequency output by the RSCL pin is appropriate for the specifications of the external EEPROM.

RSCL_SEL	Frequency formula of RSCL output
00	$f/2^7$
01	$f/2^8$
10	$f/2^9$
11	$f/2^{10}$

* Enters operating frequency of this IC in "f" in the table.

Example) When operating frequency is 100MHz (RSCL_SEL = 01)

$100 \times 10^3/2^8 = 390.625$kHz

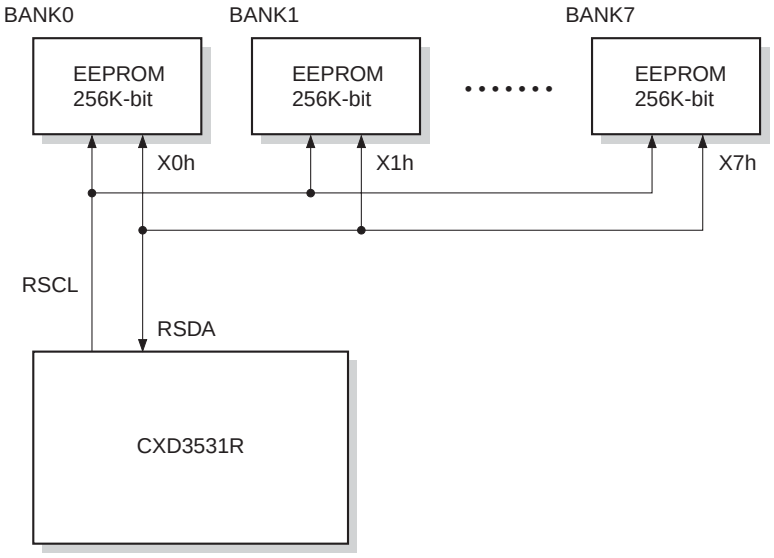
(2) External EEPROM memory capacity setting

With this IC, slave addresses and memory addresses are generated in accordance with the memory capacity set for the external EEPROM. The memory capacity of the external EEPROM is set using ROM_MAP of the serial bus control registers.

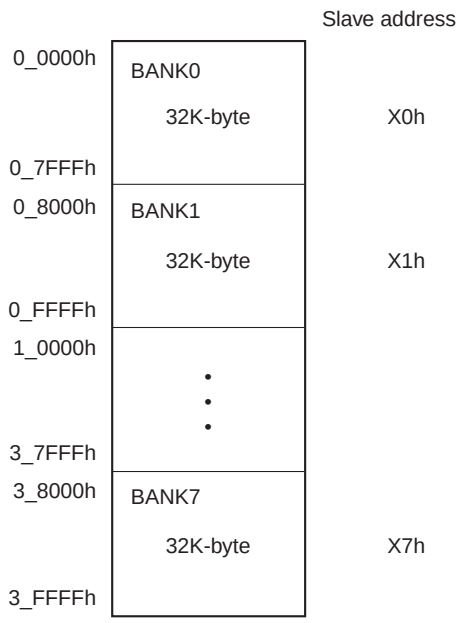
ROM_MAP	Usable memory size
00	512K-bit (65,536 × 8-bit)
01	256K-bit (32,768 × 8-bit)
10	128K-bit (16,384 × 8-bit)
11	64K-bit (8,192 × 8-bit)

[Example] Address output when using eight 256K-bit EEPROMs (ROM_MAP = 01)

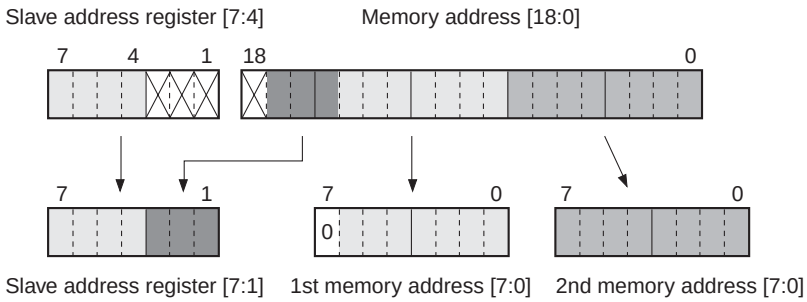
With this IC, the ROM slave address register setting [7:4] is set as is for the serial bus slave address [7:4], and the memory address [17:15] is used for the slave address [3:1]. The memory address [14:0] is used as is for the 1st and 2nd memory addresses. The 1st memory address [7] is fixed to all "0". Furthermore, up to eight external EEPROMs can be connected to this IC.



System Configuration Diagram

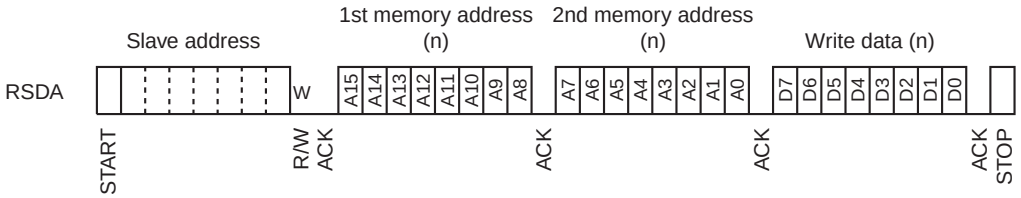


Memory Map
256K-byte space



(3) External ROM I/F slave address setting

The external ROM I/F of this IC transfers data into and out of memory using the serial bus as host I/F. Since operations conform to I^2C bus protocol just as with the host I/F, this section only describes the slave address. To access the external EEPROM, when access conditions are established, "Start" is sent, and then 7 bits representing the slave address are output, and the R/W code is output. "Acknowledgment" is received to the 9th bit from the external EEPROM, and the IC enters either read or write mode. The slave address is determined based on ROM_MAP of the serial bus ROM I/F control register and RSLV_ADDR of the serial bus ROM slave address register as previously described.
The user should set the upper 4 bits of the device address of the EEPROM to be used in RSLV_ADDR and the memory size in ROM_MAP. This allows memory to be used without awareness of memory boundaries of actual memory used for the setting memory space.



Byte Write Operation

(4) Memory location and data size setting for the external EEPROM

Since this IC performs refresh and write-back operations, it is necessary to set which addresses of the external EEPROM gamma data and color shading data have been located in.
The registers used to make these settings are the serial bus ROM gamma data start address register and the I^2C ROM color shading data start address register. By specifying the starting position of the data area in these registers data access from the specified addresses is possible during refresh and write-back operation.
Units of 1K-byte can be used to set the start addresses which can be set in these registers.

In addition, the size of data transferred during refresh and write-back operations is fixed at 2K bytes for each color in the case of gamma data. The number of bytes transferred in the case of color shading data is the value stored in the color shading data size register plus one.

(5) Refresh and write-back operations

This IC includes a function that allows an external EEPROM to automatically refresh the internal RAM. This function has the four modes described below.

- Self-refresh mode
- Forced refresh mode
- Write-back mode
- Refresh stop mode

Each mode is started by writing the specified mode into REF_MODE of the refresh register.

In self-refresh mode, the IC detects that the vertical blanking period has been entered and, using the value specified in the I^2C ROM transfer count register, uses the continuous read operation to transfer data of the size "transfer count plus 1" to the external EEPROM I/F. The data read using the continuous read transfer is written into the internal RAM.
When the transfer of the all data for the data size is completed, the access area for the internal RAM is changed, continuous read transfer is executed indefinitely until self-refresh mode is exited, and refresh operations are automatically carried out on the internal RAM. Also, refresh area can be selected by REF_AREA setting.

In forced refresh mode, continuous read transfer from the external EEPROM is performed for the RAM area specified by REF_RSEL of the refresh RAM select register, and the read data is written to the internal RAM. When the transfer of all data for the specified RAM area is completed, REF_END of the refresh status register set to a flag indicating the operation has ended, and operations stop.
If forced refresh operations are to be performed for the entire internal RAM, first set the refresh RAM select register to gamma RAM (R) and perform the forced refresh operation. Since the refresh RAM select register is automatically set to the next RAM area after all data is transferred, refresh for the entire RAM can be completed by repeating the forced refresh operation five times.

In write-back mode, continuous write transfer is performed from the RAM area specified by REF_RSEL of the refresh RAM select register to the external EEPROM. When the transfer of all data for the specified RAM area is completed, REF_END of the refresh status register set to a flag indicating the operation has ended, and operations stop.
If write-back operations are to be performed for the entire internal RAM, first set the refresh RAM select register to gamma RAM (R) just as for forced refresh operation, and then perform the write-back operation. Since the refresh RAM select register is automatically set to the next RAM area after all data is transferred, write-back for the entire RAM can be completed by repeating the write-back operation five times.

In refresh stop mode, the external ROM I/F does not operate and nothing is output on the serial bus.

(6) Forced reset of the external ROM I/F control circuit

With this IC, forced reset is possible in case a problem occurs with the external ROM I/F and the internal circuit becomes locked. Forced reset initializes only the external ROM I/F control circuit by writing "1" to ROM_RST of the refresh register. Normal operations are allowed after initialization is complete.

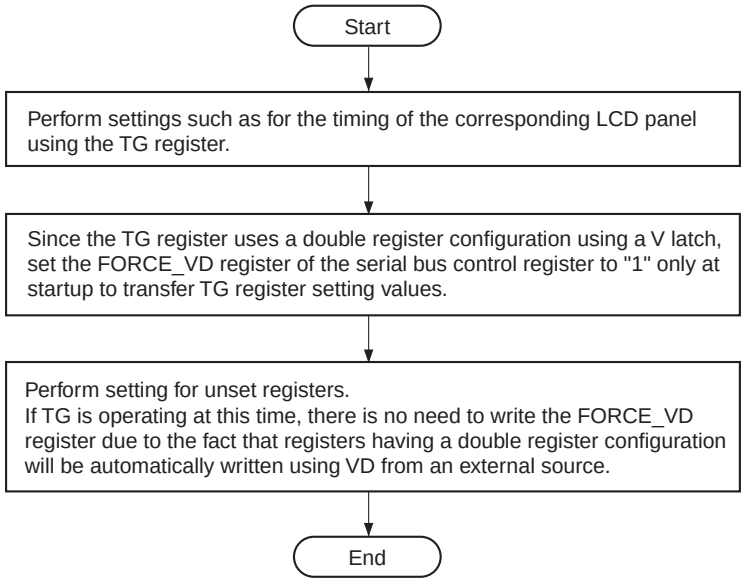
3-4. Register I/F Control Circuit

The register I/F control circuit transfers data between the host I/F and the external ROM I/F. Register data other than RAM data is stored here. Since registers have a double buffer configuration, data in the first buffer is synchronized with the internal VD and reflected in the second buffer, while data in the second buffer is input to each block. Note, however, that data in the serial bus control register has a single buffer configuration.

3-5. Software Flow

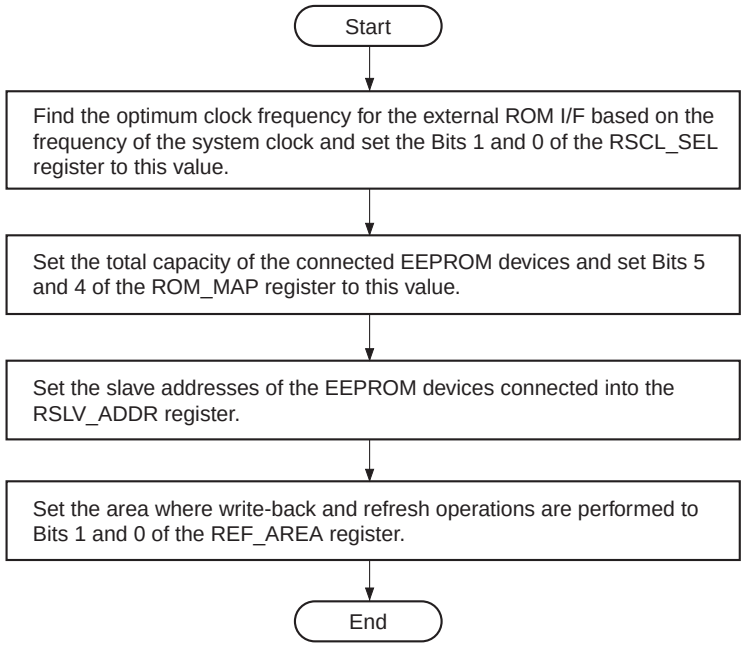
(1) Settings when power is turned on

The following procedure is the setting procedure first performed after power of the IC is turned on. If this procedure is not executed, the internal VD will not be generated and register data cannot be set correctly.



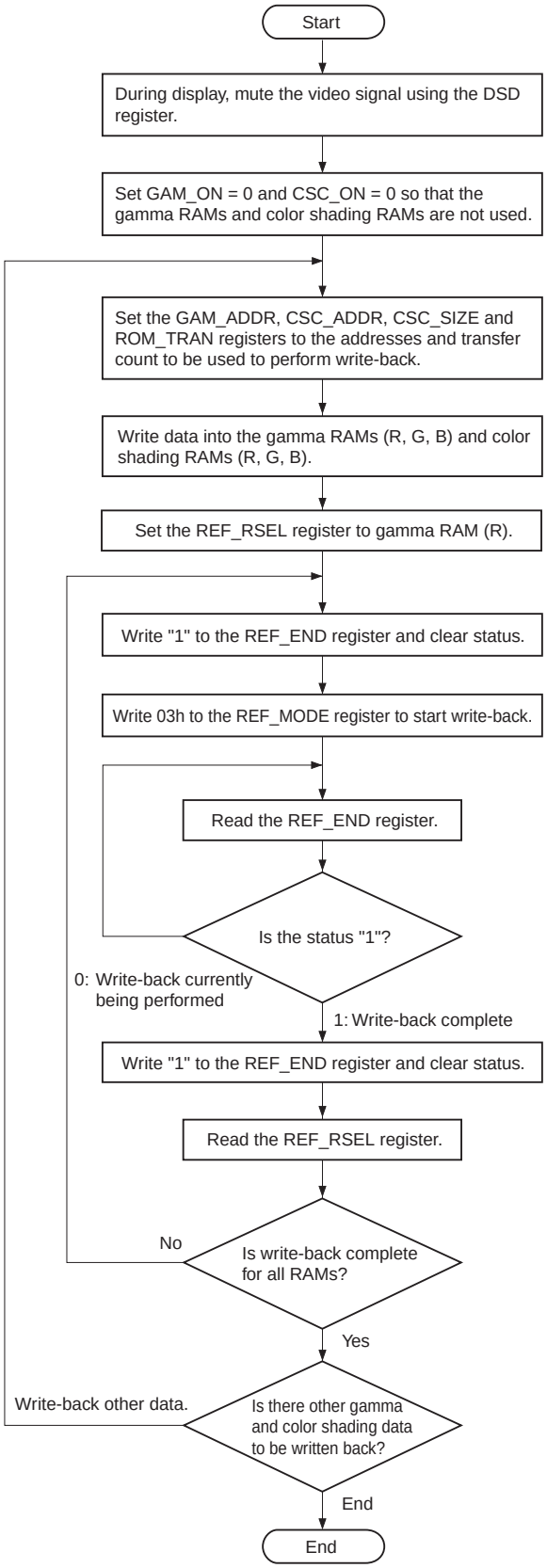
(2) Setting procedure of the serial bus control register

The following procedure is the procedure for setting the serial bus control register in accordance with the external EEPROM to which the IC is connected. Be sure to make settings according to the operating frequency of the IC and the speed, capacity and number of external EEPROMs that are connected.



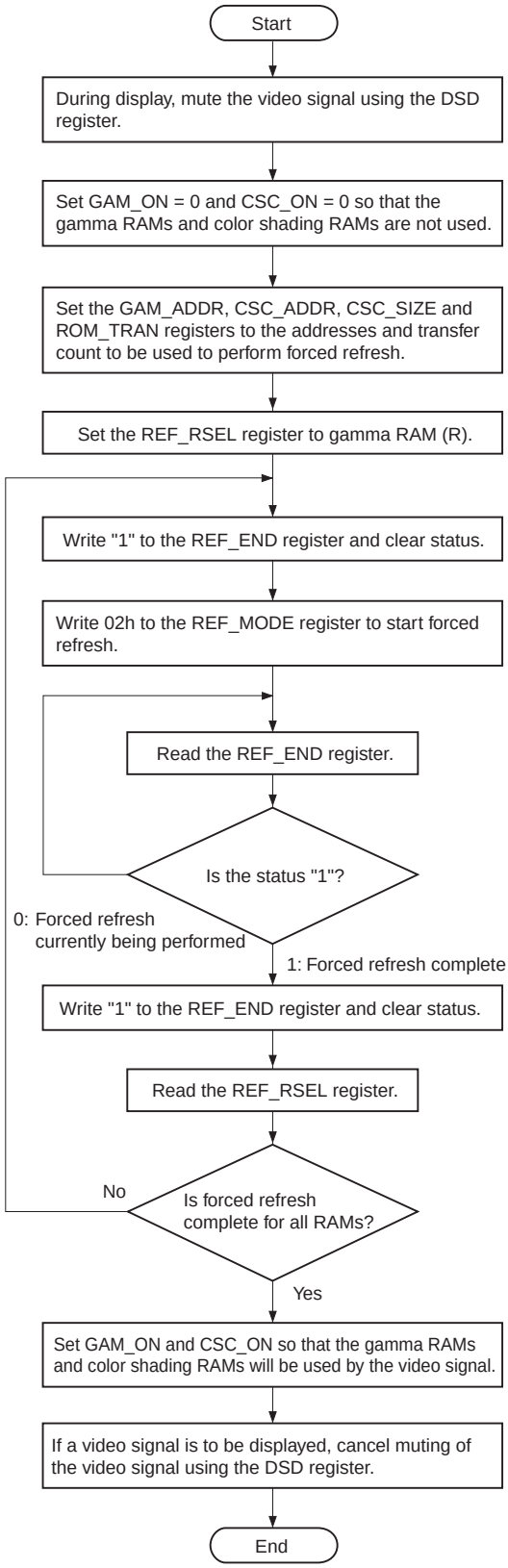
(3) Write-back procedure

The following procedure is the procedure for writing gamma correction and color shading correction data back to the external EEPROM.



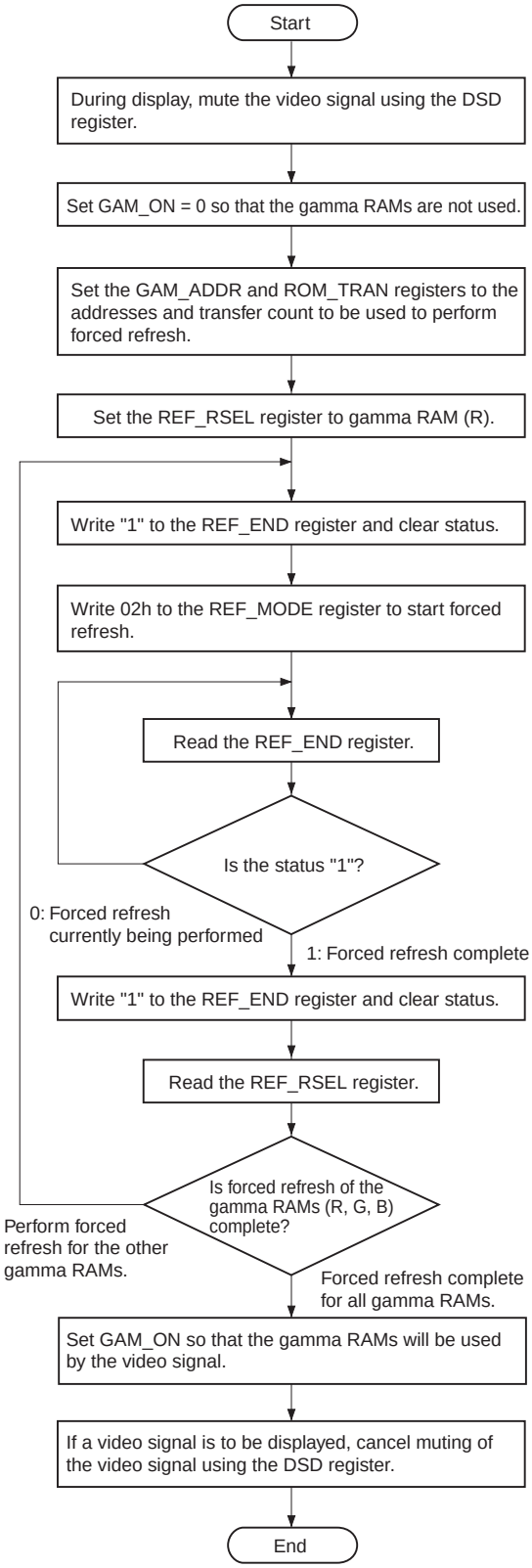
(4) Forced refresh procedure during power-on

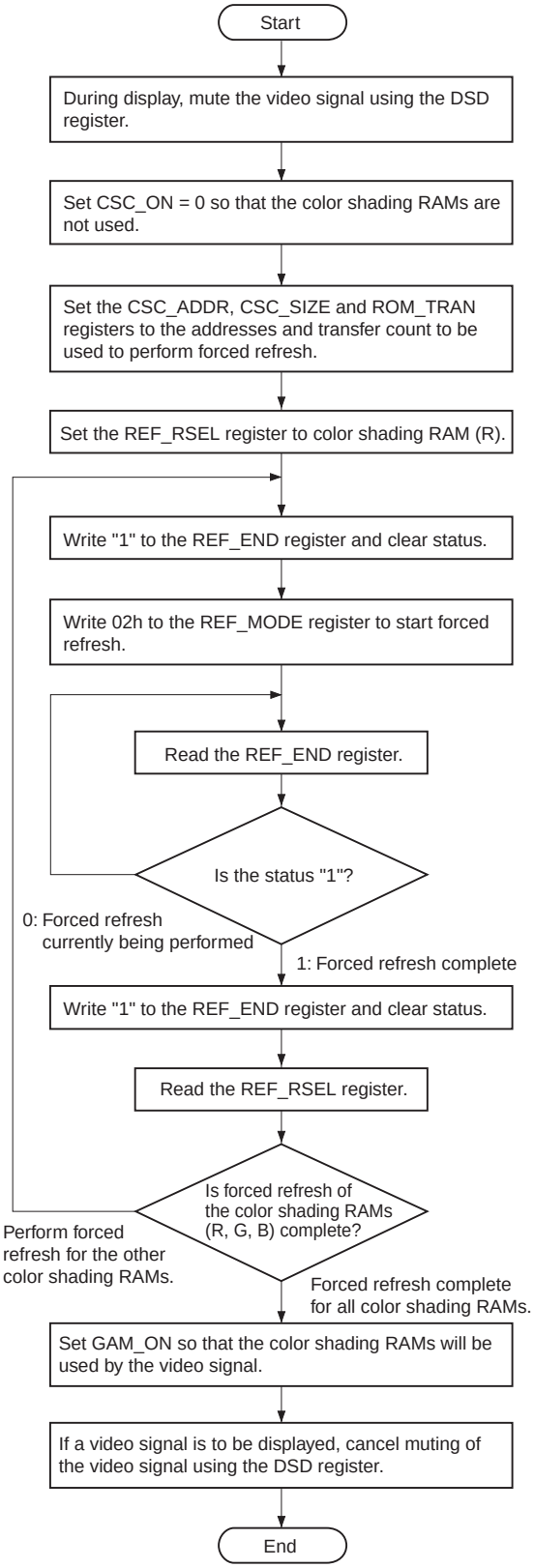
The following procedure is the procedure for setting gamma correction and color shading correction data from an external EEPROM for forced refresh when power is turned on.



(5) Procedure for forced refresh during normal operations

The following procedure is the procedure for selecting either gamma correction or color shading correction data during normal operations.

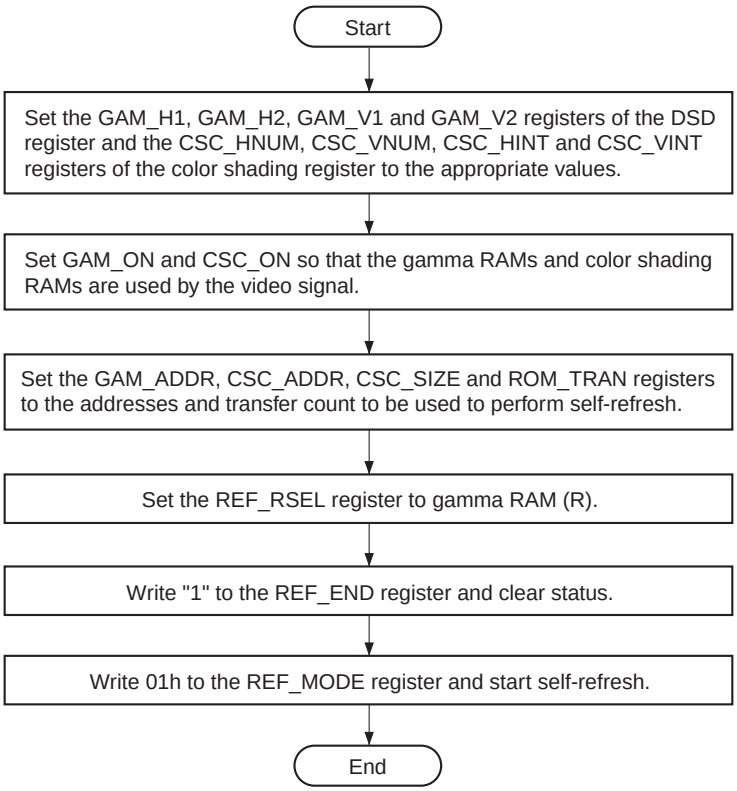




(6) Procedure for self-refresh during normal operations

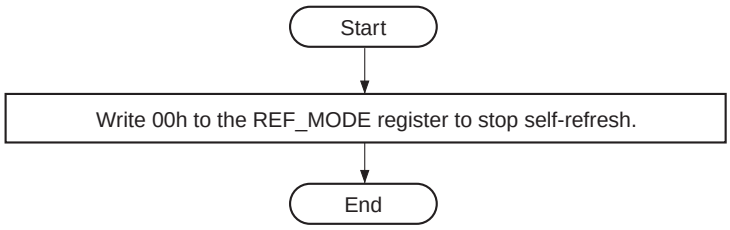
• Starting the refresh operation

The following procedure is the procedure used to set cyclic refreshing of the gamma correction and color shading correction data stored in the built-in RAM during normal operations.



• Stopping the refresh operation

The following procedure is the procedure used to stop the self-refresh operation.



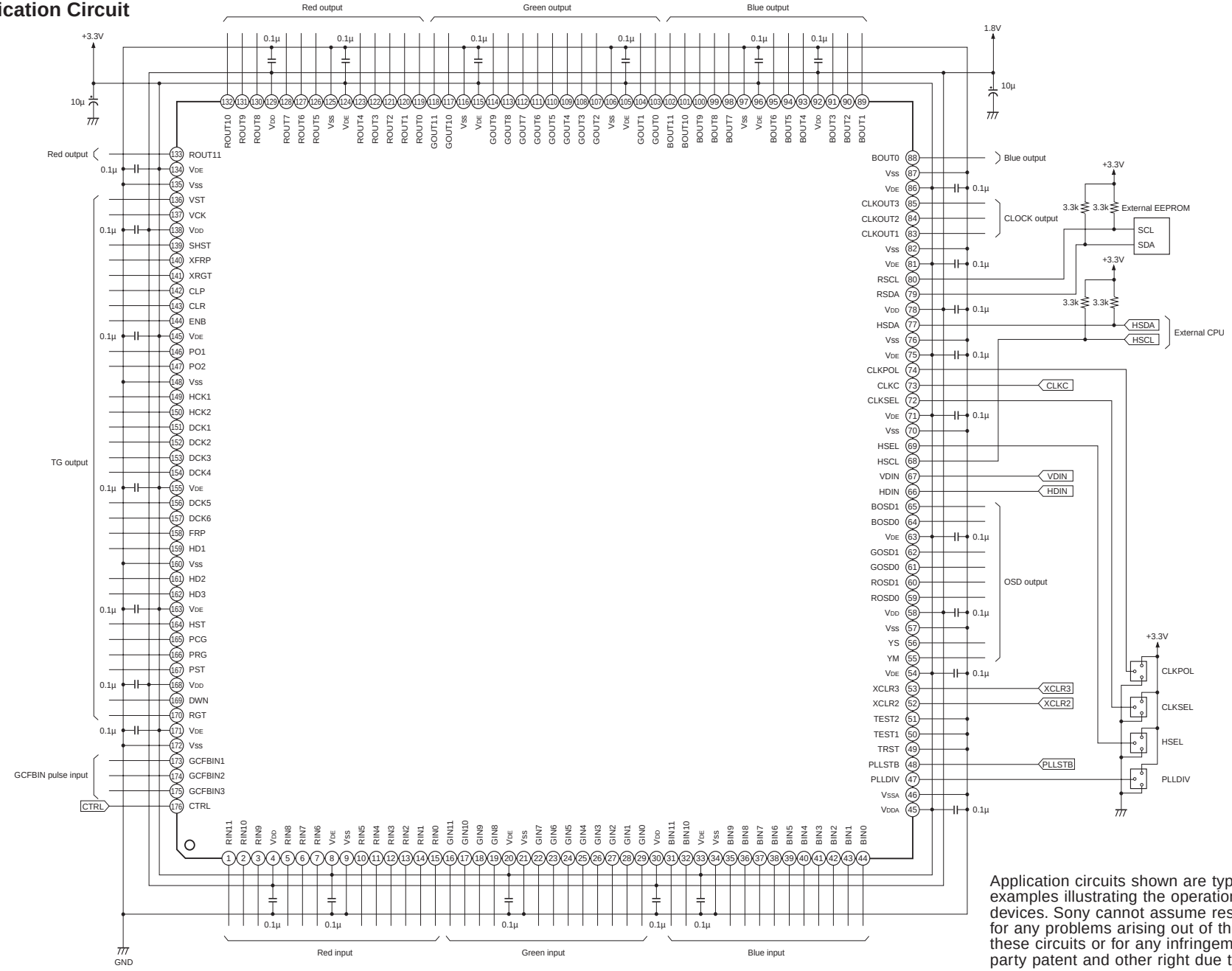
Notes on Handling

- The power supply and GND patterns have a large effect on undesired radiation on the substrate and interference to analog circuits, etc.

General precautions are as follows.

- Make the GND pattern as wide as possible. Using a multi-layer substrate and a solid ground is recommended.
- Connect each power supply pin to GND via a ceramic chip capacitor of 0.1µF or more located as close to each pin as possible.
- Do not use this IC under conditions other than the recommended operating conditions.
- Absolute maximum rating values should not be exceeded even momentarily. Exceeding that ratings may damage the device, leading to eventual breakdown.
- This IC has a MOS structure which is easily damaged by static electricity, so thorough measures should be taken to prevent electrostatic discharge.
- Since this IC utilizes a MOS structure, it may latch up due to excessive noise or power surge greater than the maximum rating of the I/O pins, interface with two power supplies of another circuit, or the order in which power is supplied to circuits. Make a thorough study of measures against the possibility of latch up before use.
- When the initialization of this IC is performed at power-on, system clear cancellation is performed after the supply voltage is set in the range of the recommended operating conditions and stabilized. Keep in mind that the internal circuit may not be initialized correctly if system clear cancellation is performed before the supply voltage is set in the range of the recommended operating conditions.
- When designing the substrate, take sufficient care for the surrounding temperature and heat radiation, and make sure the IC junction temperature does not exceed the maximum value.
- Be sure to make the number of dot clocks input to the CXD3531R in 1H an even number. Note that if there is an odd number of dot clocks, the internal phase compensation PLL will not operate properly.
- Be sure to make a thorough evaluation of any items not listed in this data sheet.

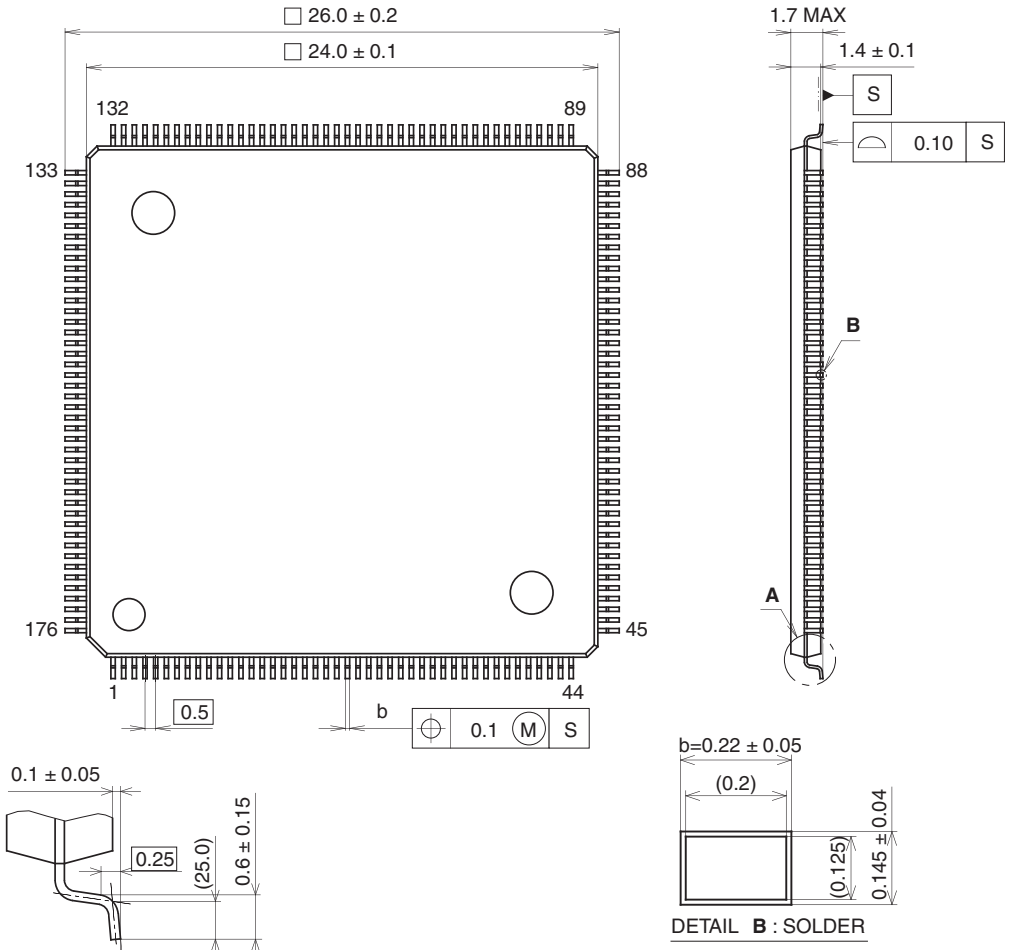
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

176PIN LQFP (PLASTIC)



SONY CODE	LQFP-176P-L01
EIAJ CODE	P-LQFP176-24x24-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.8g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm