

TOPAZ
SEMICONDUCTOR

**VNO104, VNO106
VNO109**

T-29-25.

**N-CHANNEL ENHANCEMENT-MODE
D-MOS POWER FETs**

ORDERING INFORMATION

TO-226AA (TO-92) Plastic Package	VN0104N3	VN0106N3	VN0109N3
Sorted Chips in Waffle Pack	VN0104ND	VN0106ND	VN0109ND
Description	40V, 3.0 ohm	60V, 3.0 ohm	90V, 3.0 ohm

FEATURES

- Gate Standoff Voltage, $\pm 40V$ min
- Low Output and Transfer Capacitances
- Extended Safe Operating Area
- Complementary P-Channel Devices Available

APPLICATIONS

- Complementary Voltage and Current Drivers
- Line Drivers
- Pulse Amplifiers
- Solid-State Relays

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ C$ unless otherwise specified)

Drain-Source Voltage
 VN0104 +40V
 VN0106 +60V
 VN0109 +90V

Drain-Gate Voltage ($V_{GS} = 0$)
 VN0104 +40V
 VN0106 +60V
 VN0109 +90V

Gate-Source Voltage $\pm 40V$

Continuous Drain Current
 $T_A = +25^\circ C$ $T_C = +25^\circ C$
 TO-92(N3)pkg. .23A .42A

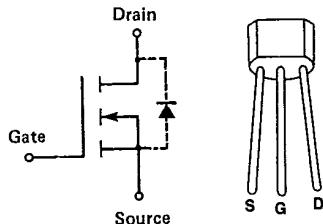
Peak Pulsed Drain Current +2.0A

Continuous Device Dissipation
 $T_A = +25^\circ C$ $T_C = +25^\circ C$
 TO-92(N3)pkg. 0.30W 1.0W

Linear Derating Factor
 $T_A = +25^\circ C$ $T_C = +25^\circ C$
 TO-92(N3)pkg. 3.0mW/ $^\circ C$ 10mW/ $^\circ C$

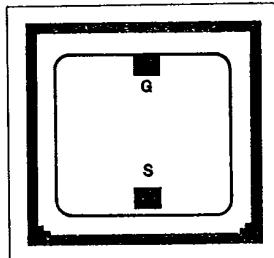
Operating Junction and Storage Temperature
 Range -55 $^\circ C$ to +150 $^\circ C$
 Lead Temperature (1/16" from mounting surface
 for 30 sec.) +260 $^\circ C$

PIN CONFIGURATION



**PACKAGE DIMENSIONS
(TO-92) TO-226A**
(See Package 5)

CHIP CONFIGURATION



Dimensions: .054 x .051 x .020 in.
 Drain is backside contact.

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VNO109****ELECTRICAL CHARACTERISTICS** ($T_A = +25^\circ\text{C}$ unless otherwise specified)**T-29-25**

#	PARAMETER	VN0104			VN0106			VN0109			UNIT	TEST CONDITIONS
		MIN	Typ	MAX	MIN	Typ	MAX	MIN	Typ	MAX		
1	BV_{DSS} Drain-Source Breakdown Voltage	40	60	;	60	90		90	105		V	$I_D = 1.0\text{mA}, V_{GS} = 0$
2				100								
3					100							
4								100				
5	Drain-Source Off Leakage Current	.01	1.0								μA	$V_{DS} = 32\text{V}$, $T_A = +125^\circ\text{C}$
6												$V_{DS} = 48\text{V}$
7	I_{DSS}											$V_{DS} = 72\text{V}$
8												$V_{DS} = 40\text{V}$
9	Gate-Body Leakage Current	± 1.0			± 1.0			± 1.0			μA	$V_{GB} = \pm 40\text{V}$, $V_{DS} = 0$
10	$V_{GS(\text{th})}$ Gate-Source Threshold Voltage	0.8	2.4	0.8		2.4	0.8		2.4		V	$V_{GS} = V_{DS}, I_D = 1.0\text{mA}$
11	$r_{DS(on)}$ Drain-Source On Resistance		5.0			5.0		5.0			ohms	$V_{GS} = 5\text{V}, I_D = .25\text{A}$
12			3.0			3.0		3.0				$V_{GS} = 10\text{V}, I_D = 1.0\text{A}$
13	$I_{D(on)}$ On Drain Current	.75		.75		.75					A	$V_{GS} = 5\text{V}$, $V_{DS} = 25\text{V}$
14		2.0		2.0		2.0						$f = 1\text{KHz}$
15	g_{fs} Common-Source Forward Transcond.	300		300		300					mmhos	$V_{DS} = 25\text{V}, I_D = 0.5\text{A}$
16	V_{SD} Source-Drain Forward Voltage		1.8			1.8		1.8			V	$I_{SD} = 1.0\text{A}, V_{GS} = 0$
17	C_{iss} Common-Source Input Capacitance		60			60		60				
18	C_{oss} Common-Source Output Capacitance		11	25		11	25		11	25	pF	$V_{DS} = 25\text{V}$, $V_{GS} = 0$, $f = 1\text{MHz}$
19	C_{rss} Common-Source Reverse Transfer Capacitance		1.5	5.0		1.5	5.0		1.5	5.0		
20	t_{on} Turn ON Time		8.0	13		8.0	13		8.0	13	nS	$V_{DD} = 25\text{V}, V_{G(\text{on})} = 10\text{V}$
21	t_{off} Turn OFF Time		8.0	17		8.0	17		8.0	17		$R_G = 51\Omega, R_L = 25\Omega$

NOTE 1: Pulse Test, 80 μSec , 1% Duty Cycle