Electrical Specifications

DSP56002 (5.0 Volt Operation)

DSP56L002 (3.3 Volt Operation – Lower Power Consumption)

The DSP56002 is fabricated in high density CMOS with TTL compatible inputs and outputs.

Table 5 Absolute Maximum Ratings (GND = 0 Vdc)

Rating	Symbol	Value		Unit
		DSP56002	DSP56L002	
Supply Voltage	V_{CC}	-0.3 to +7.0	-0.3 to +4.0	V
All Input Voltages	V_{IN}	GND - 0.5 to V_{CC} + 0.5	GND - 0.5 to V_{CC} + 0.5	V
Current Drain per Pin Excluding V_{CC} and GND	I	10	10	mA
Operating Temperature Range	T_J	-40 to +105	0 to +80	°C
Storage Temperature	T_{stg}	-55 to +150	-55 to +150	°C

Table 6 Thermal Characteristics of Packages

Thermal Resistance	PQFP			PGA			TQFP		
	Symbol	Value	Units	Symbol	Value	Units	Symbol	Value	Units
Junction to Ambient	Θ_{JA}	38	°C/W	Θ_{JA}	22	°C/W	Θ_{JA}	49	°C/W
Junction to Case (estimated)	Θ_{JC}	13	°C/W	Θ_{JC}	6.5	°C/W	Θ_{JC}	12	°C/W

Note: See discussion under "Design Considerations, Heat Dissipation," page 86.

DSP56002
DC Electrical Characteristics

(V_{CC} = 5.0 Vdc ± 10%; T_J = -40° to +105° C)

Table 7 DC Electrical Characteristics for the DSP56002

Characteristics	Symbol	DSP56002			Units
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage • Except EXTAL, $\overline{\text{RESET}}$, MODA, MODB, MODC • EXTAL • $\overline{\text{RESET}}$ • MODA, MODB, MODC	 V_{IH} V_{IHC} V_{IHR} V_{IHM}	 2.0 4.0 2.5 3.5	 — — — —	 V_{CC} V_{CC} V_{CC} V_{CC}	 V V V V
Input Low Voltage • Except EXTAL, MODA, MODB, MODC • EXTAL • MODA, MODB, MODC	 V_{IL} V_{ILC} V_{ILM}	 -0.5 -0.5 -0.5	 — — —	 0.8 0.6 2.0	 V V V
Input Leakage Current EXTAL, $\overline{\text{RESET}}$, MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, MODC/$\overline{\text{NMI}}$, $\overline{\text{BR}}$, $\overline{\text{WT}}$	I_{IN}	-1	—	1	µA
Three-State (Off-State) Input Current (@ 2.4 V / 0.4 V)	I_{TSI}	-10	—	10	µA
Output High Voltage (I_{OH} = -0.4 mA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 3.0 mA; $\overline{\text{HREQ}}$ I_{OL} = 6.7 mA, TXD I_{OL} = 6.7 mA)	V_{OL}	—	—	0.4	V
Internal Supply Current at 40 MHz (See Note 3) • in Wait Mode (See Note 1) • in Stop Mode (See Note 1)	I_{CCI} I_{CCW} I_{CCS}	— — —	90 12 2	105 20 95	mA mA µA
Internal Supply Current at 66 MHz (See Note 3) • in Wait Mode (See Note 1) • in Stop Mode (See Note 1)	I_{CCI} I_{CCW} I_{CCS}	— — —	95 15 2	130 25 95	mA mA µA
PLL Supply Current (See Note 4) at 40 MHz at 66 MHz		— —	1 1.1	1.5 1.5	mA mA
CKOUT Supply Current (See Note 5)at 40 MHz at 66 MHz		— —	14 28	20 35	mA mA
Input Capacitance (See Note 2)	C_{IN}	—	10	—	pF

NOTES:

1. In order to obtain these results all inputs must be terminated (i.e., not allowed to float) using CMOS levels.
2. Periodically sampled and not 100% tested.
3. **Power Consumption** in the **Design Considerations** section describes how to calculate the external supply current.
4. Values given are for PLL enabled.
5. Values given are for CKOUT enabled.

DSP56L002
DC Electrical Characteristics

(V_{CC} = 3.3 Vdc ± 0.3 V; T_J = 0° to +80° C)

Table 8 DC Electrical Characteristics for the DSP56L002

Characteristics	Symbol	DSP56L002			Units
		Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Input High Voltage • Except EXTAL • EXTAL	 V_{IH} V_{IHC}	 2.0 2.7	 — —	 V_{CC} V_{CC}	 V V
Input Low Voltage • Except EXTAL • EXTAL	 V_{IL} V_{ILC}	 -0.5 -0.5	 — —	 0.8 0.4	 V V
Input Leakage Current EXTAL, $\overline{\text{RESET}}$, MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, MODC/$\overline{\text{NMI}}$, $\overline{\text{BR}}$, $\overline{\text{WT}}$	I_{IN}	-1	—	1	µA
Three-State (Off-State) Input Current (@ 2.4 V / 0.4 V)	I_{TSI}	-10	—	10	µA
Output High Voltage (I_{OH} = -0.4 mA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 3.0 mA; $\overline{\text{HREQ}}$ I_{OL} = 6.7 mA, TXD I_{OL} = 6.7 mA, $\overline{\text{WR}}$, $\overline{\text{RD}}$ I_{OL}=2.0 mA)	V_{OL}	—	—	0.4	V
Internal Supply Current at 40 MHz (See Note 3) • in Wait Mode (See Note 1) • in Stop Mode (See Note 1)	I_{CCI} I_{CCW} I_{CCS}	— — —	50 10 1	65 14 50	mA mA µA
PLL Supply Current (See Note 4)		—	0.7	1.1	mA
CKOUT Supply Current (See Note 5)		—	10	14	mA
Input Capacitance (See Note 2)	C_{IN}	—	10	—	pF

NOTES:

1. In order to obtain these results all inputs must be terminated (i.e., not allowed to float) using CMOS levels.
2. Periodically sampled and not 100% tested.
3. **Power Consumption** in the **Design Considerations** section describes how to calculate the external supply current.
4. Values given are for PLL enabled.
5. Values given are for CKOUT enabled.

AC Electrical Characteristics

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, $\overline{\text{RESET}}$, MODA, MODB, and MODC. These four pins are tested using the input levels set forth in the DC Electrical Characteristics section. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002/L002 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V respectively.

Internal Clocks

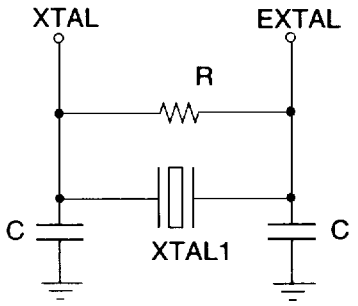
For each occurrence of T_H, T_L, T_C or I_{CYC} substitute with the expressions given in Table 9. ET_H, ET_L, and ET_C are further defined in Table 10. DF and MF are PLL division and multiplication factors set in registers.

Table 9 Internal Clocks

Characteristics	Symbol	Expression
Internal Operation Frequency	f	
Internal Clock High Period - with PLL disabled	T_H	ET_H
- with PLL enabled and MF ≤ 4		(Min) 0.48 x ET_C x DF/MF (Max) 0.52 x ET_C x DF/MF
- with PLL enabled and MF > 4		(Min) 0.467 x ET_C x DF/MF (Max) 0.533 x ET_C x DF/MF
Internal Clock Low Period - with PLL disabled	T_L	ET_L
- with PLL enabled and MF ≤ 4		(Min) 0.48 x ET_C x DF/MF (Max) 0.52 x ET_C x DF/MF
- with PLL enabled and MF > 4		(Min) 0.467 x ET_C x DF/MF (Max) 0.533 x ET_C x DF/MF
Internal Clock Cycle Time	T_C	ET_C x DF/MF
Instruction Cycle Time	I_{CYC}	2 x T_C

Clock

The DSP56002/L002 system clock may be derived from the on-chip crystal oscillator as shown in Figure 3, or it may be externally supplied. An externally supplied square wave voltage source should be connected to EXTAL, leaving XTAL physically unconnected (see Figure 4) to the board or socket. The rise and fall time of this external clock should be 4 ns maximum.



Fundamental Frequency Crystal Oscillator

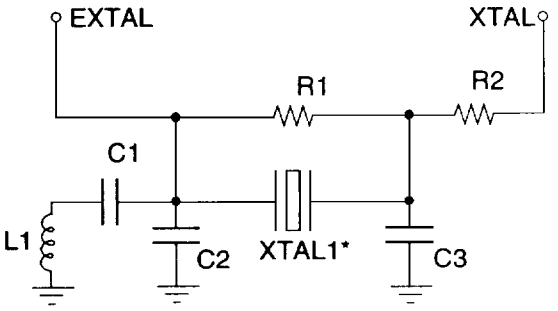
Suggested Component Values

R = 680 KΩ ± 10%

C = 20 pf ± 20%

NOTES:

1. The suggested crystal source is ICM, # 433163 - 4.00 (4 MHz fundamental, 20 pf load) or # 436163 - 30.00 (30 MHz fundamental, 20 pf load).
2. To reduce system cost, a ceramic resonator may be used instead of the crystal. Suggested source: Murata-Erie #CST4.00MGW040



3rd Overtone Crystal Oscillator

Suggested Component Values

R1 = 470 KΩ ± 10%

R2 = 330 Ω ± 10%

C1 = 0.1 µf ± 20%

C2 = 26 pf ± 20%

C3 = 20 pf ± 10%

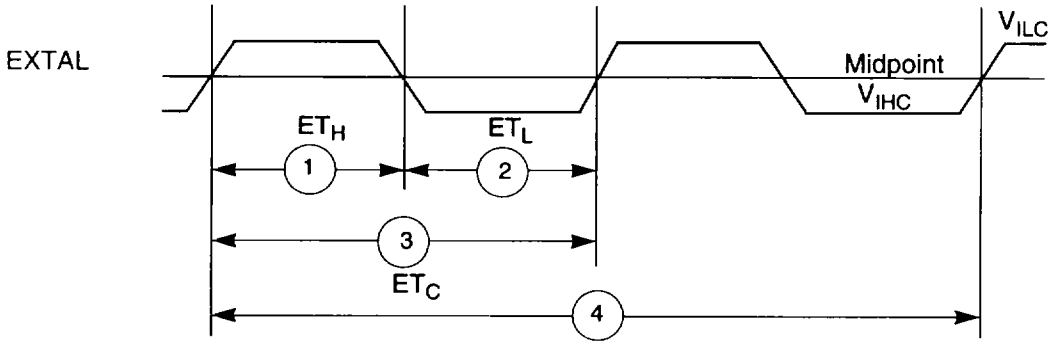
L1 = 2.37 µH ± 10%

XTAL = 40 MHz, AT cut, 20 pf load, 50 Ω max series resistance

NOTES:

1. *3rd overtone crystal.
2. The suggested crystal source is ICM, # 471163 - 40.00 (40 MHz 3rd overtone, 20 pf load).
3. R2 limits crystal current.
4. Reference Benjamin Parzen, The Design of Crystal and Other Harmonic Oscillators, John Wiley & Sons, 1983.

Figure 3 Crystal Oscillator Circuits



NOTE: The midpoint is $V_{ILC} + 0.5 (V_{IHC} - V_{ILC})$.

Figure 4 External Clock Timing

Table 10 Clock Operation

Num	Characteristics	Symbol	40 MHz		66 MHz		Unit
			Min	Max	Min	Max	
	Frequency of Operation (EXTAL Pin)	E_f	0	40	0	66	MHz
1	Clock Input High (See Note) • with PLL disabled (46.7% - 53.3% duty cycle) • with PLL enabled (42.5% - 57.5% duty cycle)	ET_H	11.7 10.5	∞ 235.5 µs	7.09 6.36	∞ 235.5 µs	ns
2	Clock Input Low (See Note) • with PLL disabled (46.7% - 53.3% duty cycle) • with PLL enabled (42.5% - 57.5% duty cycle)	ET_L	11.7 10.5	∞ 235.5 µs	7.09 6.36	∞ 235.5 µs	ns
3	Clock Cycle Time • with PLL disabled • with PLL enabled	ET_C	25 25	∞ 409.6 µs	15.15 15.15	∞ 409.6 µs	ns
4	Instruction Cycle Time = $I_{CYC} = 2 \times T_C$ (See Note) • with PLL disabled • with PLL enabled	I_{CYC}	50 50	∞ 819.2 µs	30.3 30.3	∞ 819.2 µs	ns

NOTE: External Clock Input High and External Clock Input Low are measured at 50% of the input transition.

Phase-Locked Loop (PLL)

Table 11 Phase-Locked Loop Characteristics

Characteristics	Expression	Min	Max	Unit
VCO frequency when PLL enabled	MF x E_f (See Notes 1,2)	10	f (See Note 3)	MHz
PLL external capacitor (PCAP pin to V_{CCP})	MF × Cpcap (See Note 4) @ MF ≤ 4 @ MF > 4	 MF × 340 MF × 380	 MF × 480 MF × 970	pF

NOTES:

1. The "E" in ET_H, ET_L, and ET_C means external.
2. MF is the PCTL Multiplication Factor bits (MF0 - MF11).
   DF is the PCTL Division Factor bits (DF0 - DF3).
3. The maximum VCO frequency is limited to the internal operation frequency.
4. Cpcap is the value of the PLL capacitor (connected between PCAP pin and V_{CCP}) for MF=1. The recommended value for Cpcap is 400 pF for MF ≤ 4 and 540 pF for MF > 4.

Reset, Stop, Mode Select, and Interrupt Timing

DSP56002: V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105° C, C_L = 50 pF + 2 TTL Loads

DSP56L002: V_{CC} = 3.3 Vdc ± 0.3 V, T_J = 0° to +80° C, C_L = 50 pF + 2 TTL Loads

WS = Number of wait states (1 WS = T_C) programmed into external bus access using BCR (WS = 0 - 15)

Table 12 Reset, Stop, Mode Select, and Interrupt Timing

Num	Characteristics	40/66 MHz		Unit
		Min	Max	
9	Delay from $\overline{\text{RESET}}$ Assertion to Address High Impedance (periodically sampled and not 100% tested).	—	26	ns
10	Minimum Stabilization Duration • Internal Oscillator PLL Disabled (See Note 1) • External clock PLL Disabled (See Note 2) • External clock PLL Enabled (See Note 2)	 75000 × T_C 25 × T_C 2500 × T_C	 — — —	 ns ns ns
11	Delay from Asynchronous $\overline{\text{RESET}}$ Deassertion to First External Address Output (Internal Reset Deassertion)	8 × T_C	9 × T_C + 20	ns

Table continued on next page

Table 12 Reset, Stop, Mode Select, and Interrupt Timing (continued)

Num	Characteristics	40/66 MHz		Unit
		Min	Max	
12	Synchronous Reset Setup Time from $\overline{\text{RESET}}$ Deassertion to CKOUT transition #1	8.5	T_C	ns
13	Synchronous Reset Delay Time from the CKOUT transition #1 to the First External Address Output	$8 \times T_C$	$8 \times T_C + 6$	ns
14	Mode Select Setup Time	21	—	ns
15	Mode Select Hold Time	0	—	ns
16	Minimum Edge-Triggered Interrupt Request Assertion Width	13	—	ns
16a	Minimum Edge-Triggered Interrupt Request Deassertion Width	13	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{NMI}}$ Assertion to External Memory Access Address Out Valid • Caused by First Interrupt Instruction Fetch • Caused by First Interrupt Instruction Execution	 $5 \times T_C + T_H$ $9 \times T_C + T_H$	 — —	 ns ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{NMI}}$ Assertion to General Purpose Transfer Output Valid caused by First Interrupt Instruction Execution	$11 \times T_C + T_H$	—	ns
19	Delay from Address Output Valid caused by First Interrupt Instruction Execute to Interrupt Request Deassertion for Level Sensitive Fast Interrupts (See Note 3)	—	$2\ T_C + T_L + (T_C \times WS) - 23$	ns
20	Delay from $\overline{\text{RD}}$ Assertion to Interrupt Request Deassertion for Level Sensitive Fast Interrupts (See Note 3)	—	$2T_C + (T_C \times WS) - 21$	ns
21	Delay from $\overline{\text{WR}}$ Assertion to Interrupt Request Deassertion for Level Sensitive Fast Interrupts • WS = 0 • WS > 0 (See Note 3)	 — —	 $2 \times T_C - 21$ $T_C + T_L + (T_C \times WS) - 21$	 ns ns
22	Delay from General-Purpose Output Valid to Interrupt Request Deassertion for Level Sensitive Fast Interrupts - If Second Interrupt Instruction is: • Single Cycle • Two Cycles (See Note 3)	 — —	 $T_L - 31$ $(2 \times T_C) + T_L - 31$	 ns ns
23	Synchronous Interrupt Setup Time from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{NMI}}$ Assertion to the CKOUT transition #2	10	T_C	ns
24	Synchronous Interrupt Delay Time from the CKOUT transition #2 to the First External Address Output Valid caused by the First Instruction Fetch after coming out of Wait State	$13 \times T_C + T_H$	$13 \times T_C + T_H + 6$	ns

Table 12 Reset, Stop, Mode Select, and Interrupt Timing (continued)

Num	Characteristics	40/66 MHz		Unit
		Min	Max	
25	Duration for $\overline{\text{IRQA}}$ Assertion to Recover from Stop State	12	—	ns
26	Delay from $\overline{\text{IRQA}}$ Assertion to Fetch of First Interrupt Instruction (when exiting 'Stop') • Internal Crystal Oscillator Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 • Stable External Clock, PCTL bit 17 = 1 (See Note 1)	 $65548 \times T_C$ $20 \times T_C$ $13 \times T_C$	 — — —	 ns ns ns
27	Duration of Level Sensitive $\overline{\text{IRQA}}$ Assertion to ensure interrupt service (when exiting 'Stop') • Internal Crystal Oscillator Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 • Stable External Clock, PCTL bit 17 = 1 (See Note 1)	 $65534 \times T_C + T_L$ $6 \times T_C + T_L$ 12	 — — —	 ns ns ns
28	Delay from Level Sensitive $\overline{\text{IRQA}}$ Assertion to Fetch of First Interrupt Instruction (when exiting 'Stop') • Internal Crystal Oscillator Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 • Stable External Clock, PCTL bit 17= 1 (See Note 1)	 $65548 \times T_C$ $20 \times T_C$ $13 \times T_C$	 — — —	 ns ns ns

NOTES:

1. A clock stabilization delay is required when using the on-chip crystal oscillator in two cases:
   - after power-on reset, and
   - when recovering from Stop mode.

   During this stabilization period, T_C, T_H, and T_L will not be constant. Since this stabilization period varies, a delay of $75{,}000 \times T_C$ is typically allowed to assure that the oscillator is stable before executing programs.

2. Circuit stabilization delay is required during reset when using an external clock in two cases:
   - after power-on reset, and
   - when recovering from Stop mode.

3. When using fast interrupts and $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ are defined as level-sensitive, then timings 19 through 22 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deassertive edge-triggered mode is recommended when using fast interrupt. Long interrupts are recommended when using level-sensitive mode.

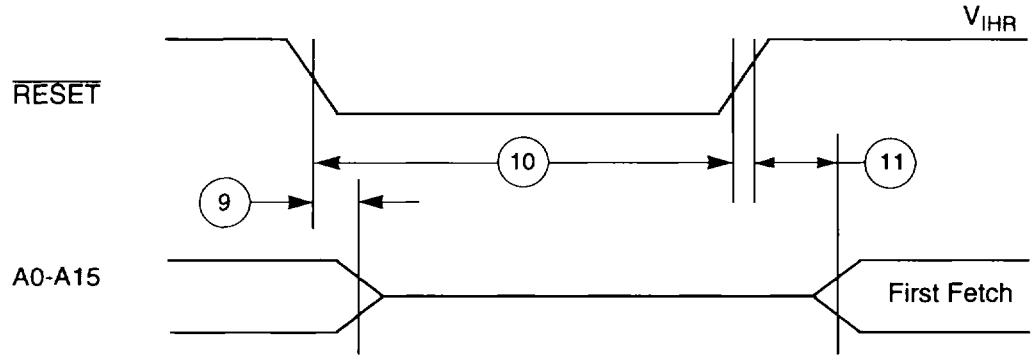


Figure 5 Reset Timing

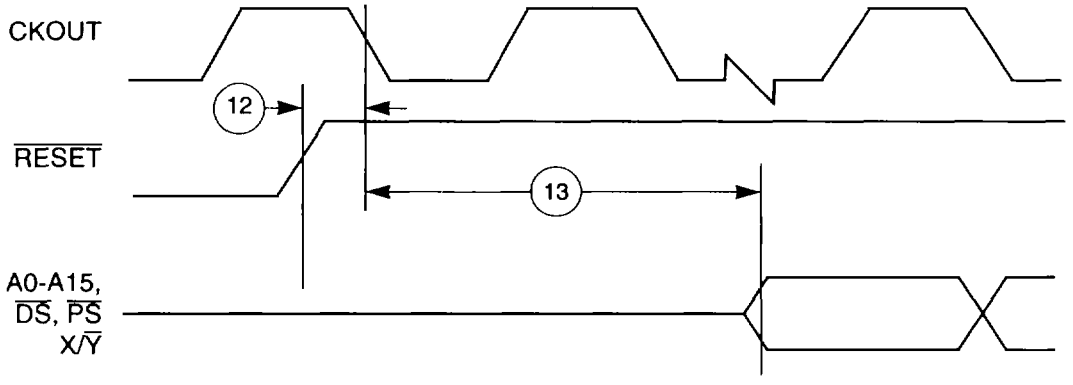


Figure 6 Synchronous Reset Timing

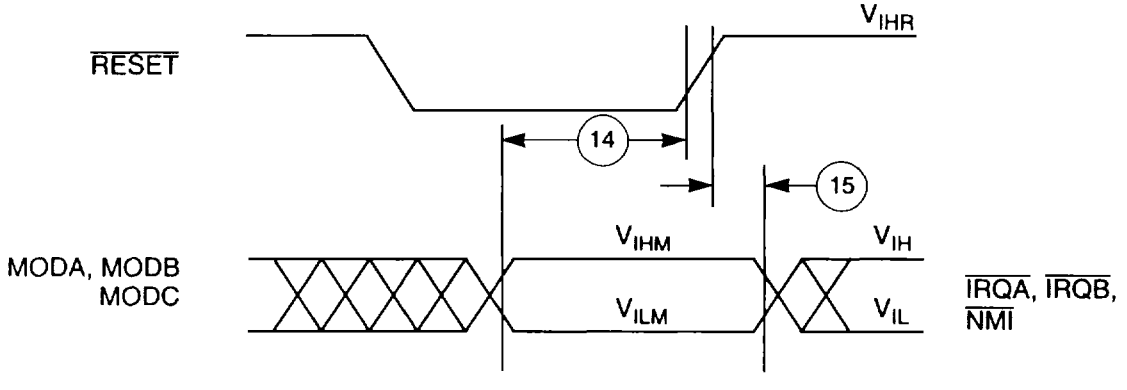
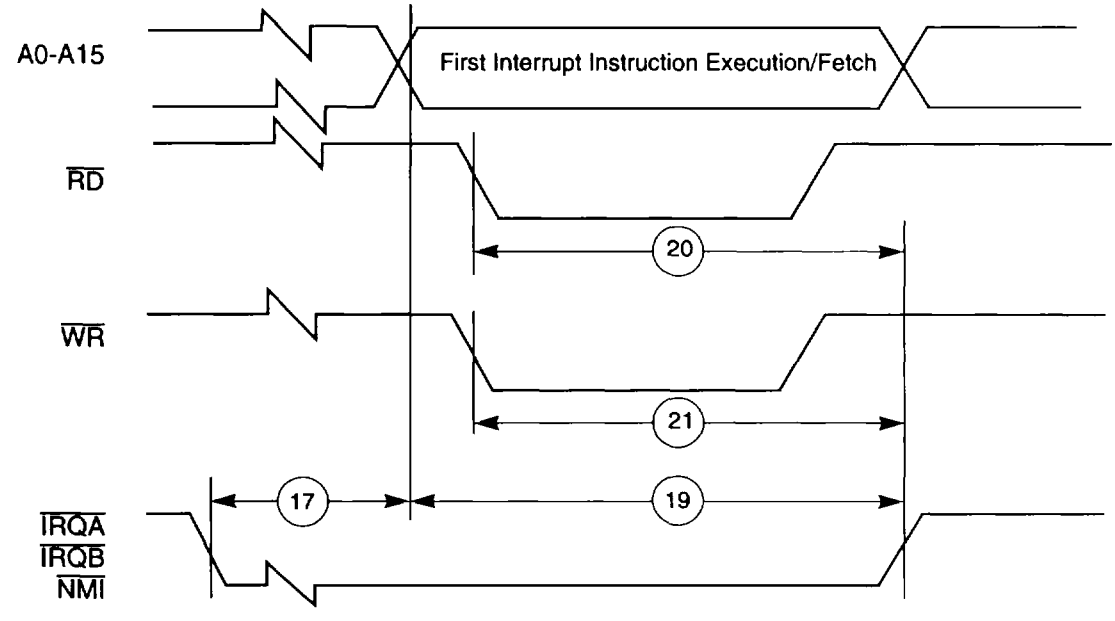
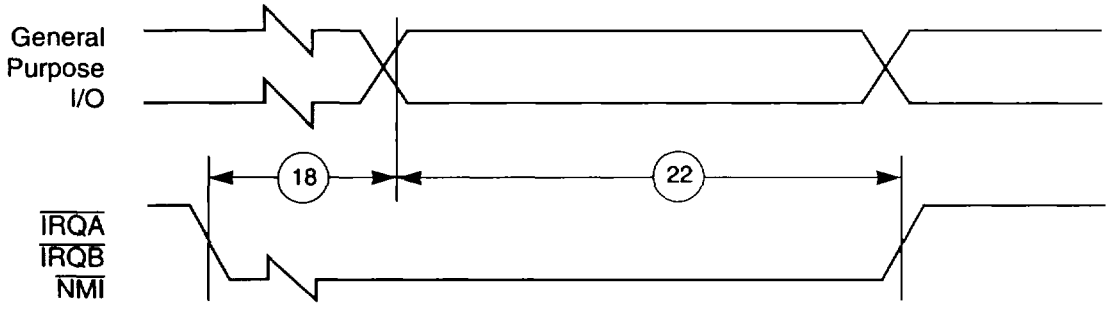


Figure 7 Operating Mode Select Timing



a) First Interrupt Instruction Execution



b) General Purpose I/O

Figure 8 External Level-Sensitive Fast Interrupt Timing

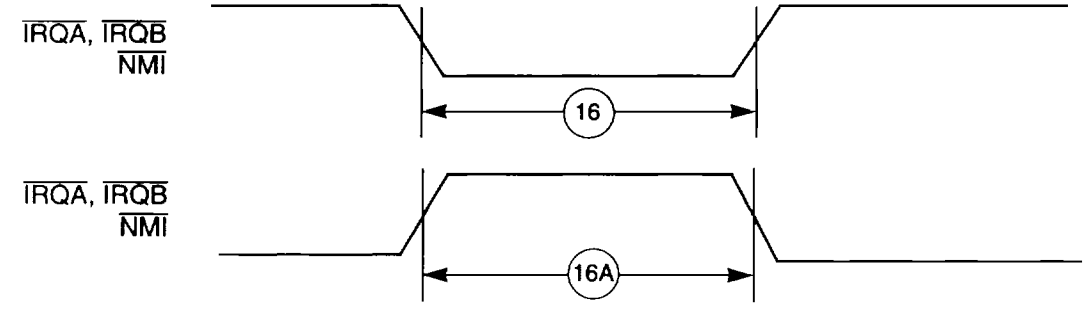


Figure 9 External Interrupt Timing (Negative Edge-Triggered)

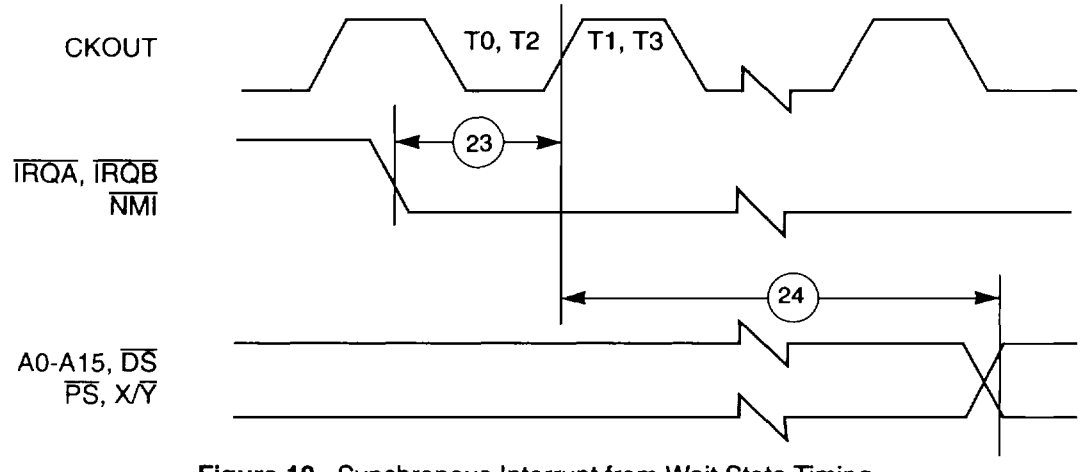


Figure 10 Synchronous Interrupt from Wait State Timing

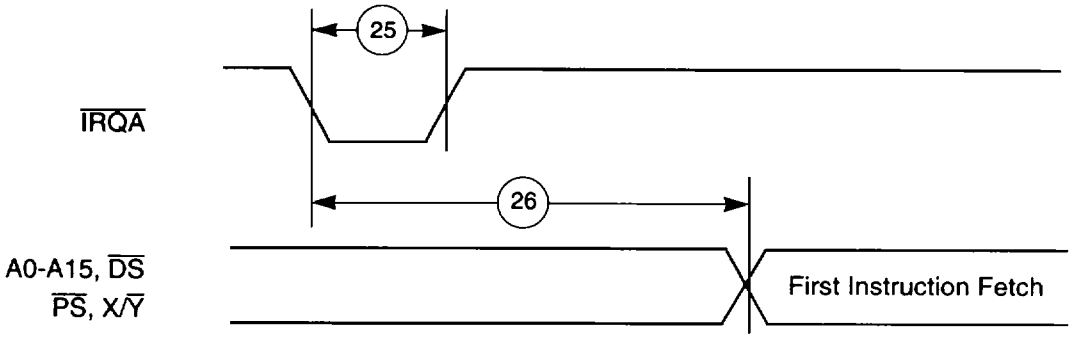


Figure 11 Recovery from Stop State Using IRQA

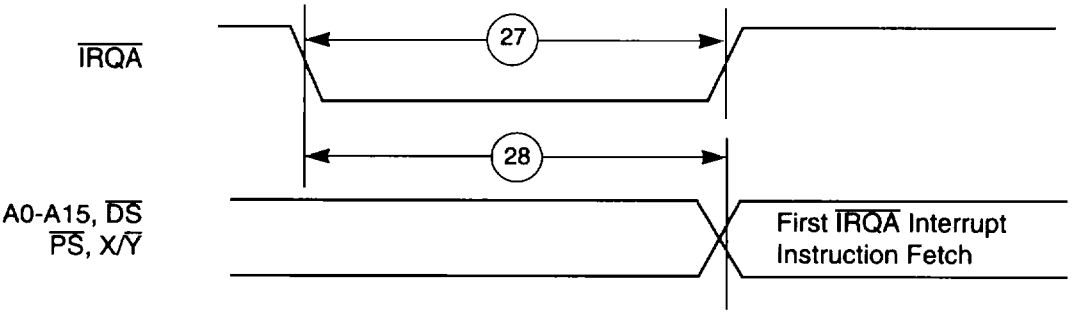


Figure 12 Recovery from Stop State Using IRQA Interrupt Service

Host I/O Timing

DSP56002: V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105° C, C_L = 50 pF + 2 TTL Loads

DSP56L002: V_{CC} = 3.3 Vdc ± 0.3 V, T_J = 0° to +80° C, C_L = 50 pF + 2 TTL Loads

Active low lines should be "pulled up" in a manner consistent with the AC and DC specifications.

Table 13 Host I/O Timing

Num	Characteristics	40/66 MHz		Unit
		Min	Max	
31	$\overline{HEN}/\overline{HACK}$ Assertion Width (See Note 1) • CVR, ICR, ISR, RXL Read • IVR, RXH/M Read • Write	 T_C + 31 26 13	 — — —	 ns
32	$\overline{HEN}/\overline{HACK}$ Deassertion Width (See Note 1) • Between Two TXL Writes (See Note 2) • Between Two CVR, ICR, ISR, RXL Reads (See Note 3)	13 2 × T_C + 31 2 × T_C + 31	— — —	ns ns ns
33	Host Data Input Setup Time Before $\overline{HEN}/\overline{HACK}$ Deassertion	4	—	ns
34	Host Data Input Hold Time After $\overline{HEN}/\overline{HACK}$ Deassertion	3	—	ns
35	$\overline{HEN}/\overline{HACK}$ Assertion to Output Data Active from High Impedance	0	—	ns
36	$\overline{HEN}/\overline{HACK}$ Assertion to Output Data Valid	—	26	ns
37	$\overline{HEN}/\overline{HACK}$ Deassertion to Output Data High Impedance (See Note 5)	—	18	ns
38	Output Data Hold Time After $\overline{HEN}/\overline{HACK}$ Deassertion (See Note 6)	2.5	—	ns
39	HR/$\overline{W}$ Low Setup Time Before $\overline{HEN}$ Assertion	0	—	ns
40	HR/$\overline{W}$ Low Hold Time After $\overline{HEN}$ Deassertion	3	—	ns
41	HR/$\overline{W}$ High Setup Time to $\overline{HEN}$ Assertion	0	—	ns
42	HR/$\overline{W}$ High Hold Time After $\overline{HEN}/\overline{HACK}$ Deassertion	3	—	ns
43	HA0-HA2 Setup Time Before $\overline{HEN}$ Assertion	0	—	ns
44	HA0-HA2 Hold Time After $\overline{HEN}$ Deassertion	3	—	ns
45	DMA $\overline{HACK}$ Assertion to $\overline{HREQ}$ Deassertion (See Note 4)	3	45	ns

Table 13 Host I/O Timing (continued)

Num	Characteristics	40/66 MHz		Unit
		Min	Max	
46	DMA $\overline{\text{HACK}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion (See Notes 4, 5) • for DMA RXL Read • for DMA TXL Write • all other cases	 $T_L + T_C + T_H$ $T_L + T_C$ 0	 — — —	 ns ns ns
47	Delay from $\overline{\text{HEN}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion for RXL Read (See Notes 4, 5)	$T_L + T_C + T_H$	—	ns
48	Delay from $\overline{\text{HEN}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion for TXL Write (See Notes 4, 5)	$T_L + T_C$	—	ns
49	Delay from $\overline{\text{HEN}}$ Assertion to $\overline{\text{HREQ}}$ Deassertion for RXL Read, TXL Write (See Notes 4, 5)	3	58	ns

NOTES:

1. See **Host Port Considerations** in the section on **Design Considerations**.
2. This timing must be adhered to only if two consecutive writes to the TXL are executed without polling TXDE or $\overline{\text{HREQ}}$.
3. This timing must be adhered to only if two consecutive reads from one of these registers are executed without polling the corresponding status bits or $\overline{\text{HREQ}}$
4. $\overline{\text{HREQ}}$ is pulled up by a 1 kΩ resistor.
5. Specifications are periodically sampled and not 100% tested.
6. May decrease to 0 ns for future versions.

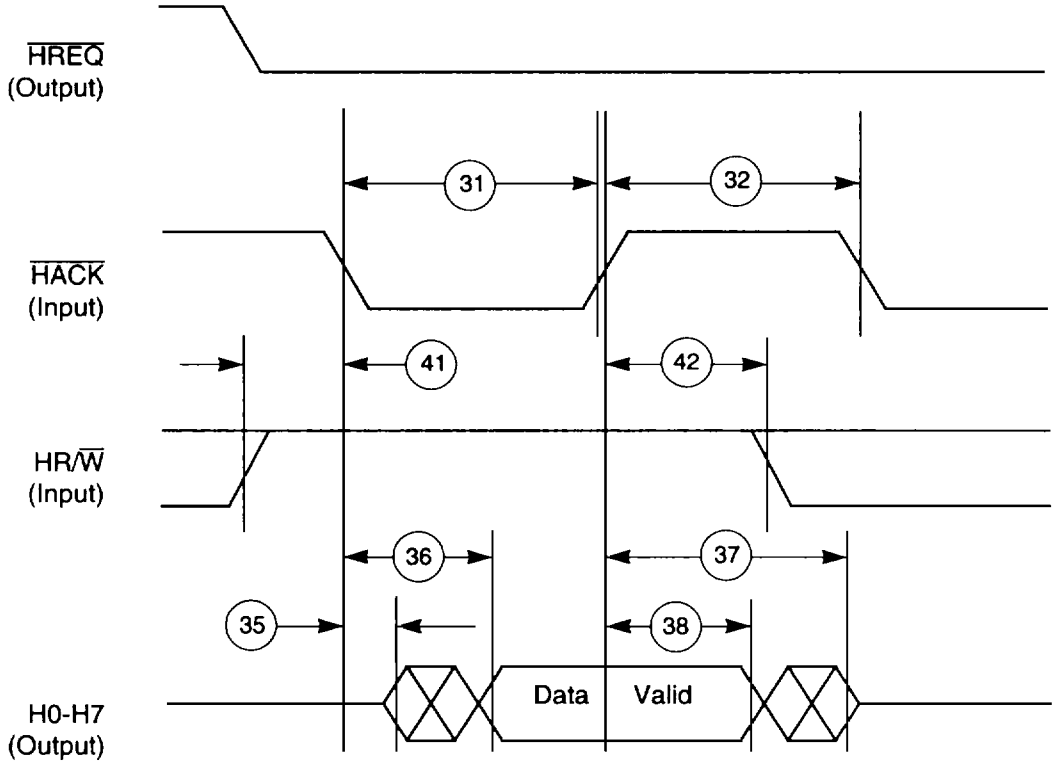


Figure 13 Host Interrupt Vector Register (IVR) Read

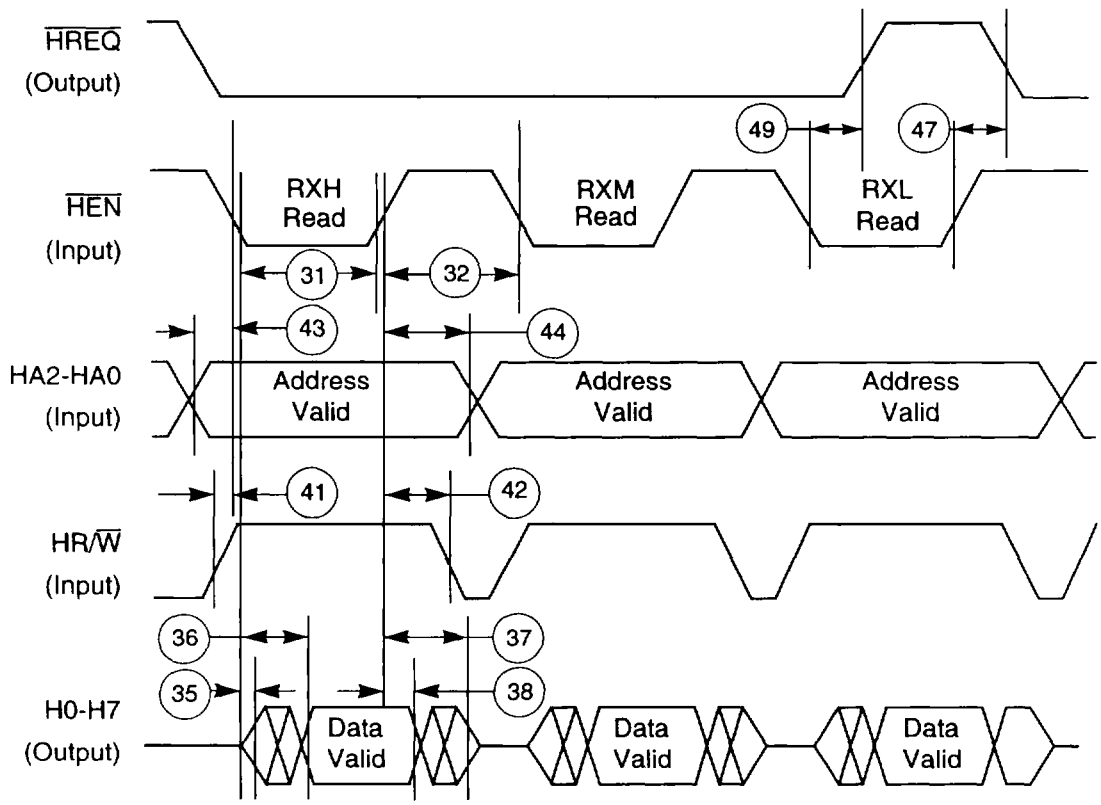


Figure 14 Host Read Cycle (Non-DMA Mode)

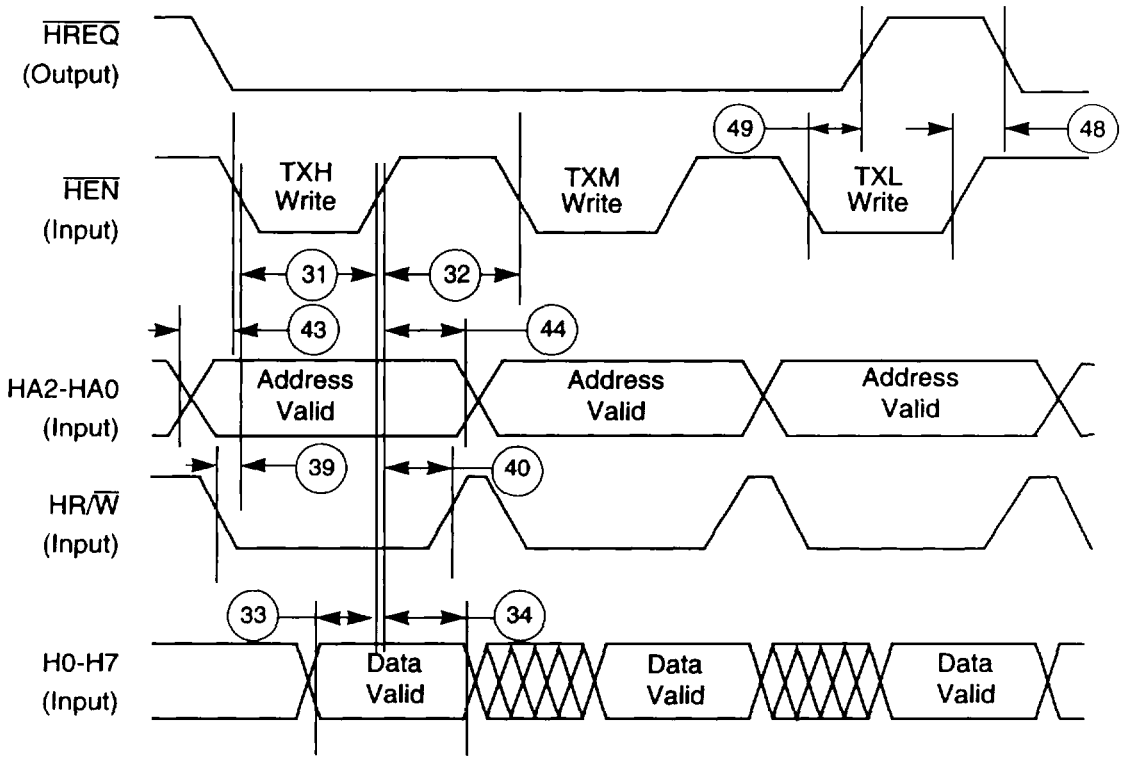


Figure 15 Host Write Cycle (Non-DMA Mode)

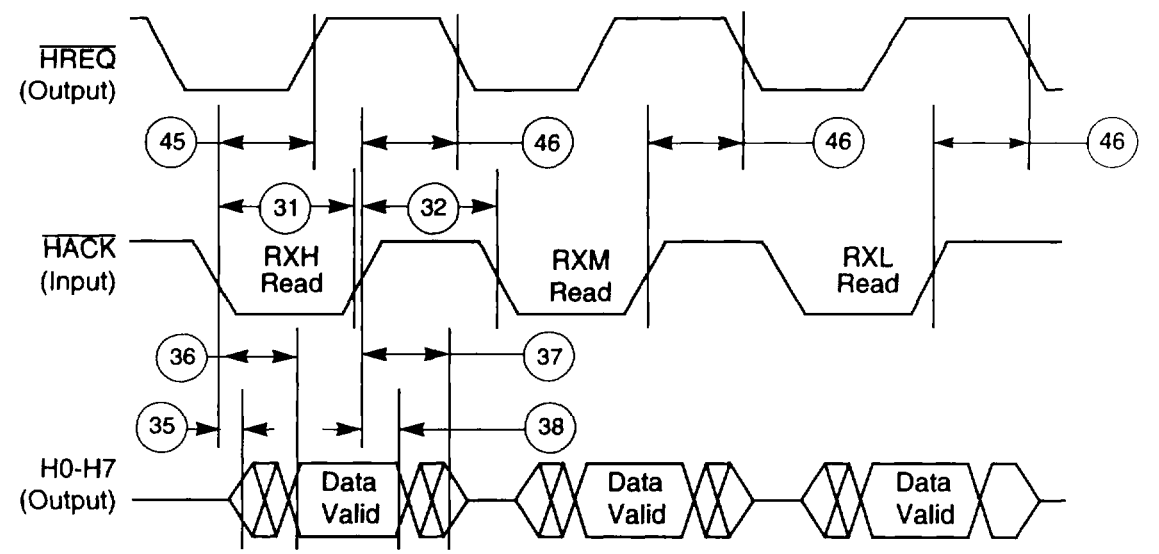


Figure 16 Host DMA Read Cycle

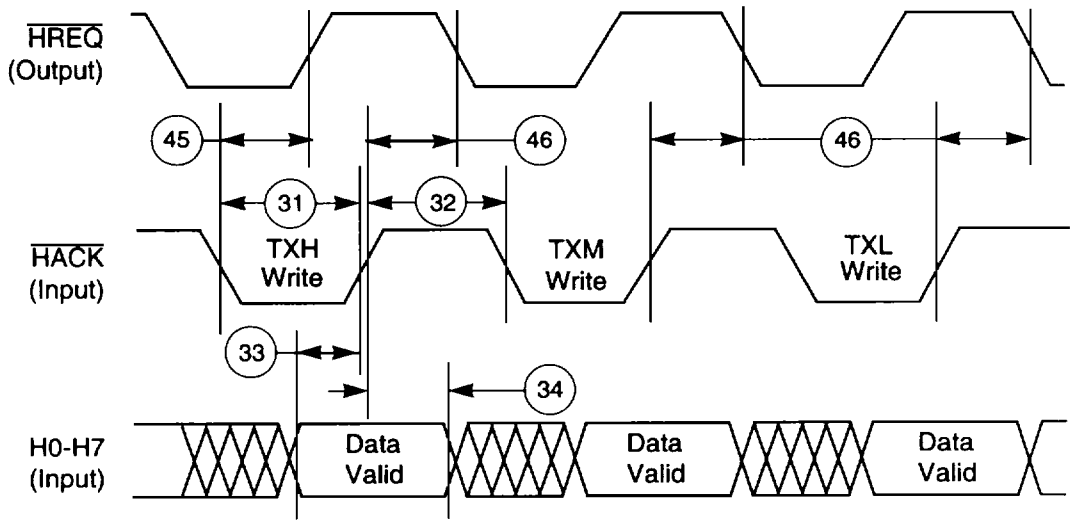


Figure 17 Host DMA Write Cycle

Serial Communication Interface (SCI) Timing

DSP56002: V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105° C, C_L = 50 pF + 2 TTL Loads

DSP56L002: V_{CC} = 3.3 Vdc ± 0.3 V, T_J = 0° to +80° C, C_L = 50 pF + 2 TTL Loads

tSCC = Synchronous Clock Cycle Time (for internal clock, tSCC is determined by the SCI clock control register and T_C). The minimum tSCC value is $8 \times T_C$.

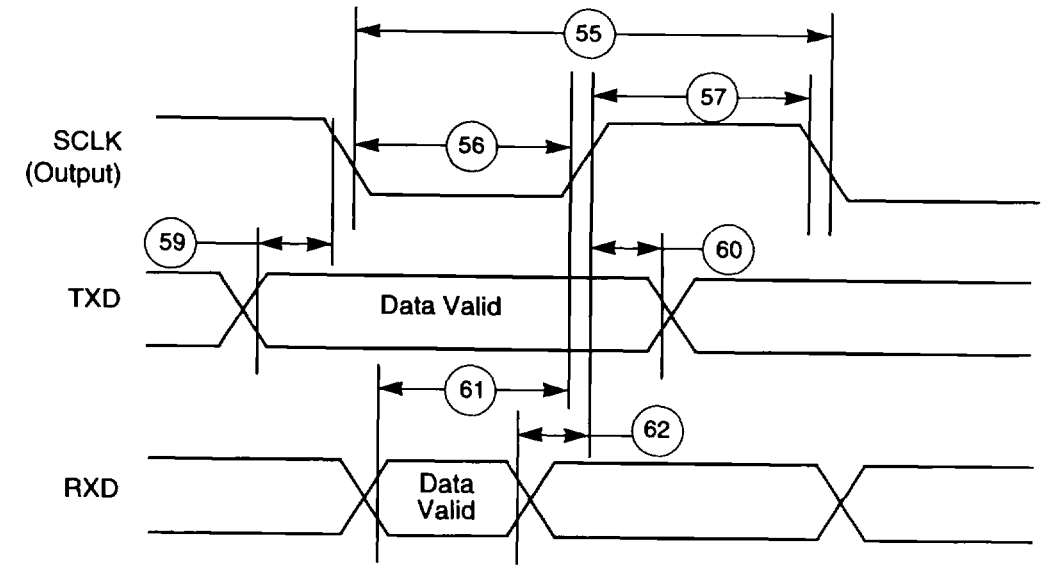
Table 14 SCI Synchronous Mode Timing

Num	Characteristics	40/66 MHz		Unit
		Min	Max	
55	Synchronous Clock Cycle — tSCC	$8 \times T_C$	—	ns
56	Clock Low Period	tSCC/2 - 10.5	—	ns
57	Clock High Period	tSCC/2 - 10.5	—	ns
58	< intentionally blank >	—	—	—
59	Output Data Setup to Clock Falling Edge (Internal Clock)	tSCC/4 + T_L - 26	—	ns
60	Output Data Hold After Clock Rising Edge (Internal Clock)	tSCC/4 -T_L - 8	—	ns
61	Input Data Setup Time Before Clock Rising Edge (Internal Clock)	tSCC/4 + T_L + 23	—	ns
62	Input Data Not Valid Before Clock Rising Edge (Internal Clock)	—	tSCC/4 + T_L - 5.5	ns
63	Clock Falling Edge to Output Data Valid (External Clock)	—	32.5	ns
64	Output Data Hold After Clock Rising Edge (External Clock)	T_C + 3	—	ns
65	Input Data Setup Time Before Clock Rising Edge (External Clock)	16	—	ns
66	Input Data Hold Time After Clock Rising Edge (External Clock)	21	—	ns

Table 15 SCI Asynchronous Mode Timing — 1X Clock

Num	Characteristics	40/66 MHz		Unit
		Min	Max	
67	Asynchronous Clock Cycle - tACC	$64 \times T_C$	—	ns
68	Clock Low Period	tACC/2 -11	—	ns
69	Clock High Period	tACC/2 -11	—	ns
70	< intentionally blank >	—	—	—
71	Output Data Setup to Clock Rising Edge (Internal Clock)	tACC/2 -51	—	ns
72	Output Data Hold After Clock Rising Edge (Internal Clock)	tACC/2 -51	—	ns

Internal Clock



External Clock

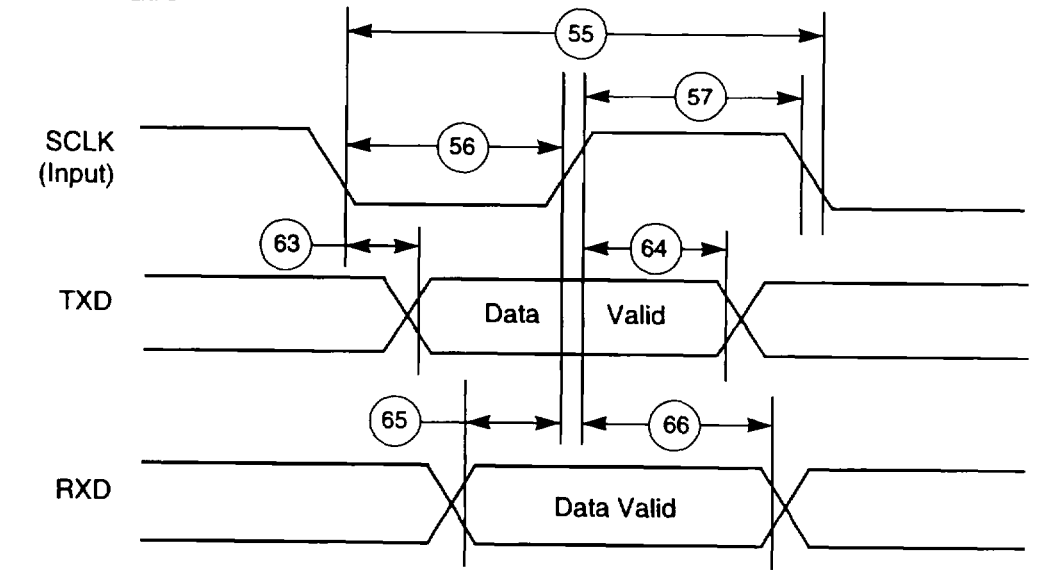
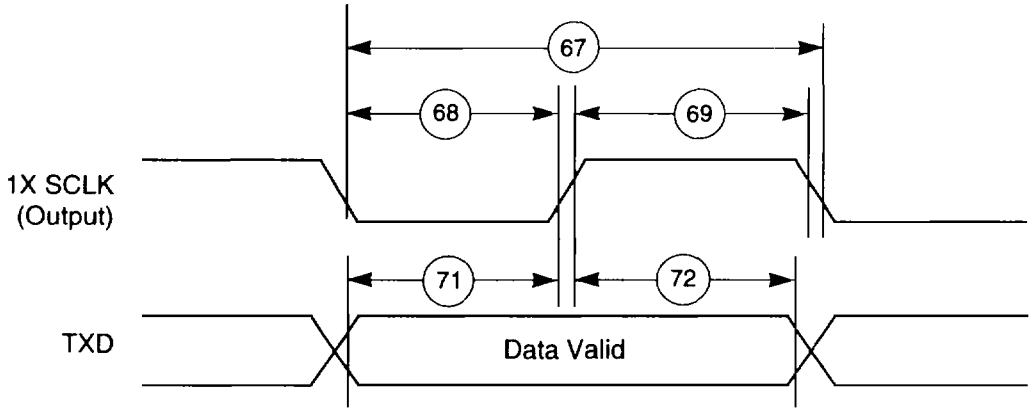


Figure 18 SCI Synchronous Mode Timing



NOTE: In the wire-OR mode, TXD can be pulled up by 1 KΩ

Figure 19 SCI Asynchronous Mode Timing

Synchronous Serial Interface (SSI) Timing

DSP56002: V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105° C, C_L = 50 pF + 2 TTL Loads

DSP56L002: V_{CC} = 3.3 Vdc ± 0.3 V, T_J = 0° to +80° C, C_L = 50 pF + 2 TTL Loads

tSSICC = SSI clock cycle time
TXC (SCK Pin) = Transmit Clock
RXC (SC0 or SCK Pin) = Receive Clock
FST (SC2 Pin) = Transmit Frame Sync
FSR (SC1 or SC2 Pin) = Receive Frame Sync
i ck = Internal Clock
x ck = External Clock
g ck = Gated Clock
i ck a = Internal Clock, Asynchronous Mode (Asynchronous implies that STD and SRD are two different clocks)
i ck s = Internal Clock, Synchronous Mode (Synchronous implies that STD and SRD are the same clock)
bl = bit length
wl = word length

Table 16 SSI Timing

Num	Characteristics	40/66 MHz		Case	Unit
		Min	Max		
80	Clock Cycle-tSSICC (See Note 1)	$4 \times T_C$ $3 \times T_C$	— —	i ck x ck	ns
81	Clock High Period	tSSICC/2 - 10.8 $T_C + T_L$	— —	i ck x ck	ns
82	Clock Low Period	tSSICC/2 - 10.8 $T_C + T_L$	— —	i ck x ck	ns
83	< intentionally blank >	—	—	—	—
84	RXC Rising Edge to FSR Out (bl) High	— —	40.8 25.8	x ck i ck a	ns
85	RXC Rising Edge to FSR Out (bl) Low	— —	35.8 25.8	x ck i ck a	ns
86	RXC Rising Edge to FSR Out (wl) High	— —	35.8 20.8	x ck i ck a	ns

Table 16 SSI Timing (continued)

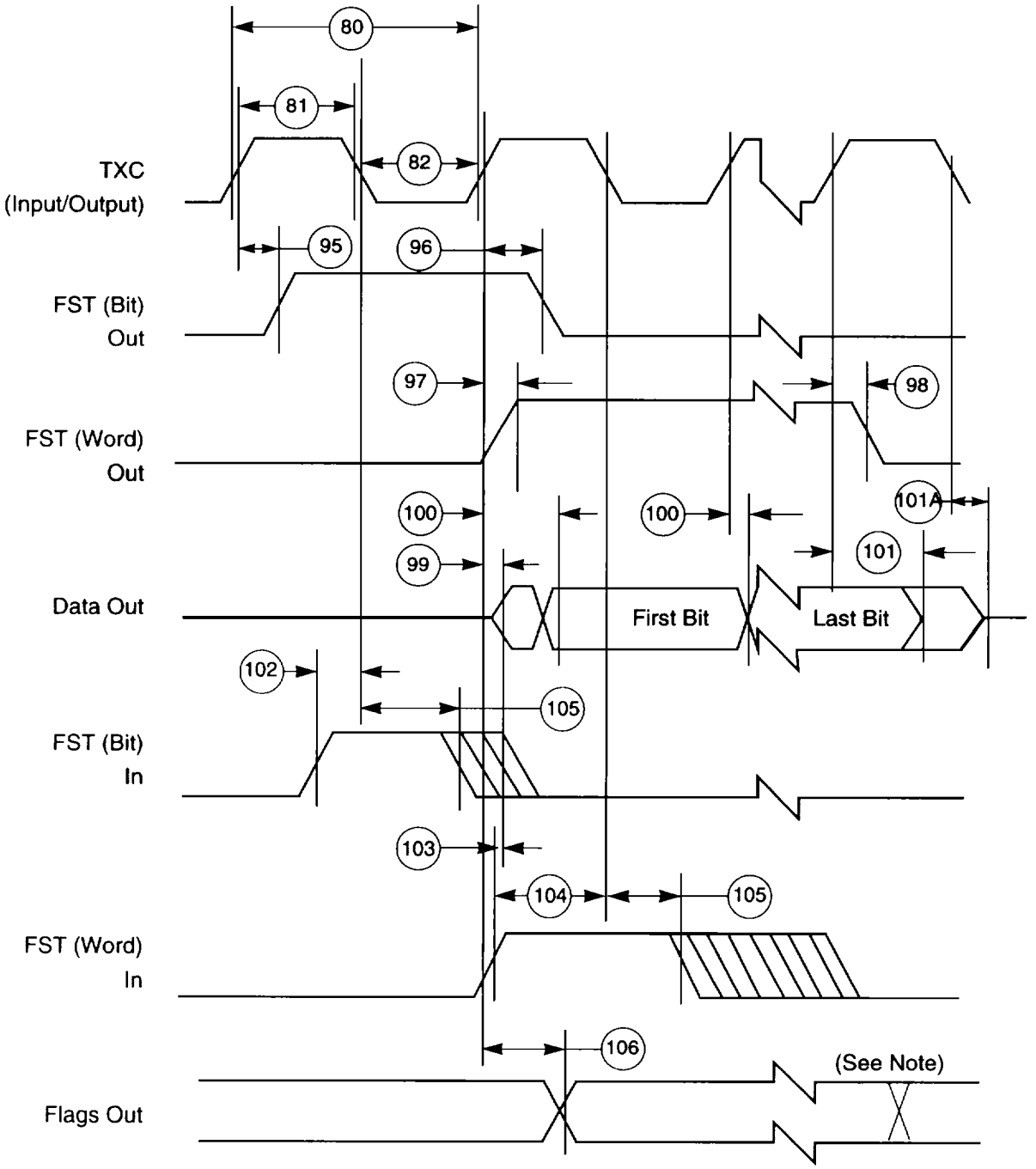
Num	Characteristics	40/66 MHz		Case	Unit
		Min	Max		
87	RXC Rising Edge to FSR Out (wl) Low	— —	35.8 20.8	x ck i ck a	ns
88	Data In Setup Time Before RXC (SCK in Synchronous Mode) Falling Edge	3.3 15.8 13	— — —	x ck i ck a i ck s	ns
89	Data In Hold Time After RXC Falling Edge	18 3.3	— —	x ck i ck	ns
90	FSR Input (bl) High Before RXC Falling Edge	0.8 17.4	— —	x ck i ck a	ns
91	FSR Input (wl) High Before RXC Falling Edge	3.3 18.3	— —	x ck i ck a	ns
92	FSR Input Hold Time After RXC Falling Edge	18.3 3.3	— —	x ck i ck	ns
93	Flags Input Setup Before RXC Falling Edge	0.8 16.7	— —	x ck i ck s	ns
94	Flags Input Hold Time After RXC Falling Edge	18.3 3.3	— —	x ck i ck s	ns
95	TXC Rising Edge to FST Out (bl) High	— —	31.6 15.8	x ck i ck	ns
96	TXC Rising Edge to FST Out (bl) Low	— —	33.3 18.3	x ck i ck	ns
97	TXC Rising Edge to FST Out (wl) High	— —	30.8 18.3	x ck i ck	ns
98	TXC Rising Edge to FST Out (wl) Low	— —	33.3 18.3	x ck i ck	ns
99	TXC Rising Edge to Data Out Enable from High Impedance	—	$33.3 + T_H$ 20.8	x ck i ck	ns
100	TXC Rising Edge to Data Out Valid	—	$33.3 + T_H$ 22.4	x ck i ck	ns

Table 16 SSI Timing (continued)

Num	Characteristics	40/66 MHz		Case	Unit
		Min	Max		
101	TXC Rising Edge to Data Out High Impedance (See Note 2)	— —	35.8 20.8	x ck i ck	ns
101A	TXC Falling Edge to Data Out High Impedance (See Note 2)	—	$T_C + T_H$	g ck	ns
102	FST Input (bl) Setup Time Before TXC Falling Edge	0.8 18.3	 —	x ck i ck	ns
103	FST Input (wl) to Data Out Enable from High Impedance	—	30.8		ns
104	FST Input (wl) Setup Time Before TXC Falling Edge	0.8 20.0	— —	x ck i ck	ns
105	FST Input Hold Time After TXC Falling Edge	18.3 3.3	— —	x ck i ck	ns
106	Flag Output Valid After TXC Rising Edge	— —	32.5 20.8	x ck i ck	ns

NOTES:

1. For internal clock, External Clock Cycle is defined by I_{cyc} and SSI control register.
2. Periodically sampled, and not 100% tested



NOTE: In the Network mode, output flag transitions can occur at the start of each time slot within the frame. In the Normal mode, the output flag state is asserted for the entire frame period.

Figure 20 SSI Transmitter Timing

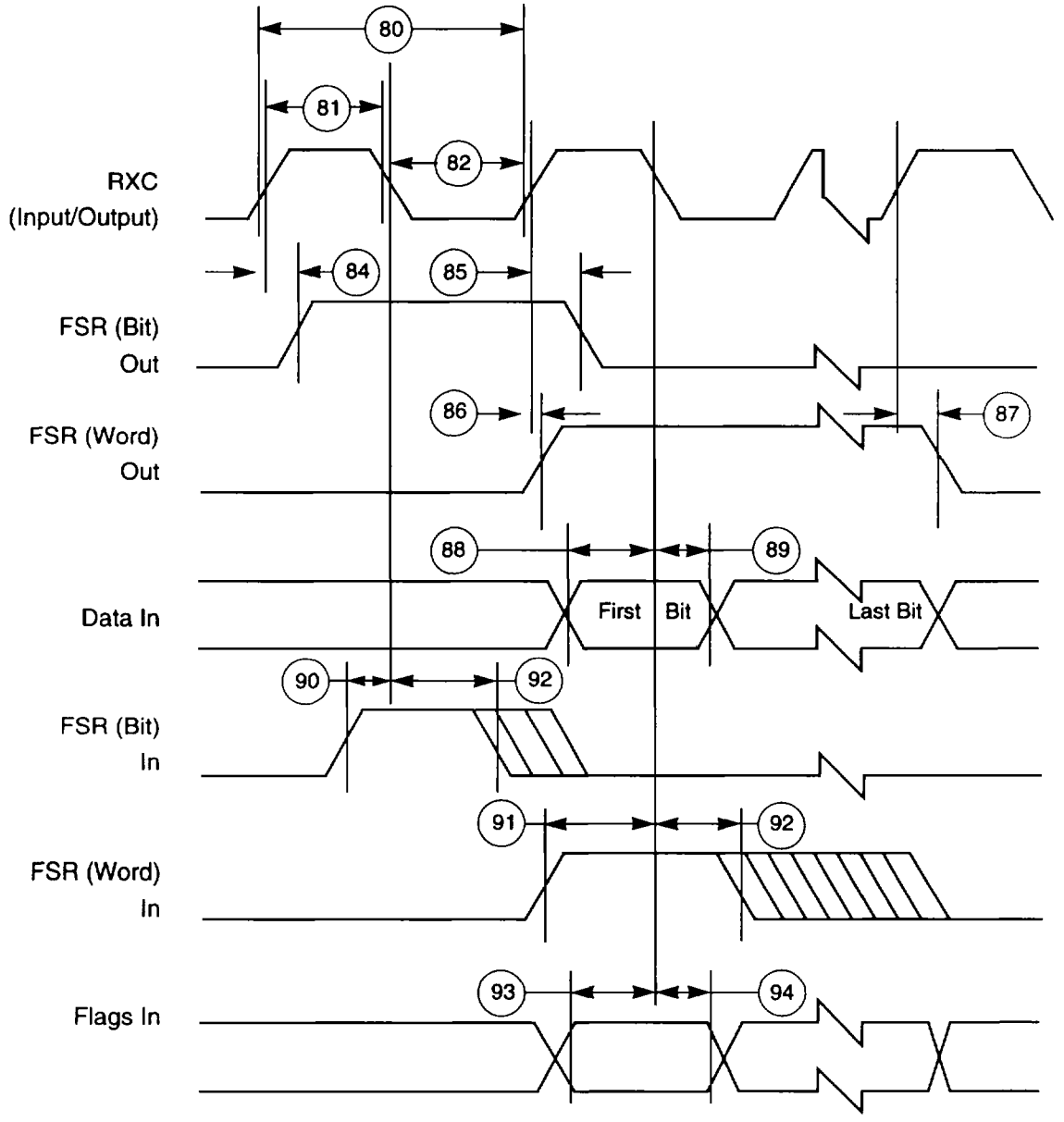


Figure 21 SSI Receiver Timing

External Bus Asynchronous Timing

DSP56002: V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105° C, C_L = 50 pF + 2 TTL Loads

DSP56L002: V_{CC} = 3.3 Vdc ± 0.3 V, T_J = 0° to +80° C, C_L = 50 pF + 2 TTL Loads

WS = Number of Wait States, as determined by BCR register (WS = 0 to 15)

Capacitance Derating

The DSP56002/L002 External Bus Timing Specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the External Bus pins (A0-A15, D0-D23, $\overline{PS}$, $\overline{DS}$, $\overline{RD}$, $\overline{WR}$, X/$\overline{Y}$, $\overline{EXTP}$) derates linearly at 1 ns per 12 pF of additional capacitance from 50 pF to 250 pF of loading. Port B and C pins (HI, SCI, SSI, and Timer) derate linearly at 1 ns per 5 pF of additional capacitance from 50 pF to 250 pF of loading. Active low lines should be "pulled up" in a manner consistent with the AC and DC specifications.

Table 17 External Bus Asynchronous Timing

Num	Characteristics	40 MHz		66 MHz		Unit
		Min	Max	Min	Max	
115	Delay from $\overline{BR}$ Assertion to $\overline{BG}$ Assertion					
	• With no external access from the DSP	$2T_C + T_H$	$4T_C + T_H + 14$	$2T_C + T_H$	$4T_C + T_H + 14$	ns
	• During external read or write access	$T_C + T_H$	$4T_C + T_H + (T_C \times WS) + 14$	$T_C + T_H$	$4T_C + T_H + (T_C \times WS) + 14$	ns
	• During external read-modify-write access	$T_C + T_H$	$6T_C + T_H + (2 \times T_C \times WS) + 14$	$T_C + T_H$	$6T_C + T_H + (2 \times T_C \times WS) + 14$	ns
	• During Stop mode - external bus will not be released and $\overline{BG}$ will not go low	∞	14	∞	14	ns
	• During Wait mode	T_H	$T_C + T_H + 15$	T_H	$T_C + T_H + 15$	ns
116	Delay from $\overline{BR}$ Deassertion to $\overline{BG}$ Deassertion	$2 \times T_C$	$4 \times T_C + 12.5$	$2 \times T_C$	$4 \times T_C + 12.5$	ns
117	$\overline{BG}$ Deassertion Duration					
	• During Wait mode	$T_C - 5.5$	—	$T_C - 5.5$	—	ns
	• All other cases	$2 \times T_C + T_H - 5.5$	—	$2 \times T_C + T_H - 5.5$	—	ns
118	Delay from Address, Data, and Control Bus High Impedance to $\overline{BG}$ Assertion	0	—	0	—	ns
119	Delay from $\overline{BG}$ Deassertion to Address and Control Bus Enabled	0	T_H	0	T_H	ns

Table 17 External Bus Asynchronous Timing (continued)

Num	Characteristics	40 MHz		66 MHz		Unit
		Min	Max	Min	Max	
120	Address Valid to $\overline{WR}$ Assertion • WS = 0 • WS > 0	 $T_L - 6$ $T_C - 6$	 — —	 $T_L - 4.5$ $T_C - 4.5$	 — —	 ns ns
121	$\overline{WR}$ Assertion Width • WS = 0 • WS > 0	 $T_C - 4$ $WS \times T_C + T_L$	 — —	 $T_C - 4$ $WS \times T_C + T_L$	 — —	 ns ns
122	$\overline{WR}$ Deassertion to Address Not Valid	$T_H - 6$	—	$T_H - 4$	—	ns
123	$\overline{WR}$ Assertion to Data Out Active From High Impedance • WS = 0 • WS > 0	 $T_H - 4$ 0	 — —	 $T_H - 4$ 0	 — —	 ns ns
124	Data Out Hold Time from $\overline{WR}$ Deassertion (the maximum specification is periodically sampled, and not 100% tested)	$T_H - 7$	$T_H - 2.5$	$T_H - 5$	$T_H - 1.5$	ns
125	Data Out Setup Time to $\overline{WR}$ Deassertion • WS = 0 • WS > 0	 $T_L - 0.8$ $WS \times T_C + T_L - 0.8$	 — —	 $T_L - 0.4$ $WS \times T_C + T_L - 0.4$	 — —	 ns
126	$\overline{RD}$ Deassertion to Address Not Valid	T_H	—	$T_H - 1$	—	ns
127	Address Valid to $\overline{RD}$ Deassertion • WS = 0 • WS > 0	 $T_C + T_L - 6$ $((WS + 1) \times T_C) + T_L - 6$	 — —	 $T_C + T_L - 6$ $((WS + 1) \times T_C) + T_L - 6$	 — —	 ns ns
128	Input Data Hold Time to $\overline{RD}$ Deassertion	0	—	0	—	ns
129	$\overline{RD}$ Assertion Width • WS = 0 • WS > 0	 $T_C - 4$ $((WS + 1) \times T_C) - 4$	 — —	 $T_C - 4$ $((WS + 1) \times T_C) - 4$	 — —	 ns ns
130	Address Valid to Input Data Valid • WS = 0 • WS > 0	 — —	 $T_C + T_L - 9.5$ $((WS+1) \times T_C) + T_L - 9.5$	 — —	 $T_C + T_L - 7$ $((WS+1) \times T_C) + T_L - 7$	 ns ns

Table 17 External Bus Asynchronous Timing (continued)

Num	Characteristics	40 MHz		66 MHz		Unit
		Min	Max	Min	Max	
131	Address Valid to $\overline{RD}$ Assertion	$T_L - 6$	—	$T_L - 4.5$	—	ns
132	$\overline{RD}$ Assertion to Input Data Valid					
	• WS = 0	—	$T_C - 7.5$	—	$T_C - 5.5$	ns
	• WS > 0	—	$((WS+1) \times T_C) - 7.5$	—	$((WS+1) \times T_C) - 5.5$	ns
133	$\overline{WR}$ Deassertion to $\overline{RD}$ Assertion	$T_C - 7$	—	$T_C - 5$	—	ns
134	$\overline{RD}$ Deassertion to $\overline{RD}$ Assertion	$T_C - 4$	—	$T_C - 2.5$	—	ns
135	$\overline{WR}$ Deassertion to $\overline{WR}$ Assertion					
	• WS = 0	$T_C - 4$	—	$T_C - 3$	—	ns
	• WS > 0	$T_C + T_H - 4$	—	$T_C + T_H - 3$	—	ns
136	$\overline{RD}$ Deassertion to $\overline{WR}$ Assertion					
	• WS = 0	$T_C - 4$	—	$T_C - 2.5$	—	ns
	• WS > 0	$T_C + T_H - 4$	—	$T_C + T_H - 2.5$	—	ns

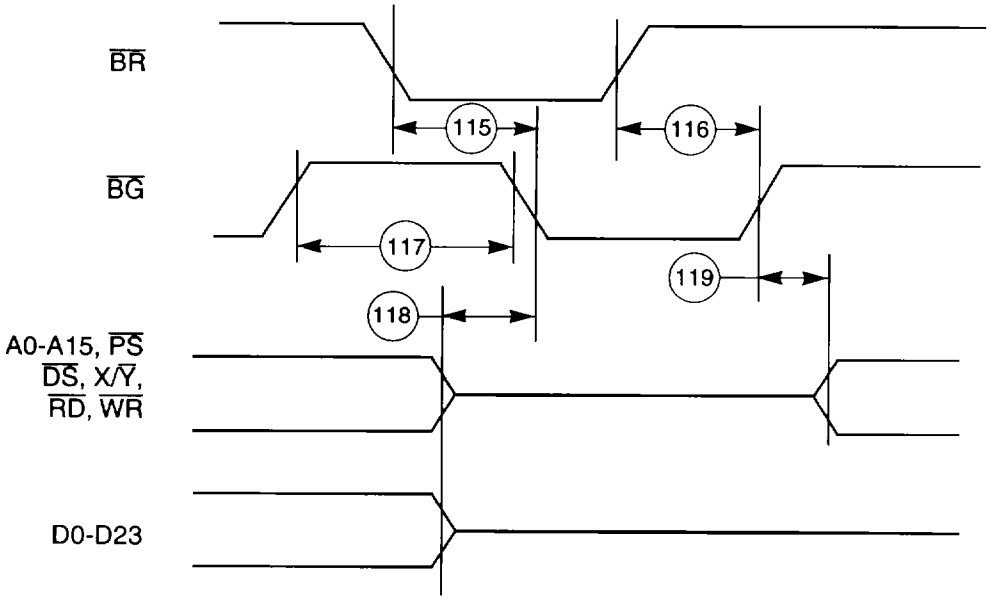
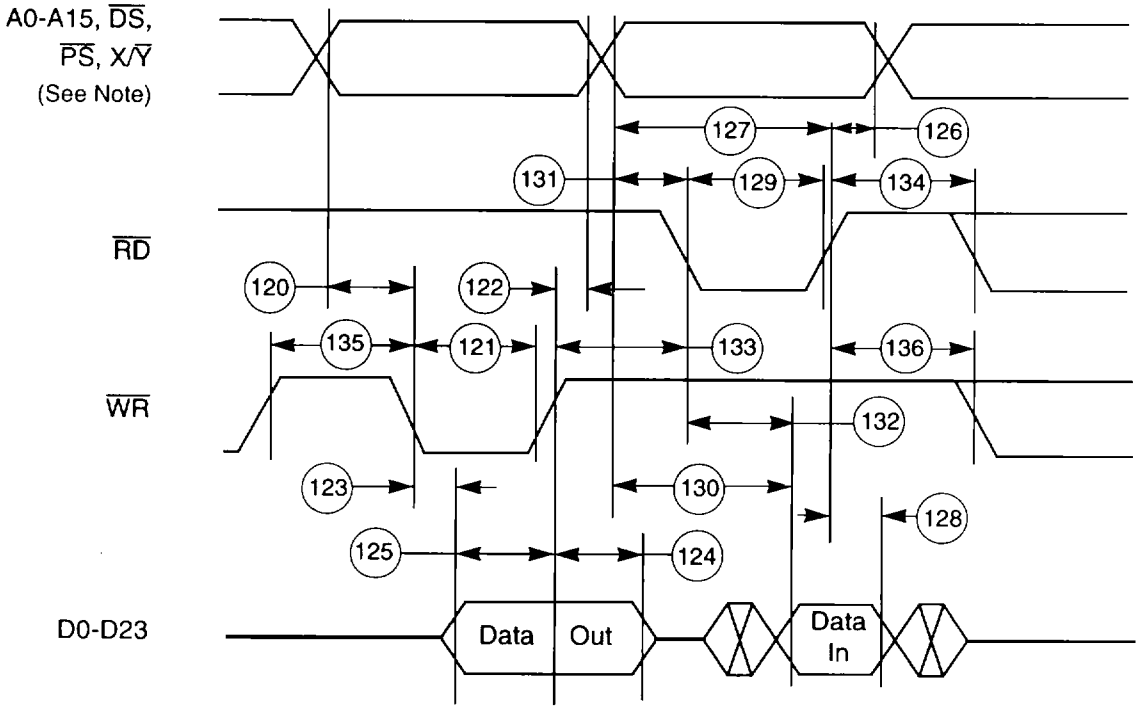


Figure 22 Bus Request / Bus Grant Timing



NOTE: During Read-Modify-Write instructions, the address lines do not change state.

Figure 23 External Bus Asynchronous Timing

External Bus Synchronous Timing

DSP56002: V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105° C, C_L = 50 pF + 2 TTL Loads

DSP56L002: V_{CC} = 3.3 Vdc ± 0.3 V, T_J = 0° to +80° C, C_L = 50 pF + 2 TTL Loads

Capacitance Derating

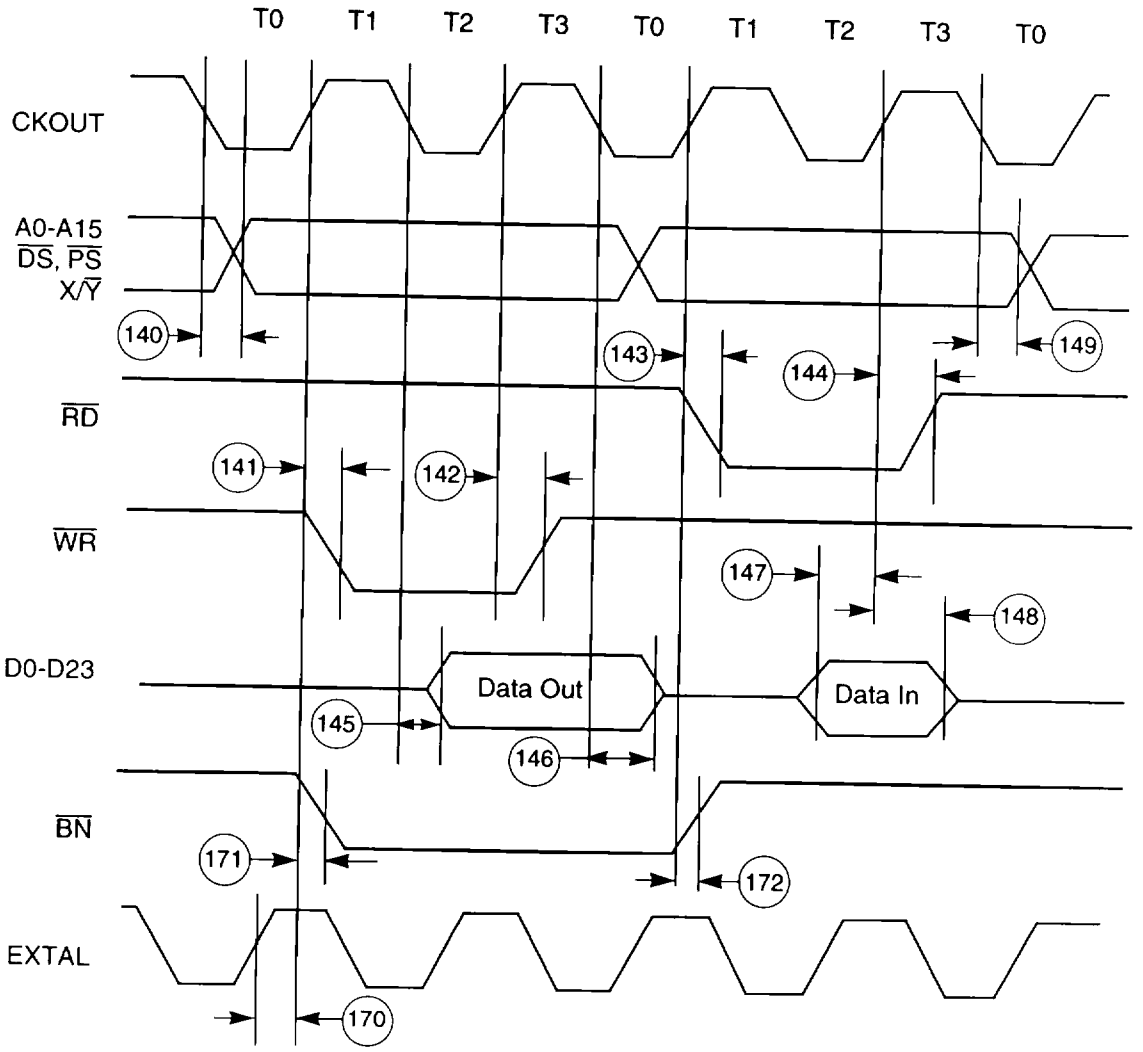
The DSP56002/L002 external bus timing specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the external bus pins (A0-A15, D0-D23, $\overline{PS}$, $\overline{DS}$, $\overline{RD}$, $\overline{WR}$, X/$\overline{Y}$, $\overline{EXTP}$) derates linearly at 1 ns per 12 pF of additional capacitance from 50 pF to 250 pF of loading. Port B and C pins (HI, SCI, SSI, and Timer) derate linearly at 1 ns per 5 pF of additional capacitance from 50 pF to 250 pF of loading. Active-low lines should be "pulled up" in a manner consistent with the AC and DC specifications.

Table 18 External Bus Synchronous Timing

Num	Characteristics	40 MHz		66 MHz		Unit
		Min	Max	Min	Max	
140	CKOUT transition #1 to Address Valid	—	6.2	—	5	ns
141	CKOUT transition #2 to $\overline{WR}$ Assertion • WS=0 • WS>0 (See Note 1)	 — —	 4.4 T_H + 4.4	 — —	 4 T_H + 4	 ns ns
142	CKOUT transition #2 to $\overline{WR}$ Deassertion	1.3	9.1	1	5	ns
143	CKOUT transition #2 to $\overline{RD}$ Assertion	—	3.9	—	3.9	ns
144	CKOUT transition #2 to $\overline{RD}$ Deassertion	0	3.4	-3	3	ns
145	CKOUT transition #1 to Data-Out Valid	—	5.4	—	4.5	ns
146	CKOUT transition #1 to Data-Out Invalid (See Note 3)	0	—	0	—	ns
147	Data-In Valid to CKOUT transition #2 (Setup)	3.4	—	3.4	—	ns
148	CKOUT transition #2 to Data-In Invalid (Hold)	0	—	0	—	ns
149	CKOUT transition #1 to Address Invalid (See Note 3)	0	—	0	—	ns

NOTES:

1. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition.
2. WS are wait state values specified in the BCR.
3. CKOUT transition #1 to data-out invalid (specification # T146) and CKOUT transition #1 to address invalid (specification # T149) indicate the time after which data/address are no longer guaranteed to be valid.
4. Timings are given from CKOUT midpoint to V_{OL} or V_{OH} of the corresponding pin(s).
5. CKOUT transition #1 is a falling edge of CKOUT for CKP=0.



NOTE: During Read-Modify-Write Instructions, the address lines do not change states.

Figure 24 Synchronous Bus Timing

Bus Strobe / Wait Timing

DSP56002: V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105° C, C_L = 50 pF + 2 TTL Loads

DSP56L002: V_{CC} = 3.3 Vdc ± 0.3 V, T_J = 0° to +80° C, C_L = 50 pF + 2 TTL Loads

Table 19 Bus Strobe / Wait Timing

Num	Characteristics	40/66 MHz		Unit
		Min	Max	
150	CKOUT transition #1 to $\overline{BS}$ Assertion	—	5.6	ns
151	WT Assertion to CKOUT transition #1(setup time)	5.3	—	ns
152	CKOUT transition #1 to $\overline{WT}$ Deassertion for Minimum Timing	0	T_C - 7.9	ns
153	$\overline{WT}$ Deassertion to CKOUT transition #1 for Maximum Timing (2 wait states)	7.9	—	ns
154	CKOUT transition #2 to $\overline{BS}$ Deassertion	—	5.2	ns
155	$\overline{BS}$ Assertion to Address Valid	0	2.4	ns
156	$\overline{BS}$ Assertion to $\overline{WT}$ Assertion (See Note 1)	0	T_C - 10.9	ns
157	$\overline{BS}$ Assertion to $\overline{WT}$ Deassertion (See Note 1 and Note 3)	(WS-1) × T_C	WS × T_C - 13.5	ns
158	$\overline{WT}$ Deassertion to $\overline{BS}$ Deassertion	T_C + T_L + 3.3	2 × T_C+T_L+7.8	ns
159	Minimum $\overline{BS}$ Deassertion Width for Consecutive External Accesses	T_H - 1	—	ns
160	$\overline{BS}$ Deassertion to Address Invalid (See Note 2)	T_H - 4.6	—	ns
161	Data-In Valid to $\overline{RD}$ Deassertion (Set Up)	3.4	—	ns
162	$\overline{BR}$ Assertion to CKOUT transition #2 for Minimum Timing	9.5	T_C	ns
163	$\overline{BR}$ Deassertion to CKOUT transition #2 for Minimum Timing	8	T_C	ns
164	CKOUT transition #1 to BG Assertion	—	8.8	ns
165	CKOUT transition #1 to BG Deassertion	—	5.3	ns
170	EXTAL to CKOUT- PLL Disabled EXTAL to CKOUT - PLL Enabled and MF < 5 (See Note 5)	3 0.3	9.7 3.7	ns ns
171	CKOUT transition #2 to $\overline{BN}$ Assertion	—	5.7	ns
172	CKOUT transition #2 to $\overline{BN}$ Deassertion	—	5	ns

NOTES:

1. If wait states are also inserted using the BCR and if the number of wait states is greater than 2, then specification numbers 156 and 157 can be increased accordingly.

(Notes continued on next page)

2. $\overline{BS}$ deassertion to address invalid indicates the time after which the address are no longer guaranteed to be valid.
3. The minimum number of wait states when using $\overline{BS}/\overline{WT}$ is two (2).
4. For read-modify-write instructions, the address lines will not change states between the read and the write cycle. However, $\overline{BS}$ will deassert before asserting again for the write cycle. If wait states are desired for each of the read and write cycle, the $\overline{WT}$ pin must be asserted once for each cycle.
5. When EXTAL frequency is less than 33 MHz, then timing 170 is not guaranteed for a period of $1000 \times T_C$ after PLOCK assertion following the events below:
   - when enabling the PLL operation by software.
   - when changing the multiplication factor.
   - when recovering from the stop state if the PLL was turned off and it is supposed to turn on when exiting the stop state.

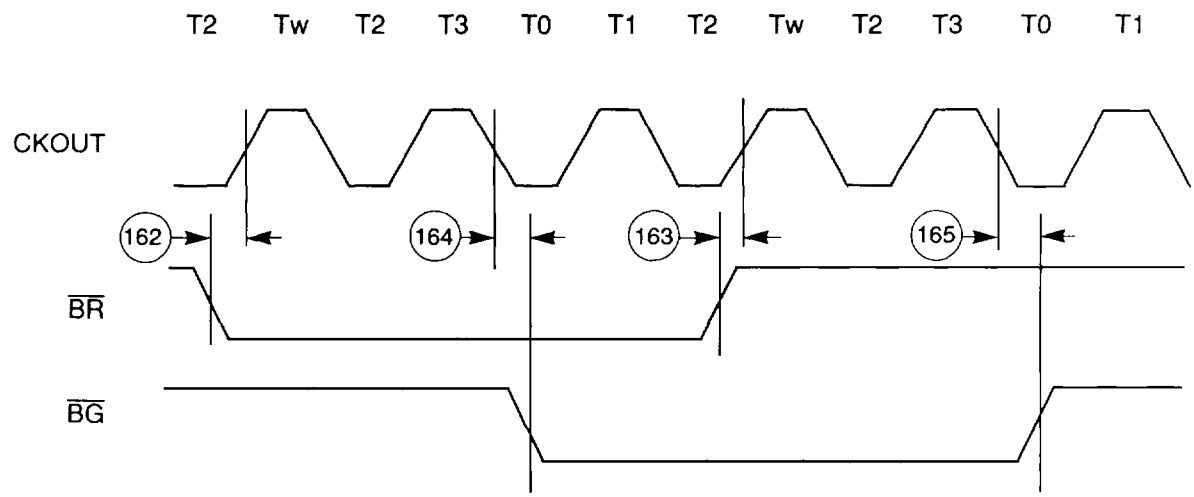
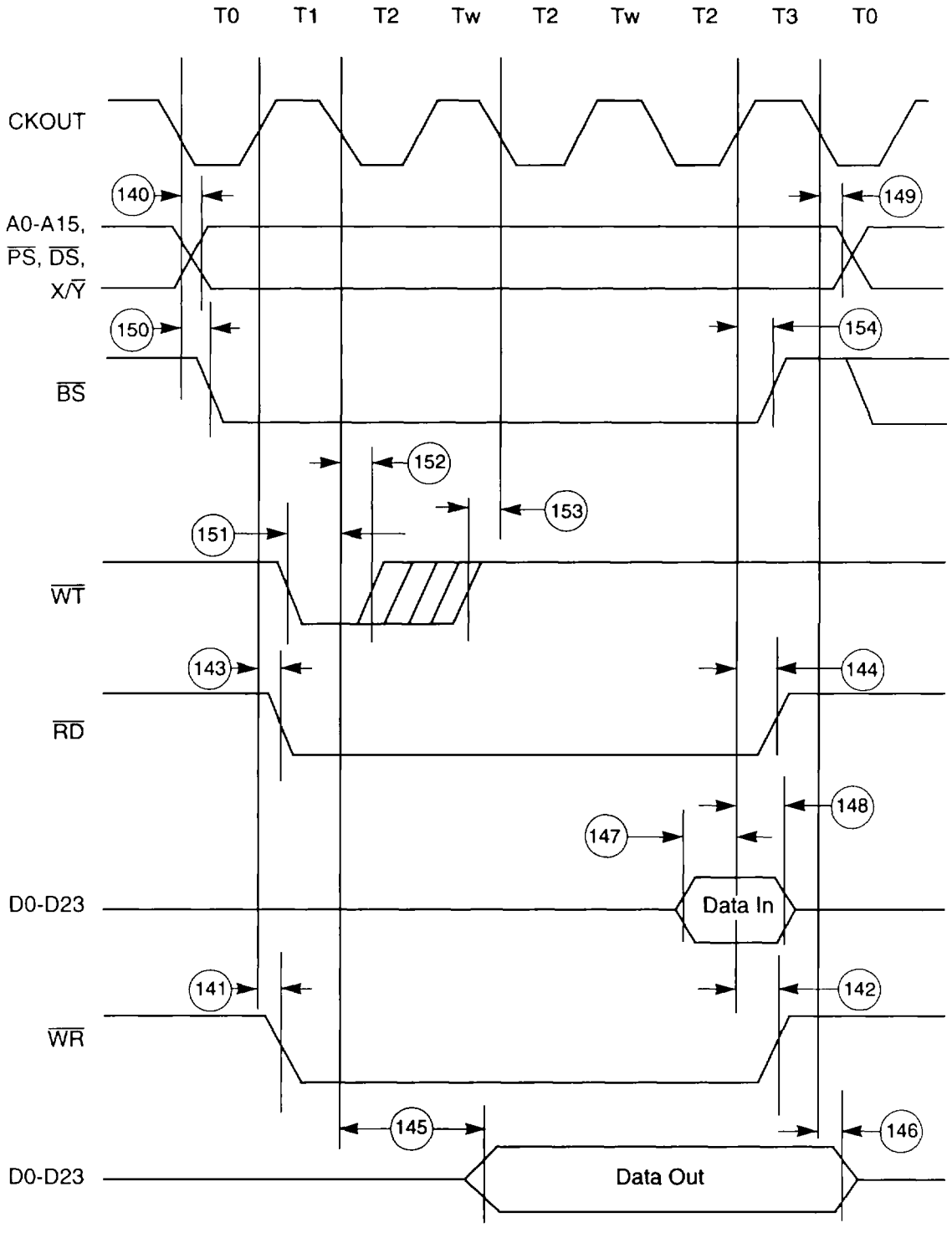
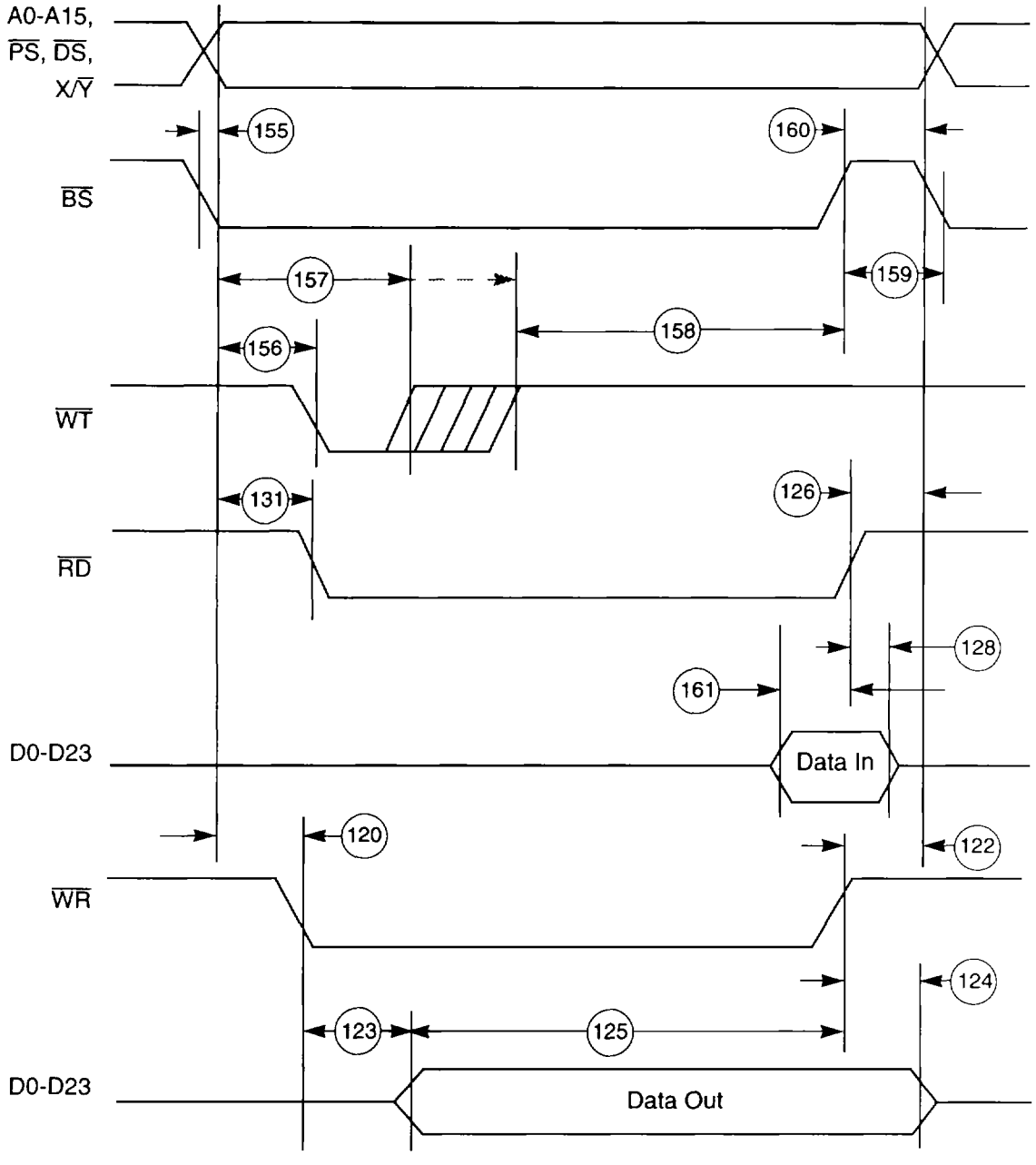


Figure 25 Synchronous Bus Request / Bus Grant Timing



NOTE: During Read-Modify-Write Instructions, the address lines do not change state. However, $\overline{BS}$ will deassert before asserting again for the write cycle.

Figure 26 Synchronous $\overline{BS}$ / $\overline{WT}$ Timings



NOTE: During Read-Modify-Write instructions, the address lines do not change state. However, $\overline{BS}$ will deassert before asserting again for the write cycle.

Figure 27 Asynchronous $\overline{BS}$ / $\overline{WT}$ Timings

OnCE™ Port Timing

DSP56002: V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105° C, C_L = 50 pF + 2 TTL Loads

DSP56L002: V_{CC} = 3.3 Vdc ± 0.3 V, T_J = 0° to +80° C, C_L = 50 pF + 2 TTL Loads

Table 20 OnCE™ Port Timing

Num	Characteristics	40/66 MHz		Unit
		Min	Max	
230	DSCK Low	40	—	ns
231	DSCK High	40	—	ns
232	DSCK Cycle Time	200	—	ns
233	$\overline{DR}$ Asserted to DSO ($\overline{ACK}$) Asserted	$5T_C$	—	ns
234	DSCK High to DSO Valid	—	42	ns
235	DSCK High to DSO Invalid	3	—	ns
236	DSI Valid to DSCK Low (Setup)	15	—	ns
237	DSCK Low to DSI Invalid (Hold)	3	—	ns
238	Last DSCK Low to OS0-OS1, $\overline{ACK}$ Active	$3T_C + T_L$	—	ns
239	DSO ($\overline{ACK}$) Asserted to First DSCK High	$2T_C$	—	ns
240	DSO ($\overline{ACK}$) Assertion Width	$4T_C + T_H - 3$	$5T_C + 7$	ns
241	DSO ($\overline{ACK}$) Asserted to OS0-OS1 High Impedance (See Note 2)	—	0	ns
242	OS0-OS1 Valid to CKOUT transition #2	$T_C - 21$	—	ns
243	CKOUT transition #2 to OS0-OS1 Invalid	0	—	ns
244	Last DSCK Low of Read Register to First DSCK High of Next Command	$7T_C + 10$	—	ns
245	Last DSCK Low to DSO Invalid (Hold)	3	—	ns
246	$\overline{DR}$ Assertion to CKOUT transition #2 for Wake Up from WAIT State	12	T_C	ns
247	CKOUT transition #2 to DSO after Wake Up from Wait State	$17T_C$	—	ns
248	$\overline{DR}$ Assertion Width • to recover from Wait • to recover from Wait and enter Debug mode	 15 $13T_C + 15$	 $12T_C - 15$ —	ns
249	$\overline{DR}$ Assertion to DSO ($\overline{ACK}$) Valid (Enter Debug Mode) After Asynchronous Recovery from Wait State	$17T_C$	—	ns

Table 20 OnCE™ Port Timing (continued)

Num	Characteristics	40/66 MHz		Unit
		Min	Max	
250A	$\overline{DR}$ Assertion Width to Recover from Stop • Stable External Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 • Stable External Clock, PCTL bit 17= 1 (See Note 1)	 15 15 15	 $65548T_C + T_L$ $20T_C + T_L$ $13T_C + T_L$	ns
250B	$\overline{DR}$ Assertion Width to Recover from Stop and Enter Debug Mode • Stable External Clock,OMR bit 6 = 0 • Stable External Clock,OMR bit 6 = 1 • Stable External Clock,PCTL bit 17= 1 (See Note 1)	 $65549T_C + T_L$ $21T_C + T_L$ $14T_C + T_L$	 — — —	ns
251	$\overline{DR}$ Assertion to DSO ($\overline{ACK}$) Valid (Enter Debug Mode) after recovery from Stop State • Stable External Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 • Stable External Clock, PCTL bit 17= 1 (See Note 1)	 $65553T_C + T_L$ $25T_C + T_L$ $18T_C + T_L$	 — — —	ns

NOTES:

1. A clock stabilization delay is required when using the on-chip crystal oscillator in two cases:
   - after power-on reset, and
   - when recovering from Stop mode.

   During this stabilization period, T_C, T_H, and T_L will not be constant. Since this stabilization period varies, a delay of $75,000 \times T_C$ is typically allowed to assure that the oscillator is stable before executing programs. While it is possible to set OMR bit 6 = 1 when using the internal crystal oscillator, it is not recommended and these specifications do not guarantee timings for that case.
2. The maximum specified is periodically sampled and not 100% tested.

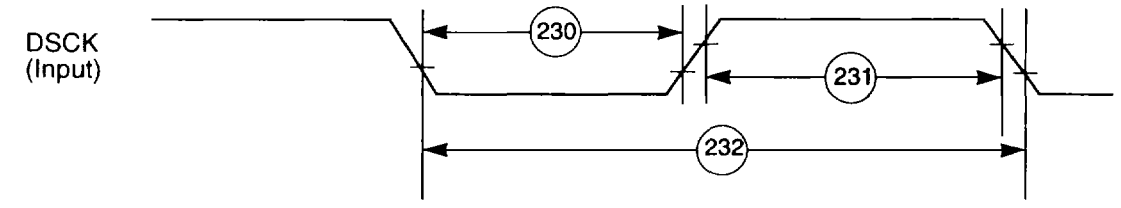


Figure 28 OnCE Serial Clock Timing

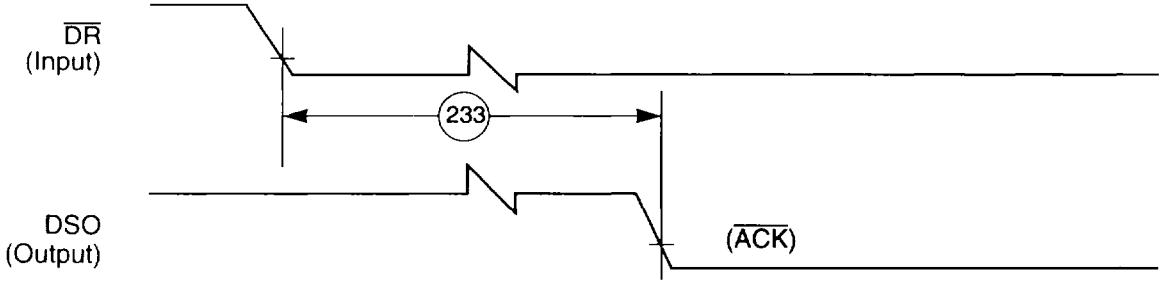
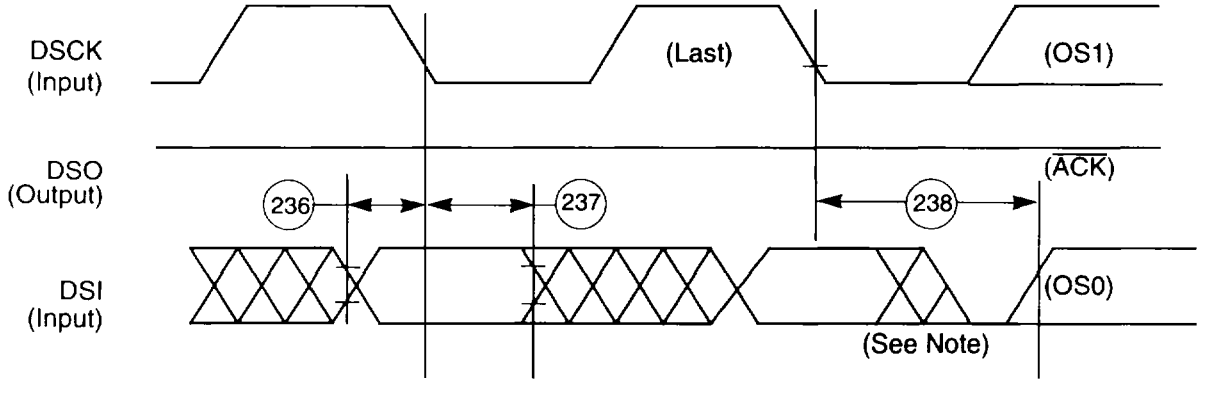
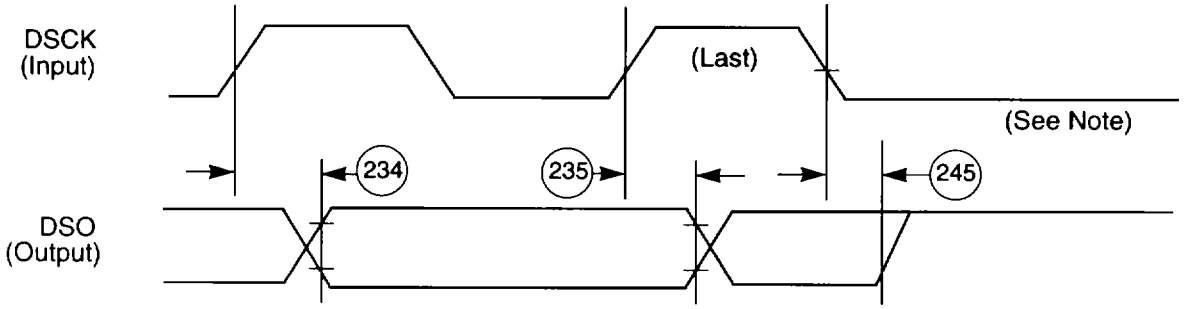


Figure 29 OnCE Acknowledge Timing



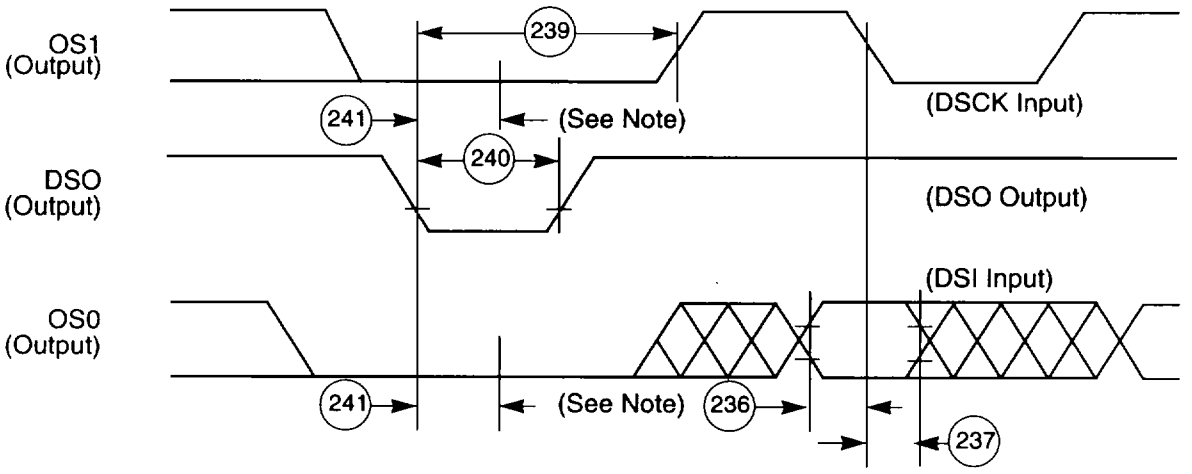
NOTE: High Impedance, external pull-down resistor

Figure 30 OnCE Data I/O To Status Timing



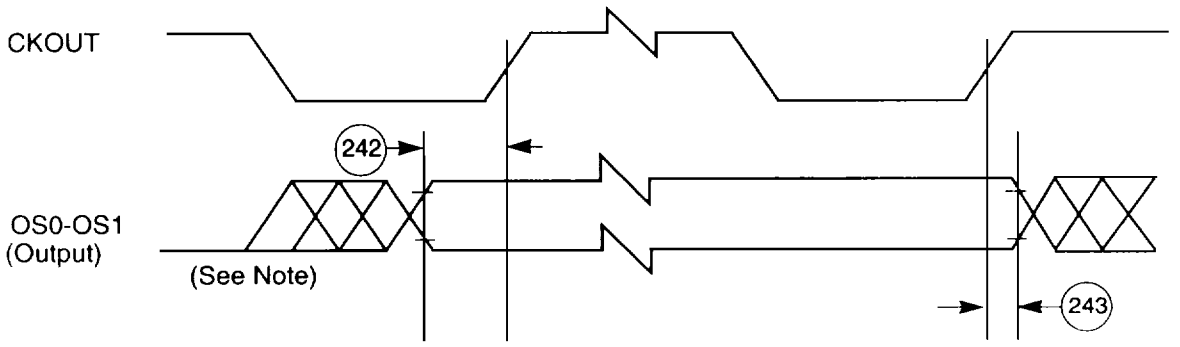
NOTE: High Impedance, external pull-down resistor

Figure 31 OnCE Read Timing



NOTE: High Impedance, external pull-down resistor

Figure 32 OnCE Data I/O To Status Timing



NOTE: High Impedance, external pull-down resistor

Figure 33 OnCE CKOUT To Status Timing

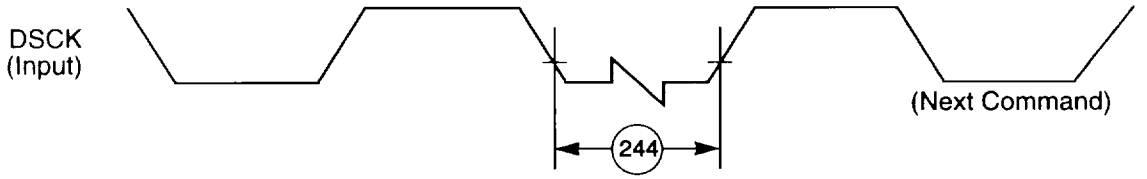


Figure 34 OnCE Read Register to Next Command Timing

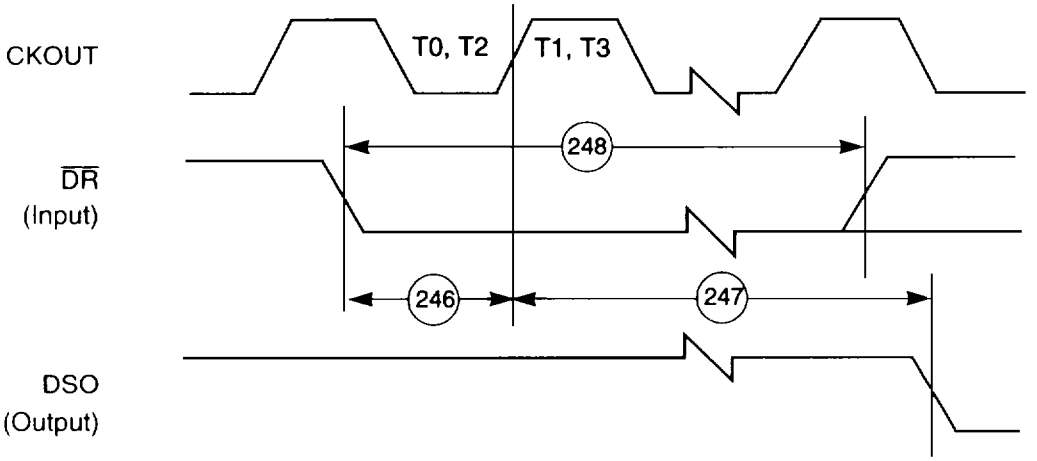


Figure 35 Synchronous Recovery from Wait State

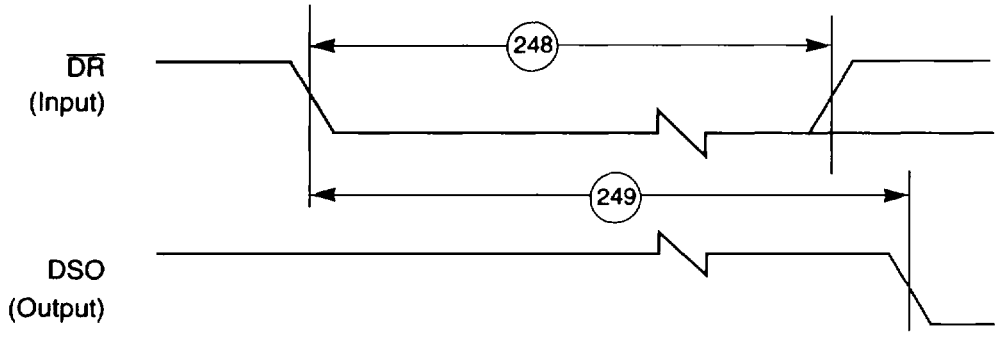


Figure 36 Asynchronous Recovery from Wait State

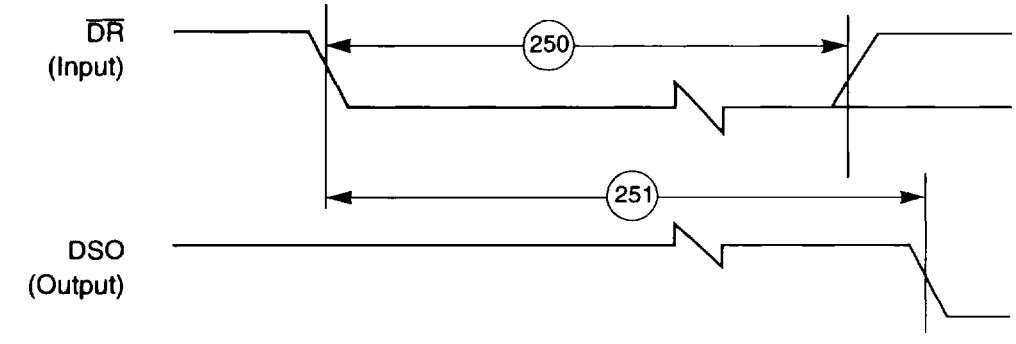


Figure 37 Asynchronous Recovery from Stop State

Timer Timing

DSP56002: V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105° C, C_L = 50 pF + 2 TTL Loads

DSP56L002: V_{CC} = 3.3 Vdc ± 0.3 V, T_J = 0° to +80° C, C_L = 50 pF + 2 TTL Loads

NOTE: Timer functions were not available in early versions of the DSP56002/L002. See Table 30 for more information. On earlier silicon the TIO signal was an "nc" (no connection) pin.

Table 21 Timer Timing

Num	Characteristics	40/66 MHz		Unit
		Min	Max	
260	TIO Low	$2T_C + 7$	—	ns
261	TIO High	$2T_C + 7$	—	ns
262	Synchronous Timer Setup Time from TIO (input) Assertion to CKOUT Rising Edge	10	T_C	ns
263	Synchronous Timer Delay Time from CKOUT Rising Edge to the External Memory Access Address Out Valid Caused by First Interrupt Instruction Execution	$5T_C + T_H$	—	ns
264	CKOUT Rising Edge to TIO (output) Assertion	0	8	ns
265	CKOUT Rising Edge to TIO (output) Deassertion	0	8	ns
266	CKOUT Rising Edge to TIO (General Purpose Output)	0	8	ns

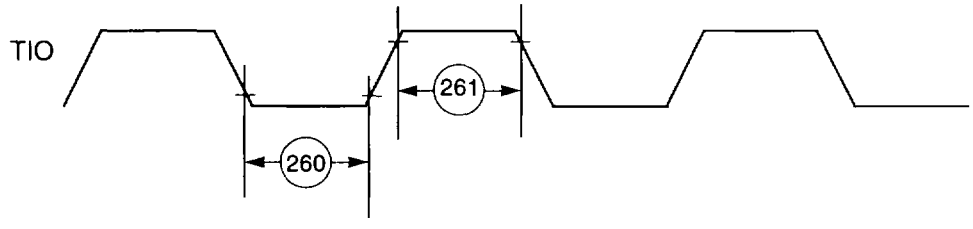


Figure 38 TIO Timer Event Input

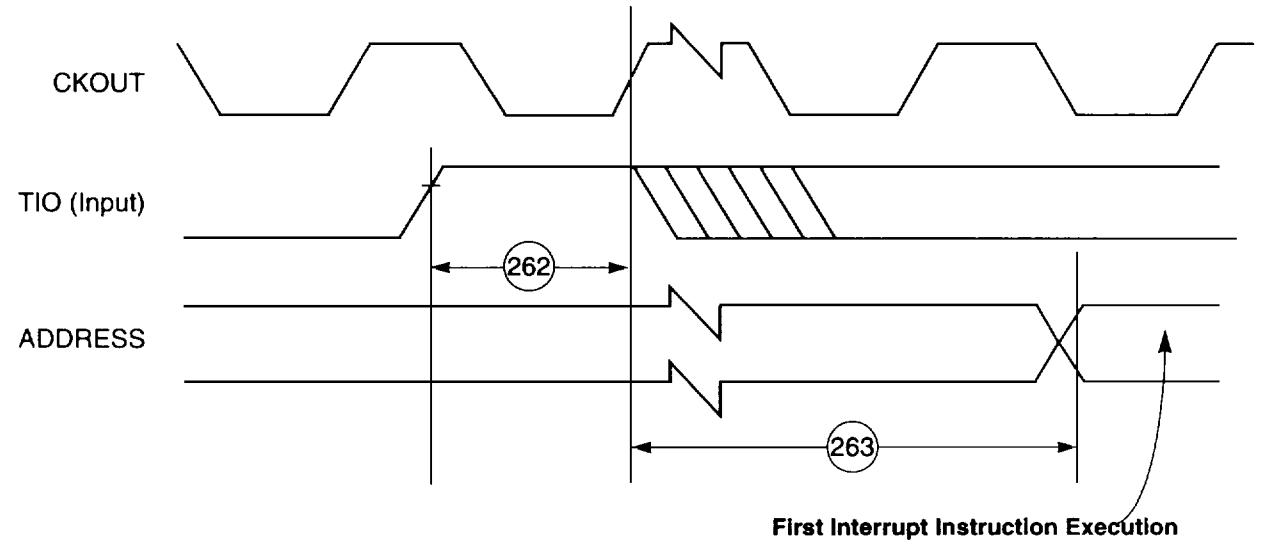


Figure 39 Timer Interrupt Generation

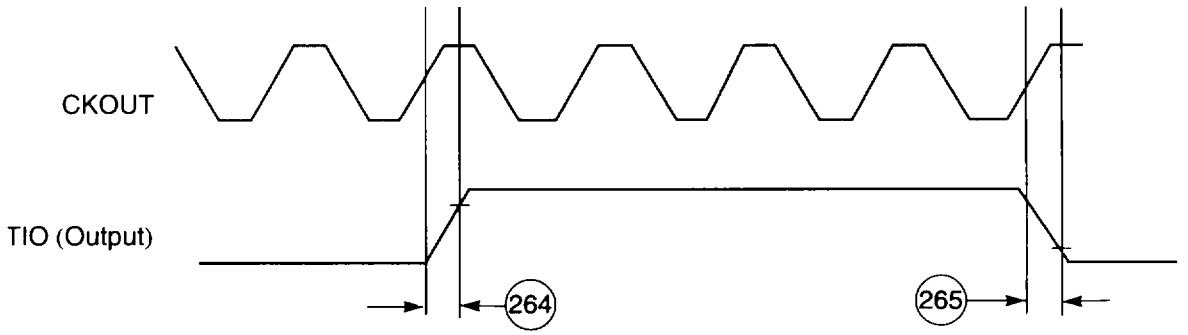


Figure 40 External Pulse Generation

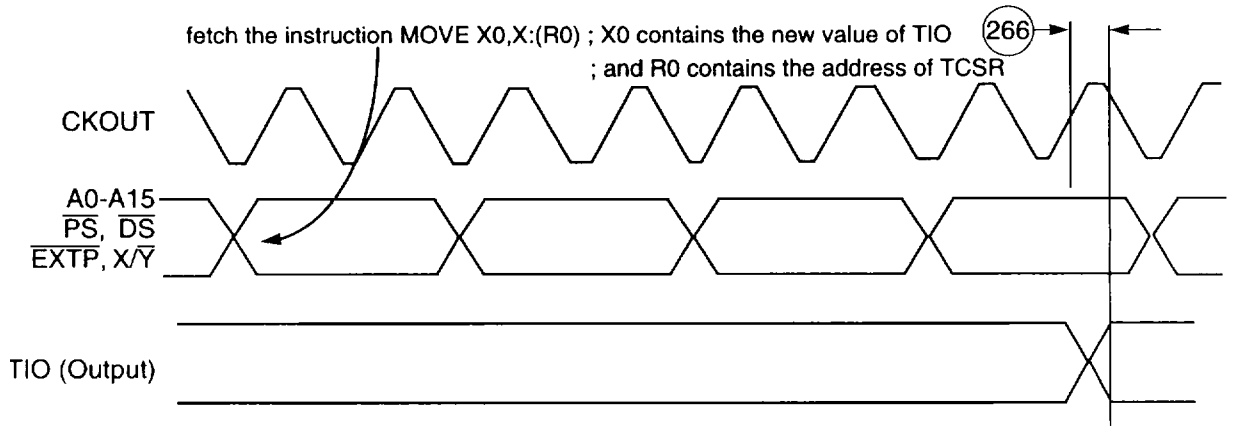


Figure 41 GPIO Output Timing