3.3V, 1-port, SATA2 i/m ReDriver™ with Analog/Digital Configuration

Features

- SATA2 i, m; external SATA2
- Two 3.0Gbps differential signal pairs
- Independent Digital Output Emphasis Control
- 100Ω Differential CML I/O's
- Input signal level detect and squelch for each channel
- OOB Support
- Enhanced Mode Features:
  - Adjustable Receiver Equalization
  - Independent Analog Output Swing Adjustment
  - Independent Analog Output Emphasis Control
  - Independent Channel Power Down Control
- Low Power (220mW per Channel)
- Stand-by Mode – Power Down State
- Supply Voltage: 3.3V
- Packaging (Pb-free & Green):
  - 20-TQFN (4x4mm)

Description

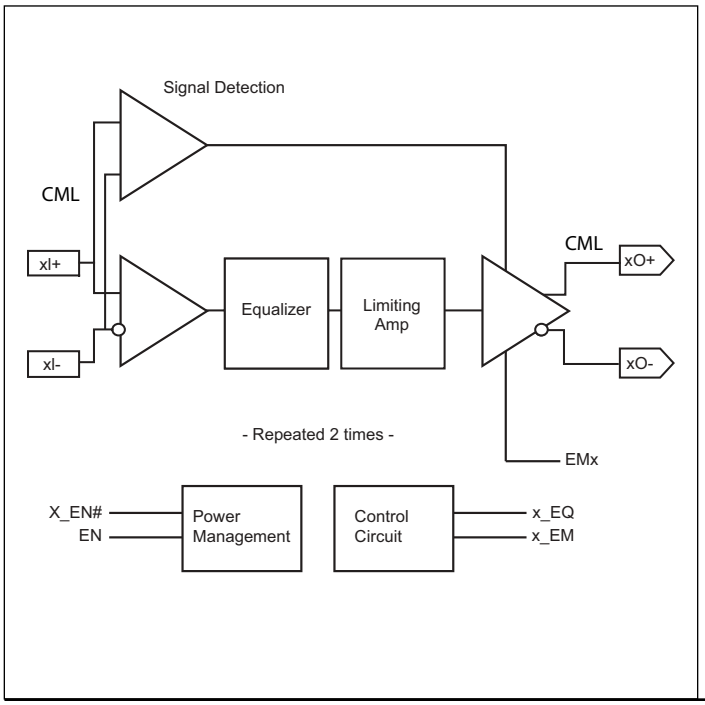
Pericom Semiconductor's PI3EQX4951B is a low power, signal ReDriver™. The device provides programmable equalization, to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI3EQX4951B supports two 100Ω Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver.

A low-level input signal detection and output squelch function is provided for each channel. Each channel operates fully independently. When the channels are enabled (x_EN=1) and operating, that channels input signal level (on xI+/-) determines whether the output is active. If the input signal level of the channel falls below the active threshold level (Vth-) then the outputs are driven to the common mode voltage.

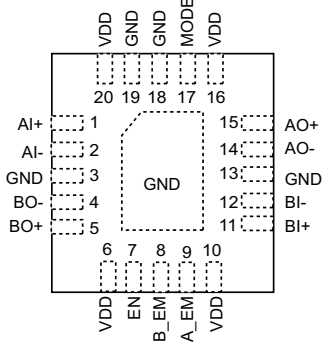
In addition to signal conditioning, when EN = 0, the device enters a low power standby mode.

Block Diagram

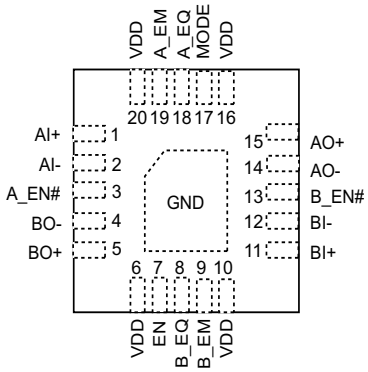


Pin Diagram (Top Side View)

Standard Mode (MODE = 0)



Enhanced Mode (MODE = 1)



Pin Description

Standard Mode Pin #	Enhanced Mode Pin #	Pin Name	Type	Description
9	19	A_EM	Input	Output emphasis adjustment for channel A. ▫ When in Standard Mode (MODE= 0) digital control is enabled, and a 100KΩ pull-up resistor is enabled on A_EM. ▫ When in Enhanced Mode (MODE= 1) analog resistive adjustment of emphasis is enabled. Refer to Configuration Tables and System Implementation diagrams for design guidelines.
—	3	A_EN#	Input	Channel A Enable, is active only when in Enhanced Mode (MODE=1). Low is normal operation. High is power down mode. Has internal 100KΩ pull-down resistor.
—	18	A_EQ	Input	Channel A Equalization adjustment is active only in Enhanced Mode (MODE = 1). With internal 100KΩ pull-up to V_{DD}. Refer to Enhanced Mode Configuration Table and System Implementation diagram for design guidelines.
1 2	1 2	AI+ AI-	Input	CML input forward channel A with internal 50Ω pull-up resistors connected to VBIAS (100Ω differential).
14 15	14 15	AO- AO+	Output	CML output channel A with internal 50Ω pull-up resistors connected to VBIAS (100Ω differential).
8	9	B_EM	Input	Output emphasis adjustment for channel B. ▫ When in Standard Mode (MODE= 0) digital control is enabled, and a 100KΩ pull-up resistor is enabled on A_EM. ▫ When in Enhanced Mode (MODE= 1) analog resistive adjustment of emphasis is enabled. Refer to Configuration Tables and System Implementation diagrams for design guidelines.
—	13	B_EN#	Input	Channel B Enable, is active only when in Enhanced Mode (MODE=1). Low is normal operation. High is power down mode. Has internal 100KΩ pull-down resistor.
—	8	B_EQ	Input	Channel A Equalization adjustment, is active only in Enhanced Mode (MODE = 1). With internal 100KΩ pull-up to V_{DD}. Refer to Enhanced Mode Configuration Table and System Implementation diagram for design guidelines.
11 12	11 12	BI+ BI-	Input	CML input return channel B with internal 50Ω pull-up, resistor connected to VBIAS (100Ω differential).
4 5	4 5	BO- BO+	Output	Positive CML output channel B with internal 50Ω pull-up resistor connected to VBIAS (100Ω differential).
7	7	EN	Input	Chip Enable "High" provides normal operation. "Low" for power down mode. With internal 100KΩ pull-up resistor.
3, 13, 18, 19, Center Pad	Center Pad	GND	GND	Supply ground.
6,10, 16, 20	6, 10, 16, 20	V_{DD}	Power	3.3V supply voltage ± 10%
17	17	MODE	Input	MODE selects Enhanced Mode operation and pin function when high. When MODE is low, Standard Mode operation is selected. With internal 100KΩ pull-up resistor to V_{DD}. See Configuration tables for use information.

Configuration Table (Standard Mode)

EN	MODE	B_EM(1)	A_EM (1)	Output B Emphasis	Output A Emphasis	Input B Equalization @ f=1.5GHz	Input A Equalization @ f=1.5GHz
0	X	X	X	Disable	Disable	Disable	Disable
1	0	0	0	0dB	0dB	2.5dB	2.5dB
1	0	0	1	0dB	3.0dB	2.5dB	2.5dB
1	0	1	0	3.0dB	0dB	2.5dB	2.5dB
1	0	1	1	3.0dB	3.0dB	2.5dB	2.5dB

Note:

1. Refer to Standard Mode Implementation Diagram

Configuration Table (Enhanced Mode)

EN	MODE	x_EN#	x_EQ	Input X Equaliza-tion	x_EM	Output X Emphasis	Function
0	X	X	X	n/a	X	n/a	Chip Power Down
1	1	1	X	n/a	X	n/a	Chip enabled, Channel x disabled
1	1	0	0	2.5dB	1.1K to 15K resistor	Resistor Controlled, 6dB to 0dB (1)	Chip and channel enabled, low input equalization
1	1	0	1	6.5dB	1.1K to 15K resistor	Resistor Controlled, 6dB to 0dB (1)	Chip and channel enabled, high input equalization

Note:

1. Refer to Enhanced Mode Implementation Diagram

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....–65°C to +150°C
Supply Voltage to Ground Potential.....–0.5V to +4.6V
DC SIG Voltage .....–0.5V to V_{DD} +0.5V
Current Output ..... –25mA to +25mA
Power Dissipation Continuous 500mW
Operating Temperature .....0 to +70°C
ESD, Human Body Model.....–6kV to +6kV

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage		3.0		3.6	V
$P_{STANDBY}$	Supply Power, Standby	EN = 0			1.5	mW
P_{IDLE}	Supply Power, Idle	EN = 1, x_EN# = 0 $_{DIFFP-P} < V_{TH-SD}$		235		mW
P_{ACTIVE}	Supply Power, Active	EN = 1, x_EN# = 0 $_{DIFFP-P} \geq V_{TH-SD}$			440	mW
$I_{DD-STANDBY}$	Supply Current Standby	EN = 0			0.4	mA
$I_{DD-IDLE}$	Supply Current Idle	EN = 1, x_EN# = 0, $V_{RX-DIFFP-P} < V_{TH-SD}$		70		
$I_{DD-ACTIVE}$	Supply Current Active	EN = 1, x_EN# = 0, $V_{RX-DIFFP-P} \geq V_{TH-SD}$			120	
t_{PD}	Latency	From input to output		2.0		ns
CML Receiver Input						
Z_{RX-DC}	DC Input Impedance		40	50	60	Ω
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance		80	100	120	
$V_{RX-DIFFP-P}$	Differential Input Peak-to-peak Voltage		0.2		1.6	V
$V_{RX-CM-ACP}$	AC Peak Common Mode Input Voltage				150	mV
V_{TH-SD}	Signal detect Threshold	EN = 1, x_EN# = 0	50		200 (1)	mVppd

(continued)

Note:

Using Compliance test at 1.5Gbps and 3Gbps. Also using OOB (OOB is formed by ALIGNp primitive or D24.3) test patterns at 1.5Gbps. The ALIGN primitive (K28.5+D10.2+D27.3 = 0011111010+0101010101+0010011100). The D24.3 = 00110011001100110011

AC/DC Electrical Characteristics (CML Receiver Input continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
RL_{dd11_RX}	RX differential mode return loss	75MHz-300MHz 300MHz-600MHz 600MHz-1.2GHz 1.2GHz-2.4GHz 2.4GHz-3.0GHz 3.0 GHz-5.0GHz	18 14 10 8 3 1			dB
RL_{cc11_RX}	RX common mode return loss	150MHz – 300MHz 300MHZ – 600MHz 600MHz – 1.2GHz 1.2GHz – 2.4GHz 2.4GHz – 3.0GHz 3.0GHz – 5.0GHz	5 5 2 2 1 1			dB
RL_{dc11_RX}	RX impedance balance	150MHz – 300MHz 300MHz – 600MHz 600MHz – 1.2GHz 1.2GHz – 2.4GHz 2.4GHz – 3.0GHz 3.0GHz – 5.0GHz	30 30 20 10 4 4			dB
Equalization						
T_J	Total Jitter	Measured at 3Gbps/500			0.37	UI
D_J	Deterministic Jitter	Measured at 3Gbps/500			0.19	UI
CML Transmitter Output (100Ω differential)[1]						
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		80	100	120	Ω
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Output Voltage	$V_{TX-DIFFP-P} = 2 * \lvert V_{TX-D+} - V_{TX-D-} \rvert$	500		600	mV
V_{TX-C}	Common-Mode Voltage	$\lvert V_{TX-D+} + V_{TX-D-} \rvert /2$	1		1.8	V
t_F, t_R	Transition Time	20% to 80%(1)	50		150	ps
t_F-t_R	Mis-match Transition Time	3G only; HFTP, MFTP			20	%
V_{amp_bal}	TX amplitude imbalance	3G only; HFTP, MFTP			10	%
T_{skew}	TX differential skew	1.5G and 3G; HFTP, MFTP			20	ps
V_{cm_ac}	TX AC common mode voltage	3G only; MFTP			50	mVpp
V_{cmOOB}	OOB common mode delta voltage				50	mV
$V_{diffOOB}$	OOB differential delta voltage				25	mV
$V_{TX-Pre-Ratio-max}$	Max TX Pre-emphasis Level				6	dB

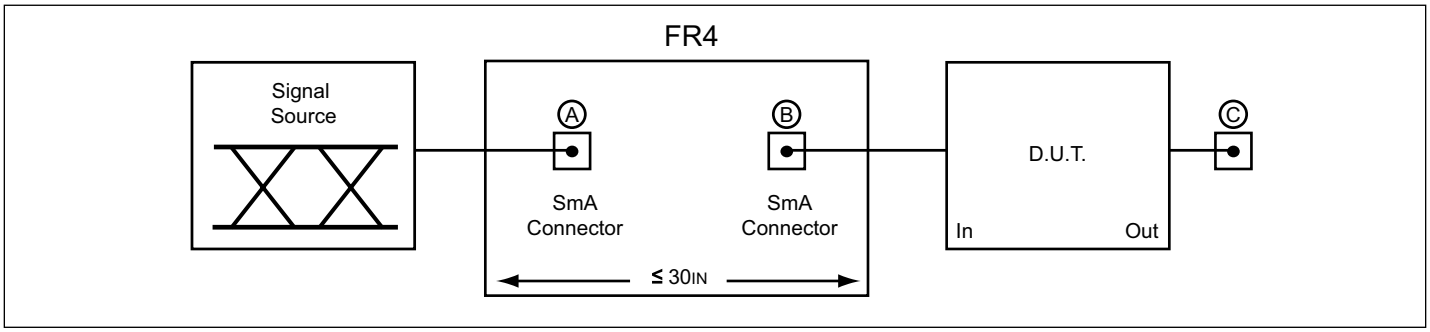
Note:

1. Recommended output coupling capacitor is 4.7nF to 12nF (on each output)

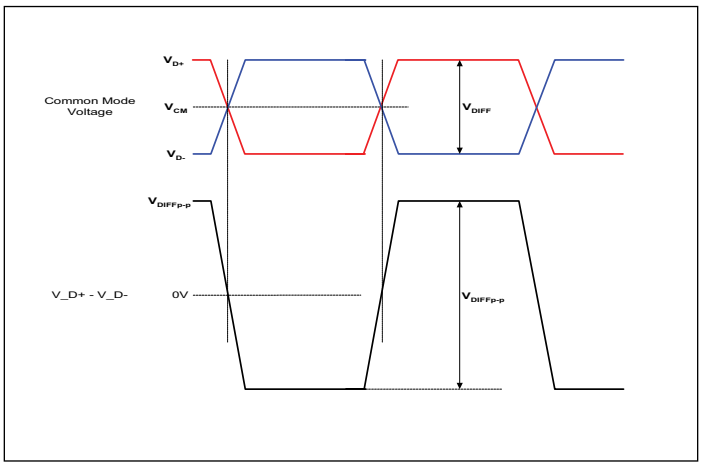
(continued)

AC/DC Electrical Characteristics (CML Transmitter Output continued)

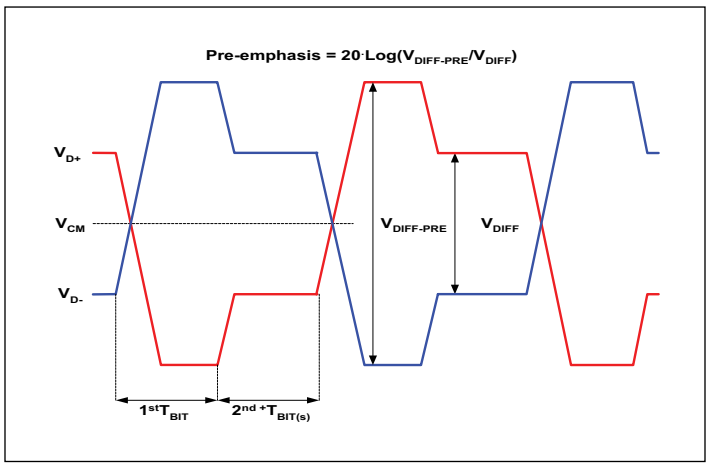
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
RL_{dd11_TX}	TX differential mode return loss	150MHz – 300MHz 300MHz – 600MHz 600MHz – 1.2GHz 1.2GHz – 2.4GHz 2.4GHz – 3.0GHz 3.0 GHz – 5.0GHz	14 8 6 6 3 1			dB
RL_{cc11_TX}	TX common mode return loss	150MHz – 300MHz 300MHz – 600MHz 600MHz – 1.2GHz 1.2GHz – 2.4GHz 2.4GHz – 3.0GHz 3.0 GHz – 5.0GHz	5 5 2 2 1 1			dB
RL_{dc11_TX}	TX impedance balance	150MHz – 300MHz 300MHz – 600MHz 600MHz – 1.2GHz 1.2GHz – 2.4GHz 2.4GHz – 3.0GHz 3.0 GHz – 5.0GHz	30 20 10 10 4 4			dB
LVCMOS Control Pins						
V_{IH}	Input High Voltage		0.65 × V_{DD}			V
V_{IL}	Input Low Voltage				0.35 × V_{DD}	
I_{IH}	Input High Current				100	µA
I_{IL}	Input Low Current				100	



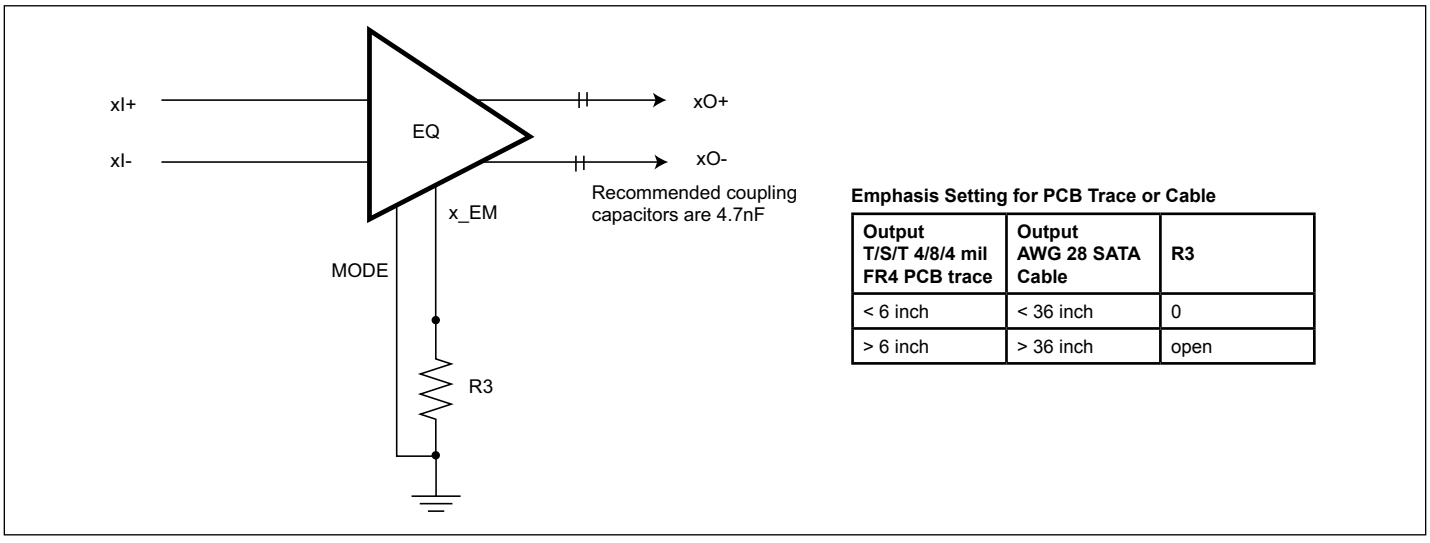
Test Condition Referenced in the Electrical Characteristic Table



Definition of Differential Voltage and Differential Voltage Peak-to-Peak



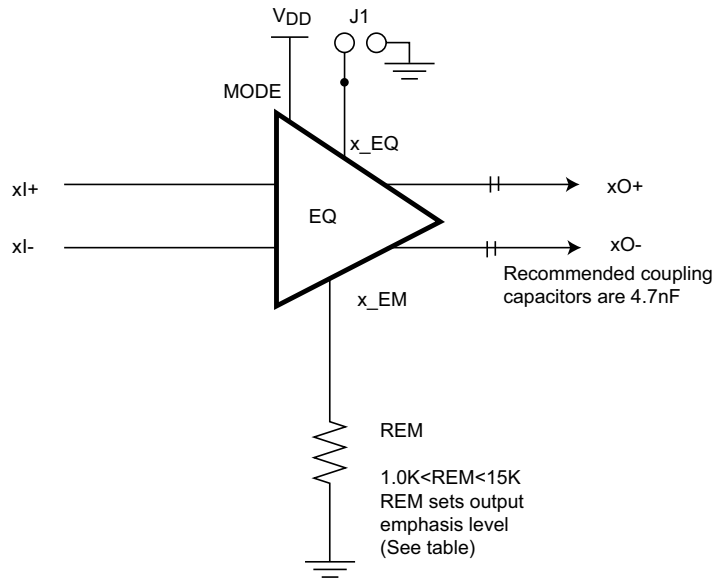
Definition of Pre-emphasis



Emphasis Setting for PCB Trace or Cable

Output T/S/T 4/8/4 mil FR4 PCB trace	Output AWG 28 SATA Cable	R3
< 6 inch	< 36 inch	0
> 6 inch	> 36 inch	open

Standard Mode Implementation Diagram



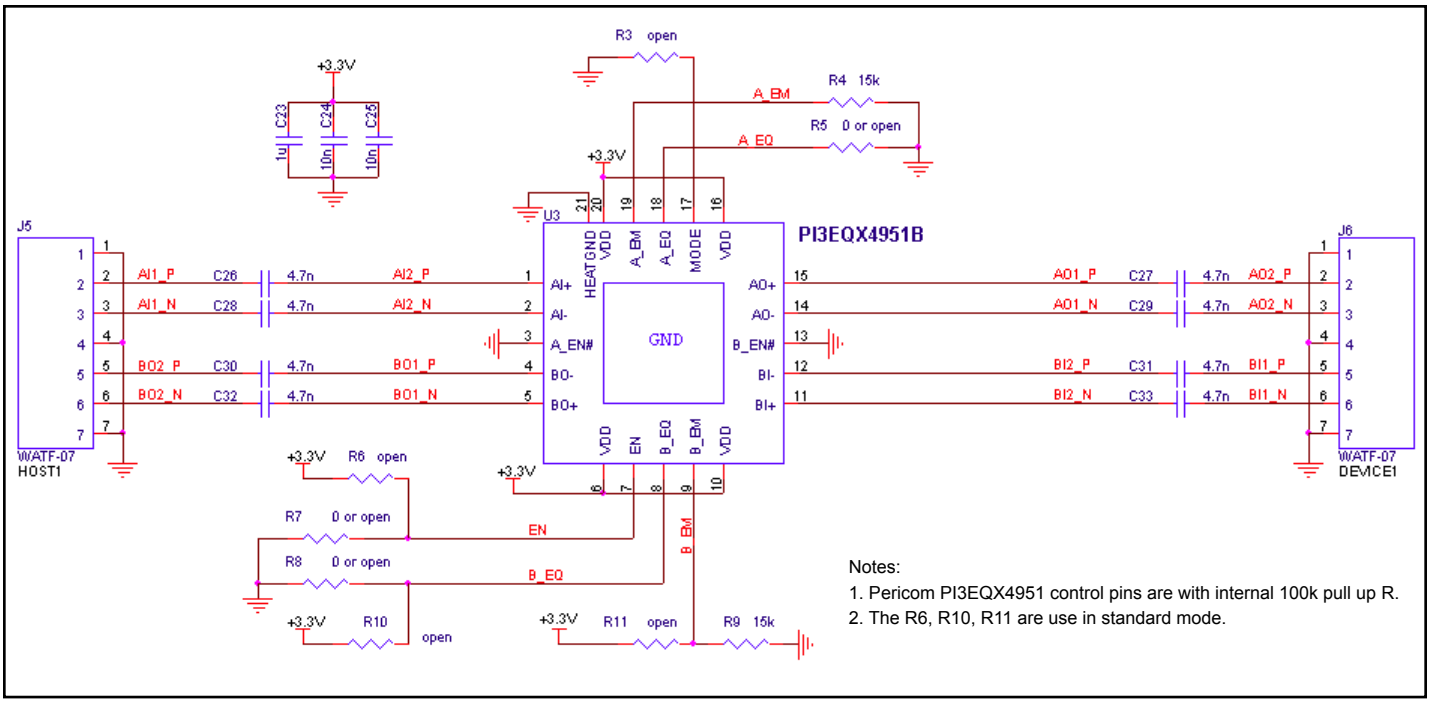
Equalization Setting for PCB Trace or Cable

Output T/S/T 4/8/4 mil FR4 PCB trace	Output AWG 28 SATA Cable	J1
< 6 inch	< 36 inch	0
> 6 inch	> 36 inch	open

REM Suggested Inital Values for PCB Trace or Cable

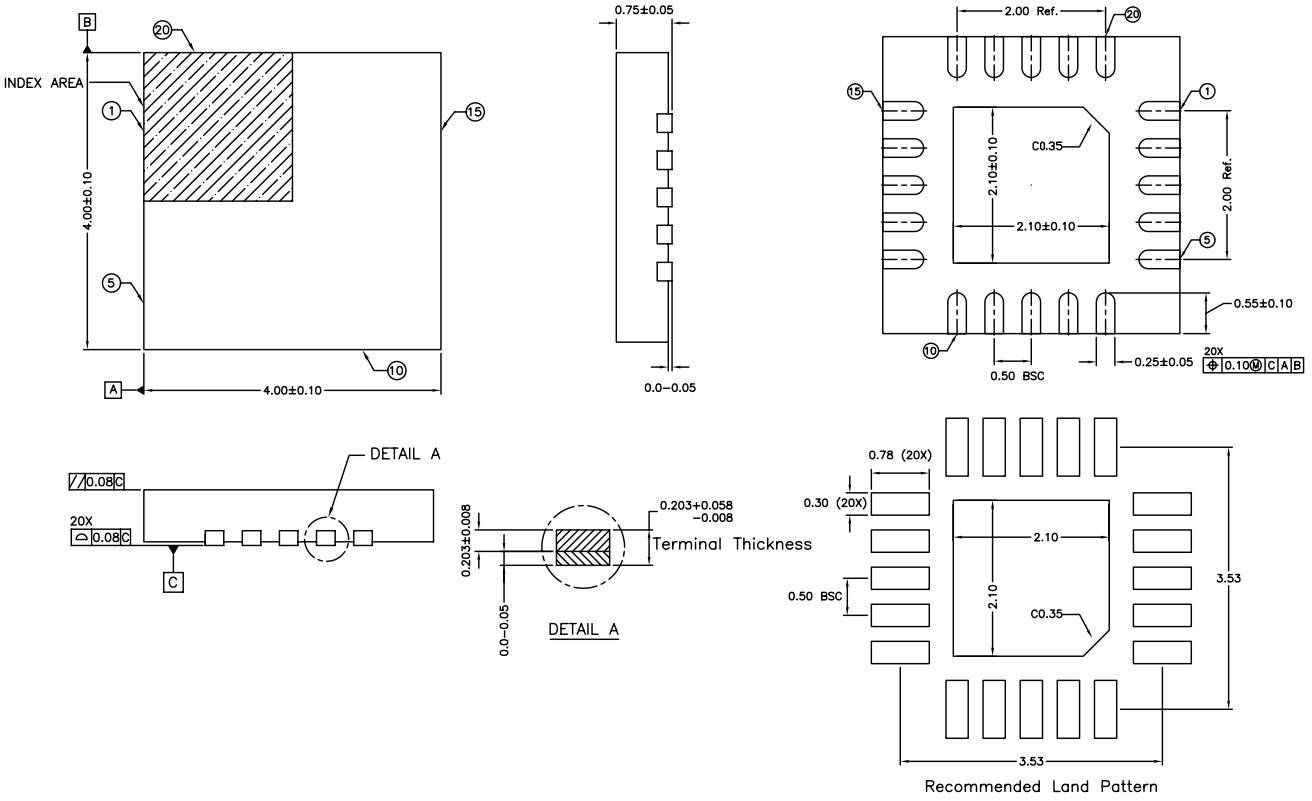
Output T/S/T 4/8/4 mil FR4 PCB trace	Output AWG 28 SATA Cable	Pre-emphasis dB	REM
< 3 inch	< 18 inch	0	15k
4 inch	30 inch	1.5dB	7.5k
6 inch	30 inch	2.0dB	6.2k
8 inch	40 inch	2.5dB	5.1k
12 inch	60 inch	3.5dB	3.3k
16 inch	48 inch	4.5dB	2.2k
24 inch	48 inch	6.0dB	1.1k

Enhanced Mode Implementation Diagram



Application Schematic

Packaging Mechanical: 20-contact TQFN (ZD)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.08 mm.
4. REFER JEDEC MO–220.

PERICOM Semiconductor Corporation — DATE: 09/11/08

DESCRIPTION: 20-Lead, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZD20

DOCUMENT CONTROL #: PD-2084 — REVISION: --

08-0456

Note: For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Number	Package Code	Package Description
PI3EQX4951BZDE	ZD	Pb-Free and Green 20-contact TQFN (4x4mm)

Notes:

- **Thermal characteristics can be found on the company web site at www.pericom.com/packaging/**
- **E = Pb-free and Green**
- **X suffix = Tape/Reel**