Ordering number : ENA0139

SANYO Semiconductors
DATA SHEET

LC87F40C8A

CMOS IC
Internal 128K-byte FROM (ROM/CGROM), 2048 byte RAM, 1024-byte CGRAM, and 704×10-bit CRT Display RAM

8-bit 1-chip Microcontroller

Overview

The SANYO LC87F40C8A is a closed caption TV controlling 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 71ns, integrates on a single chip a number of hardware features such as 128K-byte flash ROM (size-variable program ROM and CGROM), 2048-byte RAM, 1024-byte CGRAM, 704×10-bit CRT display RAM, sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters, two 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, a high-speed clock counter, a synchronous SIO interface (with automatic block transmission/reception capabilities), two channels of asynchronous/ synchronous SIO interface (bus mode selectable), a UART interface (full duplex), an 8-bit 8-channel AD converter, one 14-bit PWM channel, three 8-bit PWM channels, a closed caption data slicer, closed caption compatible OSD, a system clock frequency divider, ROM correction function, an on-chip debugger, and onboard programming facilities.

Features

■Flash ROM

128K bytes

- 95K- to 110K-byte program ROM (size variable)
- 16K- to 31K-byte character generator ROM (size variable)
- Runs on a 5V single source and permits onboard programming.
- Block erasable in 128 byte units.
- Permits 100 programming operations.

■Internal RAM

- General-purpose RAM: 2K bytes
- Character generator RAM: 1K bytes
- CRT display RAM: 704 × 10 bits
- ROM correction RAM: 256 bytes

* This product is licensed from Silicon Storage Technology, Inc. (USA), and manufactured and sold by SANYO Semiconductor Co., Ltd.

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

■Minimum Bus Cycle Time
- 71 ns (14.1MHz)

  Note: The bus cycle time here refers to the ROM read speed.

■Minimum Instruction Cycle Time
- 212 ns (14.1MHz)

■OSD
- Screen size : 36 characters × 16 lines
- Display RAM size : 704 words (1 word=10 bits)
  - Display area : 36 words × 16 lines
  - Control area : 8 words × 16 lines
- Font types : 16 × 32 font, 512 types (16 CGRAM fonts, including 4 fixed fonts)
  An arbitrary number of characters can be generated as 16 × 17 or 8 × 9 font characters.
- Display colors : 4096 colors
  Character text, background, borders, and full background can be displayed.
- Display mode specifiable on a line basis.
  Normal, 4-color pixel map, 16-color pixel map, and caption text modes
- Vertical display start line and horizontal display start position specifiable on a line basis.
- Shutter function (specifying the display start or stop line) and scroll functions specifiable on a line basis.
- Horizontal character spacing (9 to 16 dots)*1 and vertical character spacing (1 to 32 dots) specifiable on a line basis.
- Character size selectable from 16 character sizes on a line basis*1.

  (Horizontal×Vertical) = (1×1), (1×2), (2×1), (2×2), (2×4)
  (4×2), (4×4), (4×8), (1.5×1), (1.5×2)
  (3×1), (3×2), (3×4), (6×2), (6×4), (6×8)
- Cursor display function (4/16 pixel colors)
- Multilayer display
- Full screen display area specifiable.
- OSD clock selectable (normal speed mode/high speed mode/external input)
- Interlace/progressive scan selectable

*1: The supported range varies depending on the active display mode. Refer to the user's guide for details.

■Data Slicer Function (closed caption format)
- Extracts closed caption data and XDS data.
- NTSC/PAL selectable and line specifiable.

■Ports
- Normal withstand voltage I/O ports

  Ports whose I/O direction can be designated in 1-bit units 41 (P1n, P2n, P3n, P70 to P73, P8n, PC0 to PC4)

  Ports whose I/O direction can be designated in 4-bit units 8 (P0n)

■Timers
- Timer 0: 16-bit timer/counter with a capture register.
  - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels
  - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
  - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  - Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
  - Mode 0: 8-bit timer with an 8-bit prescaler + with an 8-bit prescaler 8-bit timer/counter
  - Mode 1: 6-bit timer/counter with an 8-bit prescaler
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Base timer

  1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts programmable in 5 different time schemes

■High-speed Clock Counter
1) Can count clocks with a maximum clock rate of 28.2MHz (at a main clock of 14.1MHz).
2) Can generate output real-time.

■SIO
- SIO0: 8-bit synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
  3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1 bit units, suspension and resumption of data transmission possible in 1 byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface (bus mode 1 system)
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)
- SIO6: 8-bit asynchronous/synchronous serial interface (bus mode 2 system)
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■UART
- Full duplex
- 7/8/9 data bits selectable
- 1 stop bit
- Built-in baudrate generator

■AD Converter: 8 bits × 8 channels

■PWM: 14-bit PWM × 1 channel
8-bit PWM × 3 channels

■Remote Control Receiver Circuit (sharing with P73, INT3, and T0IN pins)
- Noise rejection function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)

■Watchdog Timer
- External RC watchdog timer
- Interrupt and reset signals selectable

■High-speed Multiplication/Division Instructions
- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Interrupts

- 21 sources, 10 vector addresses

1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.

2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L
4	0001BH	H or L	INT3/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit/data slicer/SIO6
9	00043H	H or L	ADC/vertical sync (VS)/scan line
10	0004BH	H or L	Port 0/T4/T5

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 1024 levels maximum (the stack is allocated in RAM.)

■Oscillation Circuits

- RC oscillation circuit (internal) : For system clock
- VCO oscillation circuit (internal) : For system clock generation and CRT display
- Crystal oscillation circuit : For low-speed system clock, base timer, and PLL reference

■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 212ns, 424ns, 848ns, 1.7μs, 3.4μs, 6.8μs, 13.6μs, 27.1μs, and 54.3μs (at a main clock rate of 14.1MHz).

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) Canceled by a system reset or occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The VCO, RC, and crystal oscillators automatically stop operation.
  2) There are three ways of resetting the HOLD mode.
     (1) Setting the reset pin to the lower level.
     (2) Setting at least one of the INT0, INT1, and INT2 pins to the specified level
     (3) Having an interrupt source established at port 0

■ROM Correction Function

- Executes the correction program on detection of a match with the program counter value.
- Correction program area size: 256 bytes (4 vector addresses)

■Onchip Debugger

- Supports software debugging with the IC mounted on the target board

■Package Form

- QIP64E(14×14): Lead-free type
- DIP64S(600mil): Lead-free type

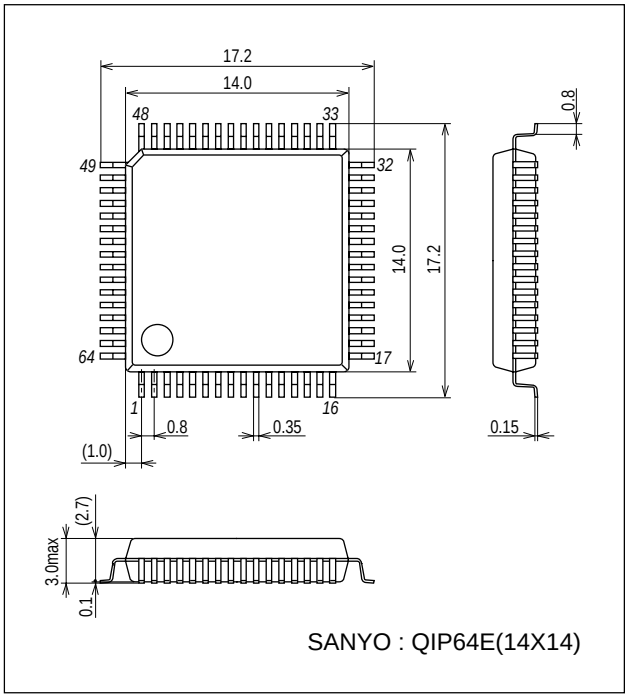
■Development Tools

- Onchip debugger interface board: TCB87 (Type B)

Package Dimensions

unit : mm (typ)

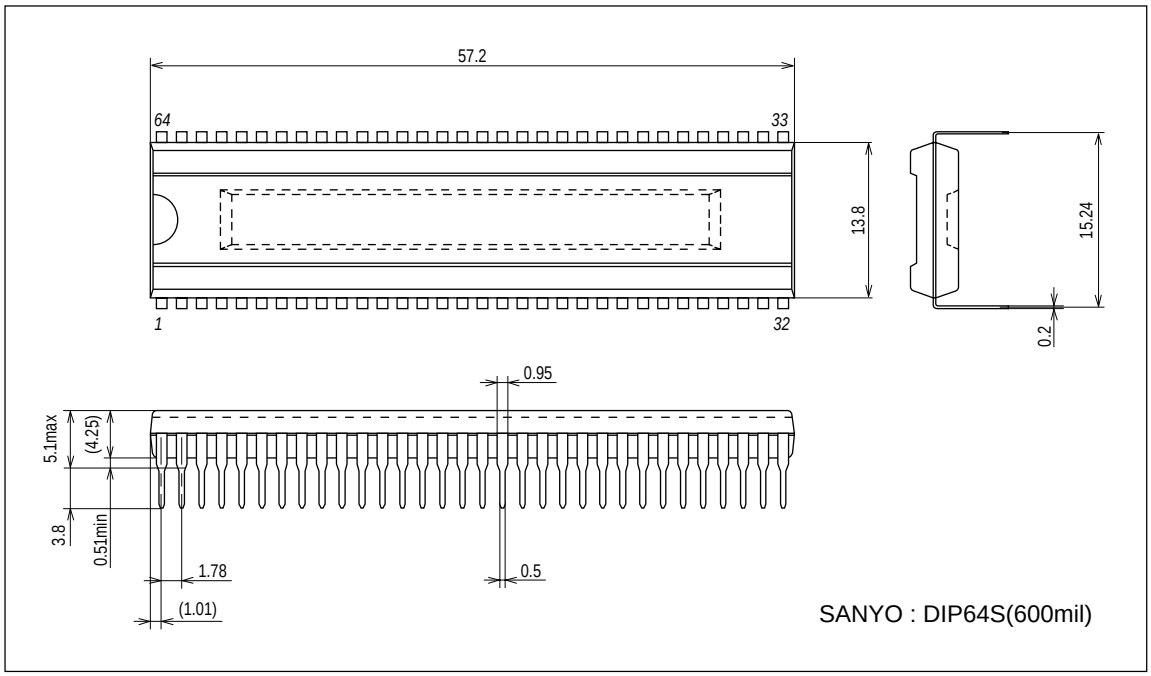
3159A



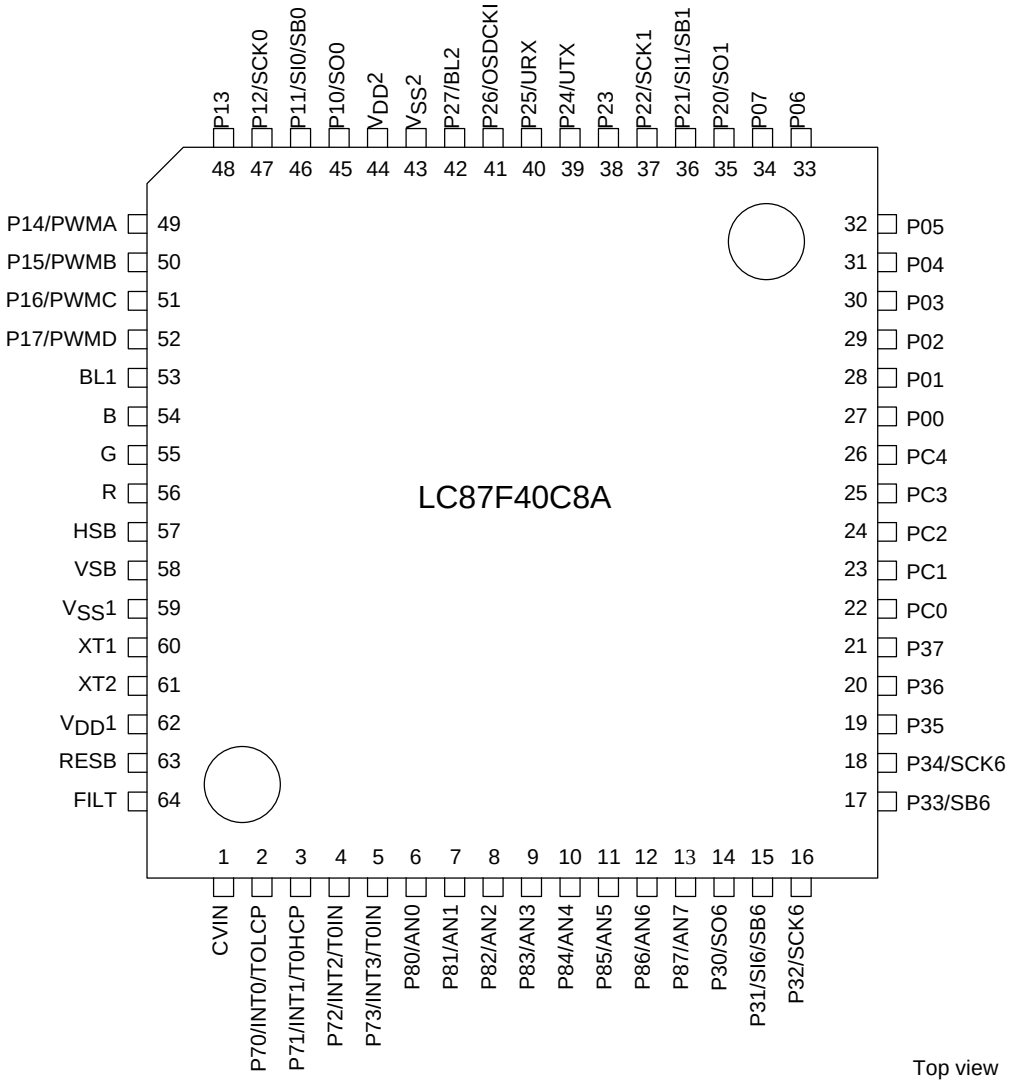
Package Dimensions

unit : mm (typ)

3300

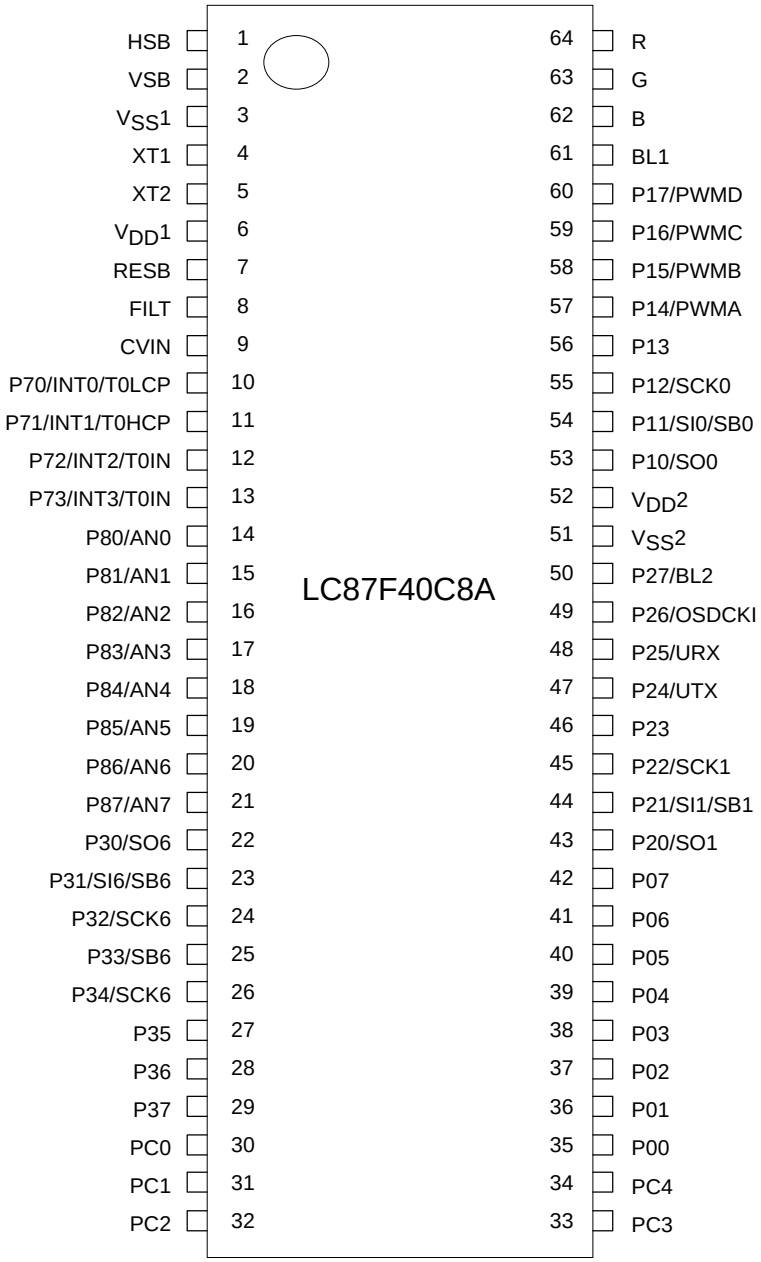


Pin Assignments



Top view

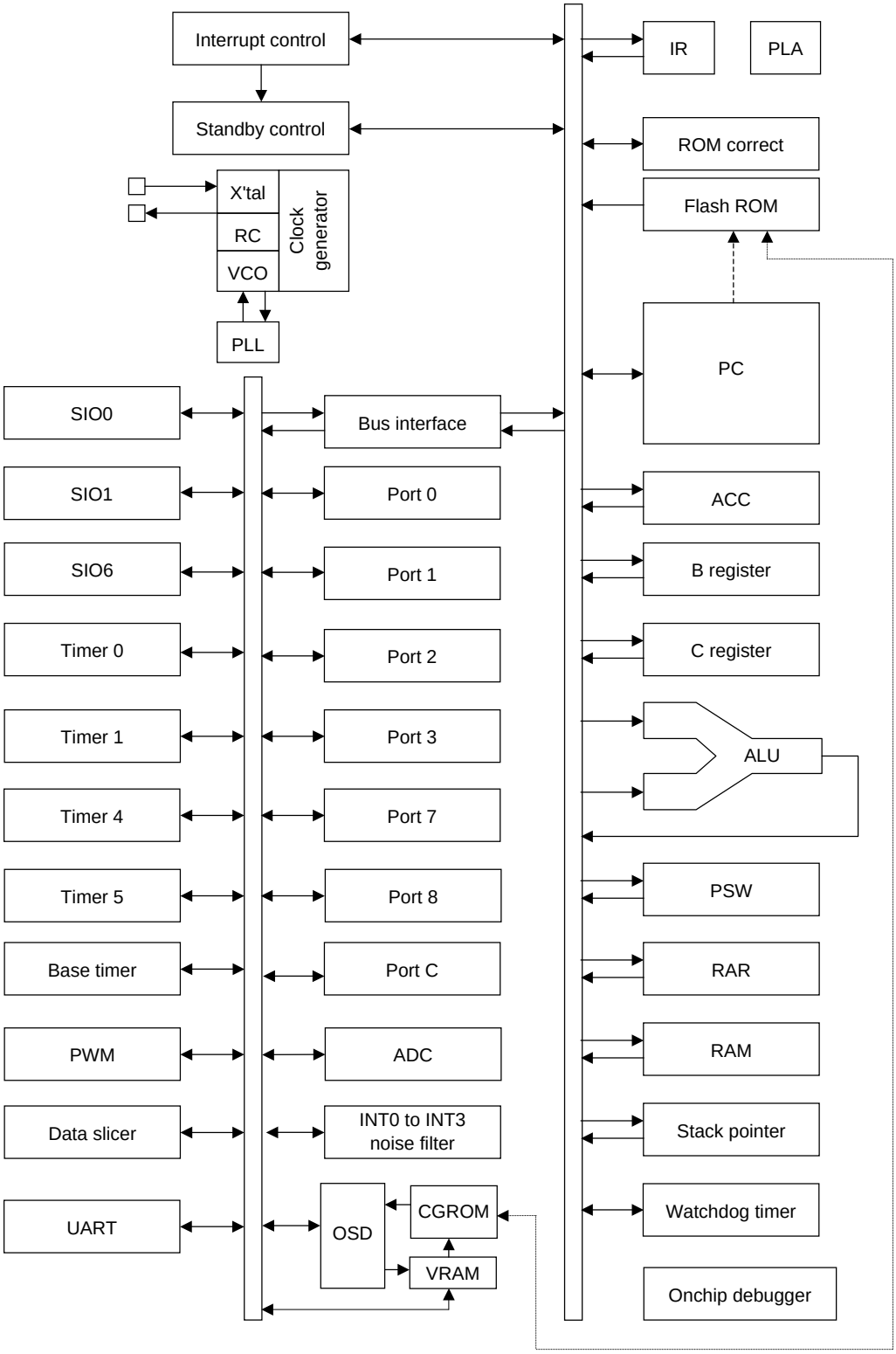
SANYO : QIP64E(14×14) “Lead-free Type”



Top view

SANYO : DIP64S (600mil) “Lead-free Type”

System Block Diagram



Pin Description

Pin Name	I/O	Description	Option
$V_{SS}1$ $V_{SS}2$	-	- power supply pin	No
$V_{DD}1$ $V_{DD}2$	-	+ power supply pin	No
Port 0 P00 to P07	I/O	• 8-bit I/O port • I/O specifiable in 4-bit units • Pull-up resistors can be turned on and off in 4-bit units. • HOLD reset input • Port 0 interrupt input	Yes
Port 1 P10 to P17	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions P10: SIO0 data output P11: SIO0 data input/bus I/O P12: SIO0 clock I/O P14: PWMA output P15: PWMB output P16: PWMC output P17: PWMD output	Yes
Port 2 P20 to P27	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions P20: SIO1 data output P21: SIO1 data input/bus I/O P22: SIO1 clock I/O P24: UART transmit P25: UART receive P26: External OSD clock input P27: Fast blanking 2 control signal output	Yes
Port 3 P30 to P37	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions P30: SIO6 data output P31: SIO6 data input/bus I/O P32: SIO6 clock I/O P33: SIO6 bus I/O P34: SIO6 clock I/O Onchip debugger pins: DBGP0 to DBGP2 (P35 to P37)	Yes

Continued on next page.

Continued from preceding page.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Shared pins
P70: INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output
P71: INT1 input/HOLD reset input/timer 0H capture input
P72: INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input
P73: INT3 input (with noise filter input)/timer 0 event input/timer 0H capture input
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H Level</th><th>L Level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>Port 8
P80 to P87</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Shared pins
AD converter input: AN0 (P80) to AN7 (P87)</td><td>No</td></tr>
<tr><td>Port C
PC0 to PC4</td><td>I/O</td><td>• 5-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.</td><td>Yes</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>Input</td><td>Reset pin</td><td>No</td></tr>
<tr><td>XT1</td><td>Input</td><td>• 32.768kHz crystal oscillator input pin</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>• 32.768kHz crystal oscillator output pin</td><td>No</td></tr>
<tr><td>FILT</td><td>Output</td><td>• Internal PL filter pin</td><td>No</td></tr>
<tr><td>CVIN</td><td>Input</td><td>• Video input pin</td><td>No</td></tr>
<tr><td>VS</td><td>Input</td><td>• Vertical sync input pin</td><td>No</td></tr>
<tr><td>HS</td><td>Input</td><td>• Horizontal sync input pin</td><td>No</td></tr>
<tr><td>R</td><td>Output</td><td>• Red (R) RGB video output pin</td><td>No</td></tr>
<tr><td>G</td><td>Output</td><td>• Green (G) RGB video output pin</td><td>No</td></tr>
<tr><td>B</td><td>Output</td><td>• Blue (B) RGB video output pin</td><td>No</td></tr>
<tr><td>BL1</td><td>Output</td><td>• Fast blanking 1 control output pin</td><td>No</td></tr>
</table>

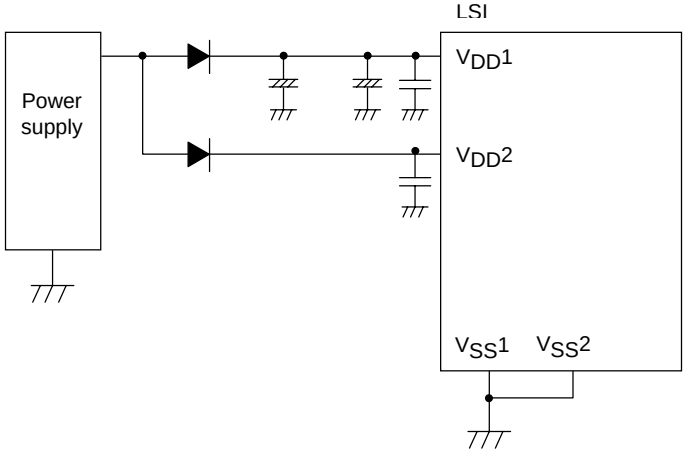
Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17 P20 to P27 P30 to P37	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P87	-	No	Nch-open drain	No
PC0 to PC4	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable

Note 1: Programmable pull-up resistors for port 0 are controlled in 4 bit units (P00 to 03, P04 to 07).

*1 Connect the IC as shown below to minimize the noise input to the $V_{DD}1$ pin.
Be sure to electrically short the $V_{SS}1$ and $V_{SS}2$ pins**.**



On-board writing system

The LC87F40C8A has the On-board writing system. The program is renewable by using SANYO Flash On-board System after the LSI has been installed on the application board.
This system has to connect the 6 pins (V_{DD}, V_{SS}, $\overline{RES}$, communication pins) with the interface board of SANYO Flash On-board System.
It is necessary that the pins to be used for the rewriting system should be able to be separated from the application board properly.

- The loader program must be written into the ROM to use On-board writing system. The loader program should be written into the ROM before the LSI has been installed on the board by the general purpose PROM programs. When the option setting selects the this system to use, the loader program automatically links on the user program linking.

Please ask to our sales persons before using On-board writing system.

Method of how to rewrite it in FLASH programmer/ SANYO FLASH writing tool (SFWS)

When reading or writing data to the LC87F40C8A, FLASH programmer of our recommendation or SANYO FLASH writing tool (SFWS) is used. In both cases, exclusive conversion board (W87F40C8D, W87F40C8Q) is needed.

(1) FLASH programmer of our recommendation
Single word write

Manufacture	Name of device	version	applicable device (code)	Data protection setting after write operation
Flash Support Group co. (the former Ando Electric)	AF9708	Rev02.35	SANYO LC87F40C8A (3B21C)	Protected

Write multiple words

Manufacture	Name of device	Version	applicable device (code)	Data protection setting after write operation
Flash Support Group co. (the former Ando Electric)	AF9723 + AF9833	Rev01.83	SANYO LC87F40C8A (3B21C)	Protected

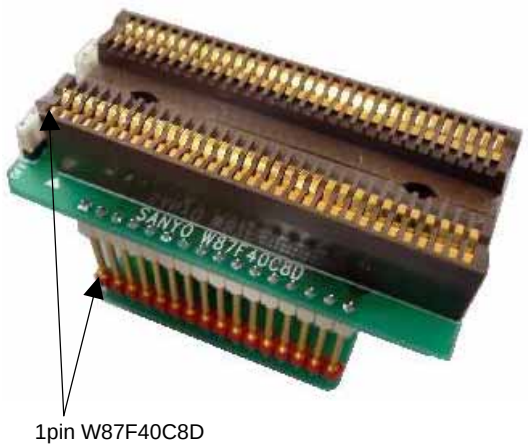
- The LC87F40C8A does not support a silicon signature feature.
  Do not use the feature (automatic device type selection) when programming this device.
- To avoid erasing the program, confirm the setting of the protection for activating the written program before using.
- It can't be written with device code 29EE010

(2) SANYO FLASH writing tool (SFWS)
PC is connected with writer unit (SKK) by USB cable and it uses it.

(3) Exclusive writing conversion board
- W87F40C8D: DIP64S purpose
- W87F40C8Q: QIP64E purpose

When using the conversion board, all of the jumper SW must be set to the OFF position.
If set to the ON position, read/write operations will not perform correctly.

Pin 1 of the conversion board should be located as indicated below.
W87F40C8D: when viewing from the edge closest to jumper SW, pin 1 is located on the lower right of both the chip and conversion board.
W87F40C8Q: when viewing from the edge closest to jumper SW, pin 1 of the chip is located on the upper right while pin 1 of the conversion board is located on the lower right.



Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$	$V_{DD}1=V_{DD}2$		-0.3		+6.5	V
Input voltage		V_I(1)	XT1, $\overline{RES}$, HS, VS, CVIN			-0.3		V_{DD}+0.3	V
Output voltage		VO(1)	XT2, BL1, R, G, B FILT			-0.3		V_{DD}+0.3	V
Input/output voltage		V_{IO}(1)	Ports 0, 1, 2, 3 Ports 7, 8 Port C			-0.3		V_{DD}+0.3	V
High level output current	Peak output current (Note 1-1)	IOPH(1)	Ports 0, 1, 2, 3, C BL	CMOS output select Per 1 applicable pin		-10			mA
		IOPH(2)	Ports 71 to 73	Per 1 applicable pin		-5			mA
		IOPH(3)	R, G, B	OSD is digital mode Per 1 applicable pin		-10			mA
	Total output current	ΣIOAH(1)	Port 7	Total of all applicable pins		-25			mA
		ΣIOAH(2)	Ports 0, 2, 3, C	Total of all applicable pins		-25			mA
		ΣIOAH(3)	Ports 1 R, G, B, BL	Total of all applicable pins		-25			mA
Low level output current	Peak output current (Note 1-1)	IOPL(1)	Ports 0, 1, 2, 3, C BL	Per 1 applicable pin				20	mA
		IOPL(2)	Ports 7, 8	Per 1 applicable pin				10	mA
		IOPL(3)	R, G, B	OSD is digital mode Per 1 applicable pin				20	mA
	Total output current	ΣIOAL(1)	Ports 7, 8	Total of all applicable pins				20	mA
		ΣIOAL(2)	Ports 0, 2, 3, C	Total of all applicable pins				45	mA
		ΣIOAL(3)	Ports 1 R, G, B, BL	Total of all applicable pins				45	mA
Allowable power dissipation		Pd max	QIP64E(14×14)	Ta=-10 to +70°C				390	mW
			DIP64S(600mil)					880	mW
Operating ambient temperature		Topr				-10		+70	°C
Storage ambient temperature		Tstg				-55		+125	°C

Note 1-1: The average current per applicable pit must not exceed 10mA.

Allowable Operating Conditions at Ta = -10°C to +70°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification				
					V_{DD}[V]	min	typ	max	unit
Operating supply voltage	$V_{DD}(1)$	$V_{DD}1=V_{DD}2$	0.211µs≤tCYC≤200µs			4.5		5.5	V
Memory sustaining supply voltage	VHD	$V_{DD}1=V_{DD}2$	RAM and register contents sustained in HOLD mode			2.0		5.5	
High level input voltage	$V_{IH}(1)$	Ports 0, 1, 2, 3 P71 to P73, 8, C P70 port input/ interrupt side HS, VS			4.5 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	Port 70 watchdog timer side			4.5 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(3)$	XT1, $\overline{RES}$			4.5 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 0, 1, 2, 3 P71 to P73, 8, C P70 port input/ interrupt side HS, VS			4.5 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
	$V_{IL}(2)$	Port 70 watchdog timer side			4.5 to 5.5	V_{SS}		$0.15V_{DD}$ +0.4	
	$V_{IL}(3)$	XT1, $\overline{RES}$			4.5 to 5.5	V_{SS}		$0.25V_{DD}$	
CVIN input amplitude	VCVIN	CVIN			5.0	1Vp-p -3dB	1Vp-p	1Vp-p +3dB	Vp-p
Instruction cycle time	tcyc(1) (Note 2-1)		All functions		4.5 to 5.5	0.211	0.212	0.213	µs
	tcyc(2) (Note 2-1)		Except for OSD and data slicer functions		4.5 to 5.5	0.211		200	µs
External OSD clock frequency	FEXOS(1)	P26/OSDCKI	DUTY50±5% of external OSD clock (Note 2-3)	SCON1=0	4.5 to 5.5	14.28		15.44	MHz
	FEXOS(2)			SCON1=1		28.56		30.88	
Oscillation frequency range (Note 2-2)	FmVCO1		Internal VCO1 oscillator		4.5 to 5.5	14.08	14.15	14.22	MHz
	FmVCO2		Internal VCO2 Oscillator (Note 2-3)	CKSEL0=0	4.5 to 5.5	14.28	14.75	15.44	
				CKSEL0=1		28.56	29.5	30.88	
	FmRC		Internal RC oscillator		4.5 to 5.5	0.3	1.0	2.0	
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation mode See Fig. 1.		4.5 to 5.5		32.768		kHz

Note 2-1: Relationship between tCYC and oscillation frequency is 3/FmVCO1 at a division ratio of 1/1 and 6/FmVCO1 at a division ratio of 1/2.

Note 2-2: See Table 1 for the oscillation constants

Note 2-3: SCAN1 is Hsync frequency switch bit. CKSEL0 is OSD clock frequency switch bit. (Refer to the LC874000 user's manual for details.)

Electrical Characteristics at Ta = -10°C to +70°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 2, 3 Ports 7, 8 Port C	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (including output Tr's off leakage current)	4.5 to 5.5			1	µA
	$I_{IH}(2)$	$\overline{RES}$, HS, VS	$V_{IN}=V_{DD}$	4.5 to 5.5			1	
Low level input current	$I_{IL}(1)$	Ports 0, 1, 2, 3 Ports 7, 8 Port C	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (including output Tr's off leakage current)	4.5 to 5.5	-1			
	$I_{IL}(2)$	$\overline{RES}$, HS, VS	$V_{IN}=V_{SS}$	4.5 to 5.5	-1			
High level output voltage	$V_{OH}(1)$	Ports 0, 1, 2, 3, 8 Port C	I_{OH}=-1.0mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$	P71 to P73	I_{OH}=-0.4mA	4.5 to 5.5	V_{DD}-1			
	$V_{OH}(3)$	R, G, B	I_{OH}=-5mA	4.5 to 5.5	V_{DD}-1			
	$V_{OH}(4)$	BL1, P27/BL2	I_{OH}=-5mA When BL2 is output	4.5 to 5.5	V_{DD}-1			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1, 2, 3, 8 Port C	I_{OL}=10mA	4.5 to 5.5			1.5	
			I_{OL}=1.6mA	4.5 to 5.5			0.4	
	$V_{OL}(2)$	Port 7	I_{OL}=1mA	4.5 to 5.5			0.4	
	$V_{OL}(3)$	R, G, B	I_{OL}=5mA	4.5 to 5.5			0.4	
	$V_{OL}(4)$	BL1, P27/BL2	I_{OL}=5mA When BL2 is output	4.5 to 5.5			0.4	
Pull-up resistance	Rpu	Ports 0, 1, 2, 3, 7 Ports 8, C	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	40	70	kΩ
Hysteresis voltage	VHYS	$\overline{RES}$ Ports 1, 2, 3, 7 HS, VS		4.5 to 5.5		0.35		V
Bus terminal short circuit resistance for internal communication	RBS	• P31, P33 • P32, P34				130	300	Ω
Pin capacitance	CP	All pins	For pins other than that under test: $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	4.5 to 5.5			10	pF

Serial I/O Characteristics at Ta = -10°C to +70°C, $V_{SS}1 = V_{SS}2 = 0V$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Period	tSCK(1)	SCK0(P12)	See Fig. 5.	4.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1a)		• Continuous data transmission/ reception mode • OSD inactive • See Fig. 5. • (Note4-1-2)		4			
			tSCKHA(1b)		• Continuous data transmission/ reception mode • OSD active • See Fig. 5. • (Note4-1-2)		6			
	Output clock	Period	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 5.	4.5 to 5.5	4/3			tCYC
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2a)		• Continuous data transmission/ reception mode • OSD inactive • See Fig. 5.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
			tSCKHA(2b)		• Continuous data transmission/ reception mode • OSD active • See Fig. 5.		tSCKH(2) +2tCYC		tSCKH(2) +(16/3) tCYC	
Serial input	Data setup time		tsDI(1)	SI0(P11), SB0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 5.	4.5 to 5.5	0.03			µs
	Data hold time		thDI(1)				0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11),	• Continuous data transmission/ reception mode • (Note4-1-3)	4.5 to 5.5			(1/3)tCYC +0.05	
			tdD0(2)		• Synchronous 8-bit mode • (Note4-1-3)				1tCYC +0.05	
	Output clock		tdD0(3)		(Note4-1-3)				(1/3)tCYC +0.05	

Note4-1-1: This standard value is a theory value. Be sure to ensure the margin according to busy condition.

Note4-1-2: When using the serial clock in continuous data transmission/reception mode, the time to the first falling edge of the serial clock after it sets SIORUN in “H” state is more extended than tSCLKHA.

Note4-1-3: It is defined for the falling edge of SIOCLK. In open drain output, it is defined as the time to start the output change. See Fig. 5.

2. SIO1, 6 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK(3)	SCK1(P22), SCK6(P32, P34)	See Fig. 5.	4.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Period	tSCK(4)	SCK1(P22), SCK6(P32, P34)	• CMOS output selected • See Fig. 5.	4.5 to 5.5	2			
		Low level pulse width	tSCKL(4)				1/2			tSCK
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SI1(P21), SB1(P21), SI6(P31), SB6(P31, P33),	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 5.	4.5 to 5.5	0.03			µs
	Data hold time		thDI(2)				0.03			
Serial output	Output delay time		tdD0(4)	SO1(P20), SB1(P21), SO6(P30), SB6(P31, P34)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 5.	4.5 to 5.5			1/3tCYC +0.05	

Note4-2-1: This standard value is a theory value. Be sure to ensure the margin according to busy condition.

Pulse Input Conditions at Ta = -10°C to +70°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72),	• Interrupt source flag can be set. • Event inputs for timers 0 and 1 are enabled.	4.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	4.5 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	4.5 to 5.5	256			
	tPIL(5)	$\overline{RES}$	Resetting is enabled.	4.5 to 5.5	200			µs
	tPIH(6) tPIL(6)	$\overline{HS}$, $\overline{VS}$	• Display position controllable (Note) • The active edge of $\overline{HS}$ and $\overline{VS}$ must be apart at least 1 tCYC. • See Fig. 7.	4.5 to 5.5	1			
Falling time	tTHL	$\overline{HS}$	See Fig. 7. (Note 5-1)	4.5 to 5.5			100	ns
External OSD clock input frequency	tOSCKI	OSDCKI(P26)	See Fig. 8.	4.5 to 5.5	10			ns

Note 5-1: When the falling edge of $\overline{HS}$ is affected by the noise, the start position of OSD can slip off. Note that the signal lines with rapid state change or with large current should be allocated away from $\overline{HS}$ line.

AD Converter Characteristics at Ta = -10°C to +70°C, $V_{SS}1 = V_{SS}2 = 0V$

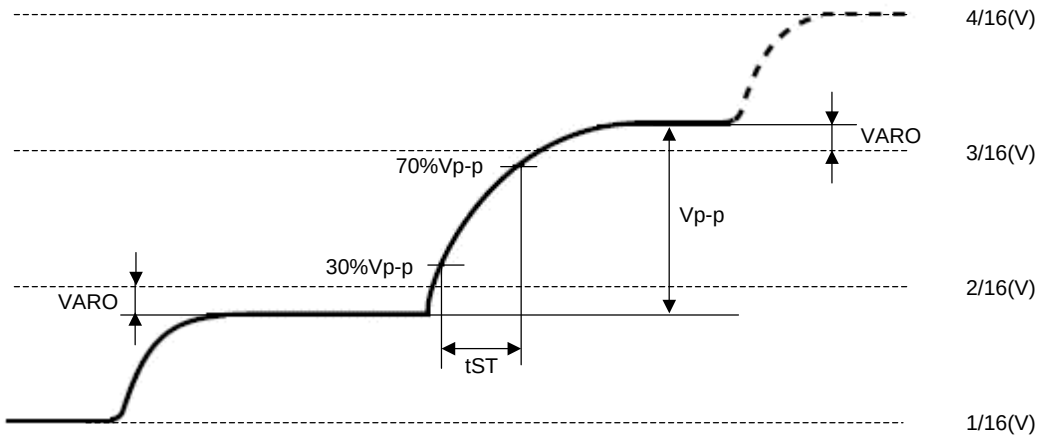
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN7(P87)		4.5 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	4.5 to 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time=32× tCYC (when ADCR2=0) (Note 6-2)	4.5 to 5.5	13.50 (tCYC= 0.422µs)		97.92 (tCYC= 3.06µs)	µs
			AD conversion time=64× tCYC (when ADCR2=1) (Note 6-2)	4.5 to 5.5	13.50 (tCYC= 0.211µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			4.5 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	4.5 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	4.5 to 5.5	-1			

Note 6-1: The quantization error (±1/2LSB) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the time the complete digital value corresponding to the analog input value is loaded in the required register.

Analog mode RGB Characteristics at Ta = -10°C to +70°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification			
				min	typ	max	unit
Output resistance		R, G, B	V_{DD}=5.0V			2.5	kΩ
Analog output deflection	VARO	R, G, B	V_{DD}=5.0V			20	%
Time seting	tST	R, G, B	70%DC level 10pf load			50	ns



Consumption Current Characteristics at Ta = -10°C to +70°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	Max	unit
Normal mode current drain (Note 7-1)	IDDOP(1)	$V_{DD}1$ =$V_{DD}2$	• FmX'tal=32.768kHz crystal oscillation mode • System clock set to main clock VCO • OSD VCO active • Internal RC oscillator inactive • 1/1 frequency division ratio • OSD is analog mode • DSL active	4.5 to 5.5		36	58	mA
	IDDOP(2)		• FmX'tal=32.768kHz crystal oscillation mode • System clock set to main clock VCO • OSD VCO active • Internal RC oscillator inactive • 1/1 frequency division ratio • OSD is digital mode • DSL active	4.5 to 5.5		28	47	mA
	IDDOP(3)		• FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz • Main clock and OSD VCOs inactive • Internal RC oscillator inactive • 1/2 frequency division ratio	4.5 to 5.5		100	300	µA
HALT mode current drain (Note 7-1)	IDDHALT(1)		HALT mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to main clock VCO • OSD VCO active • Internal RC oscillator inactive • 1/1 frequency division ratio	4.5 to 5.5		7	11	mA
	IDDHALT(2)		HALT mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillator • 1/1 frequency division ratio	4.5 to 5.5		600	1600	µA
	IDDHALT(3)		HALT mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz • Main and OSD VCOs inactive • Internal RC oscillator inactive • 1/2 frequency division ratio	4.5 to 5.5		75	200	
HOLD mode current drain	IDDHOLD	$V_{DD}1$	HOLD mode • All oscillators inactive	4.5 to 5.5		0.05	20	µA

Note 7-1: The current drain value includes none of the currents that flow into the output transistors and internal pull-up resistors.

F-ROM Programming Characteristics Ta = +10 to +55°C, $V_{SS}1 = V_{SS}2 = 0V$

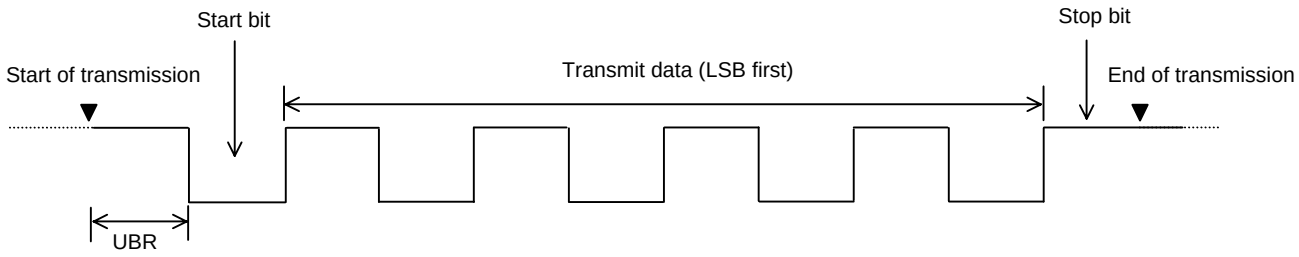
Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• 128-byte programming • Erasing current included	4.5 to 5.5		25		mA
Programming time	tFW(1)		• 128-byte programming • Erasing current included • Time for setting up 128-byte data is excluded.	4.5 to 5.5		22.5		ms

UART (Full Duplex) Operating Conditions at Ta=-10 to +70°C, $V_{SS}1=V_{SS}2=0V$

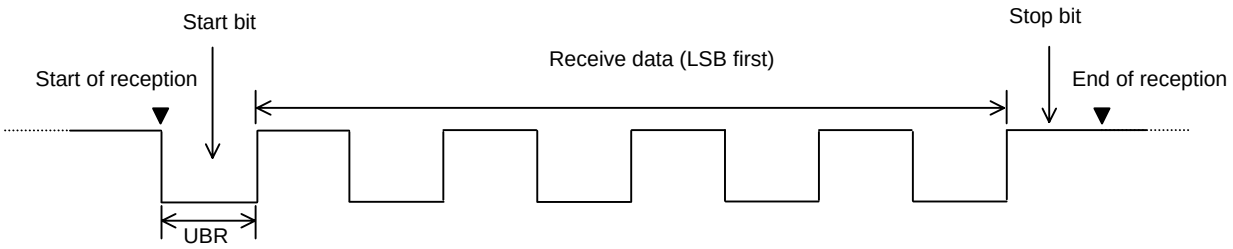
Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR	P24, P25		4.5 to 5.5	16/3		8192/3	tCYC

Data length: 7/8/9 bits (LSB first)
Stop bits: 1 bit
Parity bits: None

Example of Continuous 8-bit Data Reception Mode Processing (First Transmit Data=55H)



Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data=55H)



Recommended Oscillation Circuit and Sample Characteristics

The sample oscillation circuit characteristics in the table below is based on the following conditions:

- Recommended circuit parameters are verified by an oscillator manufacturer using a Sanyo provided oscillation evaluation board.
- Sample characteristics are the result of the evaluation with the recommended circuit parameters connected externally.

Table 1. Recommended oscillation circuit and sample characteristics (Ta = -10 to +70°C)

Frequency	Manufacturer	Oscillator	Recommended circuit parameters				Operating supply voltage Range [V]	Oscillation Stabilizing time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [s]	max [s]	
32.768kHz	Seiko Epson	C-002RX	18	18	OPEN	620k	4.5 to 5.5	1.00	1.50	

Notes: The oscillation stabilizing time period is the time until the VCO oscillation for the internal system becomes stable after the following conditions. (See Figure 3.)
1. The V_{DD} becomes higher than the minimum operating voltage after the power is supplied.
2. The HOLD mode is released.

The sample oscillation circuit characteristics may differ applications. For further assistance, please contact with oscillator manufacturer with the following notes in your mind.

- Since the oscillation frequency precision is affected by wiring capacity of the application board, etc., adjust the oscillation frequency on the production board.
- The above oscillation frequency and the operating supply voltage range are based on the operating temperature of -10°C to +70°C. For the use with the temperature outside of the range herein, or in the application requiring high reliability such as car products, please consult with oscillator manufacturer.
- When using the oscillator which is not shown in the sample oscillation circuit characteristics, please consult with Sanyo sales personnel.

Since the oscillation circuit characteristics are affected by the noise or wiring capacity because the circuit is designed with low gain in order to reduce the power dissipation, refer to the following notices.

- The distance between the clock I/O terminal (XT1 terminal XT2 terminal) and external parts should be as short as possible.
- The capacitors' V_{SS} should be allocated close to the microcontroller's GND terminal and be away from other GND.
- The signal lines with rapid state change or with large current should be allocated away from the oscillation circuit.

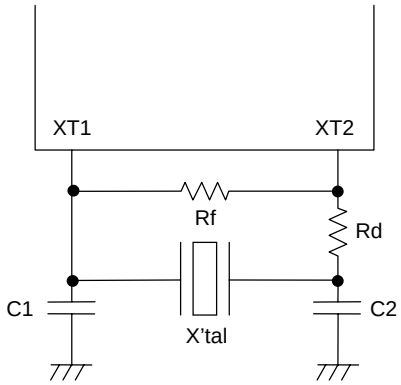


Figure 1 Recommended oscillation circuit

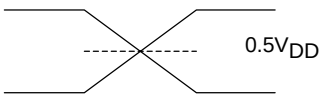
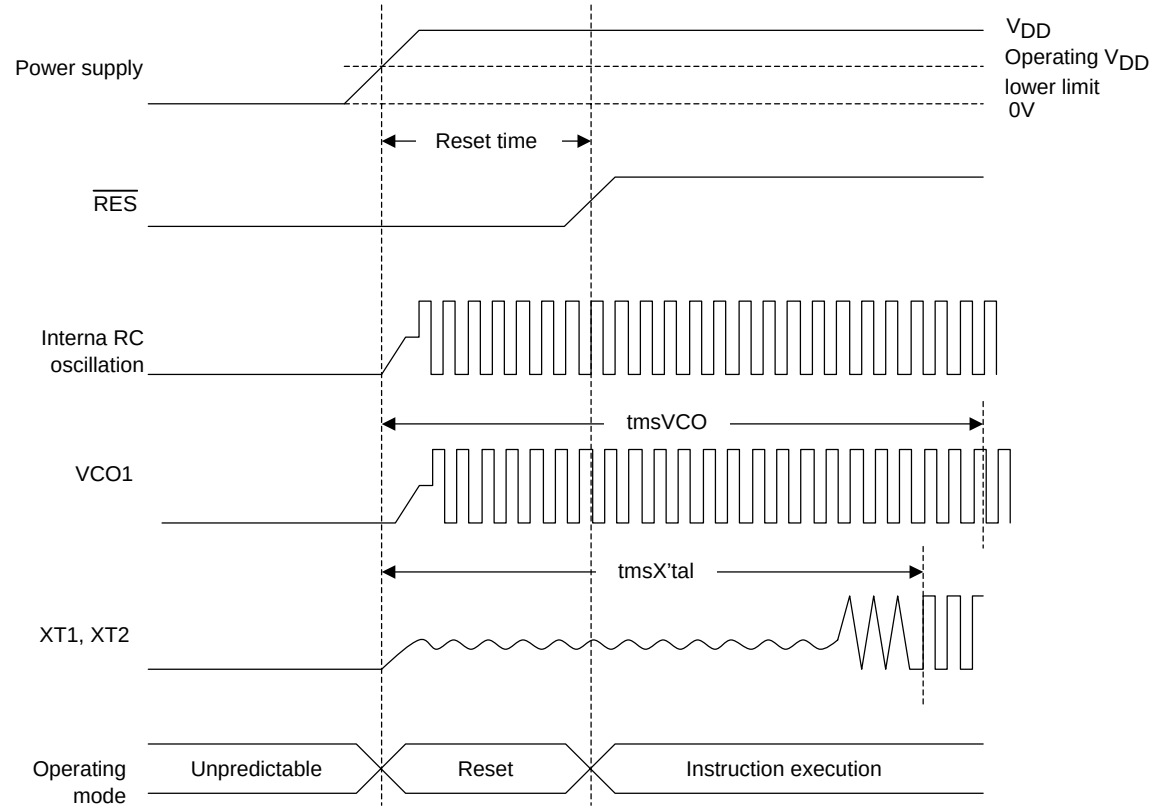
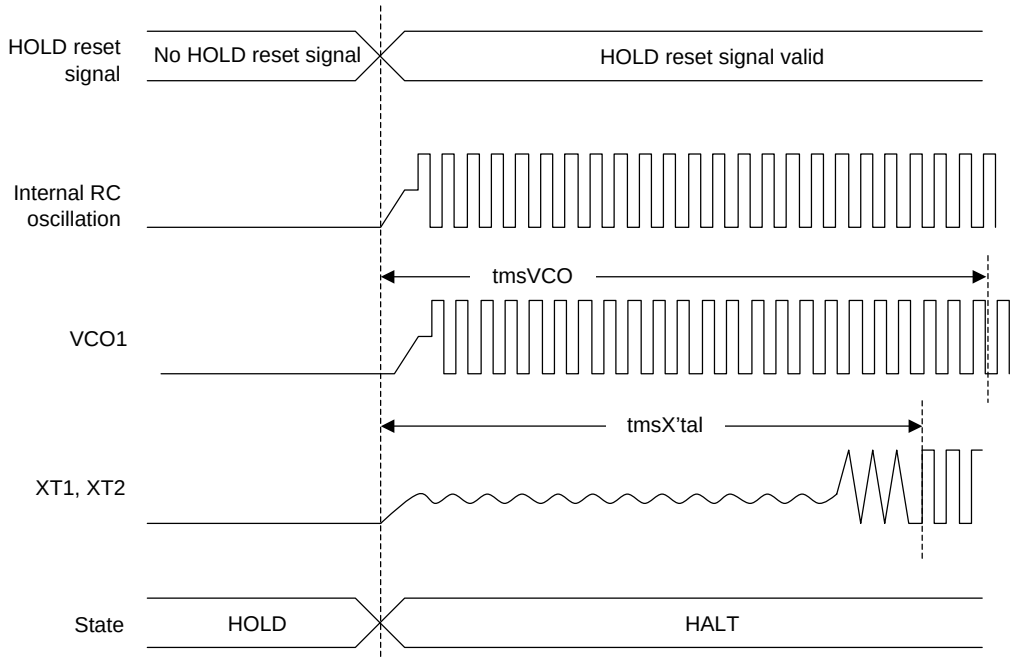


Figure 2 AC Timing Measurement Point

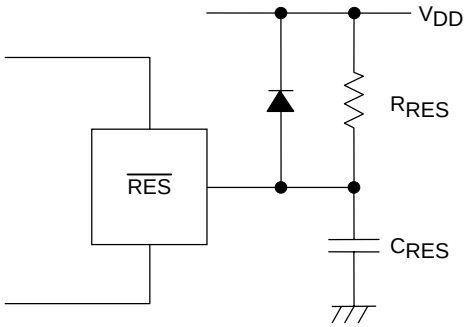


Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 3 Oscillation Stabilization Timing



Note:
Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of 200µs after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 4 Reset Circuit

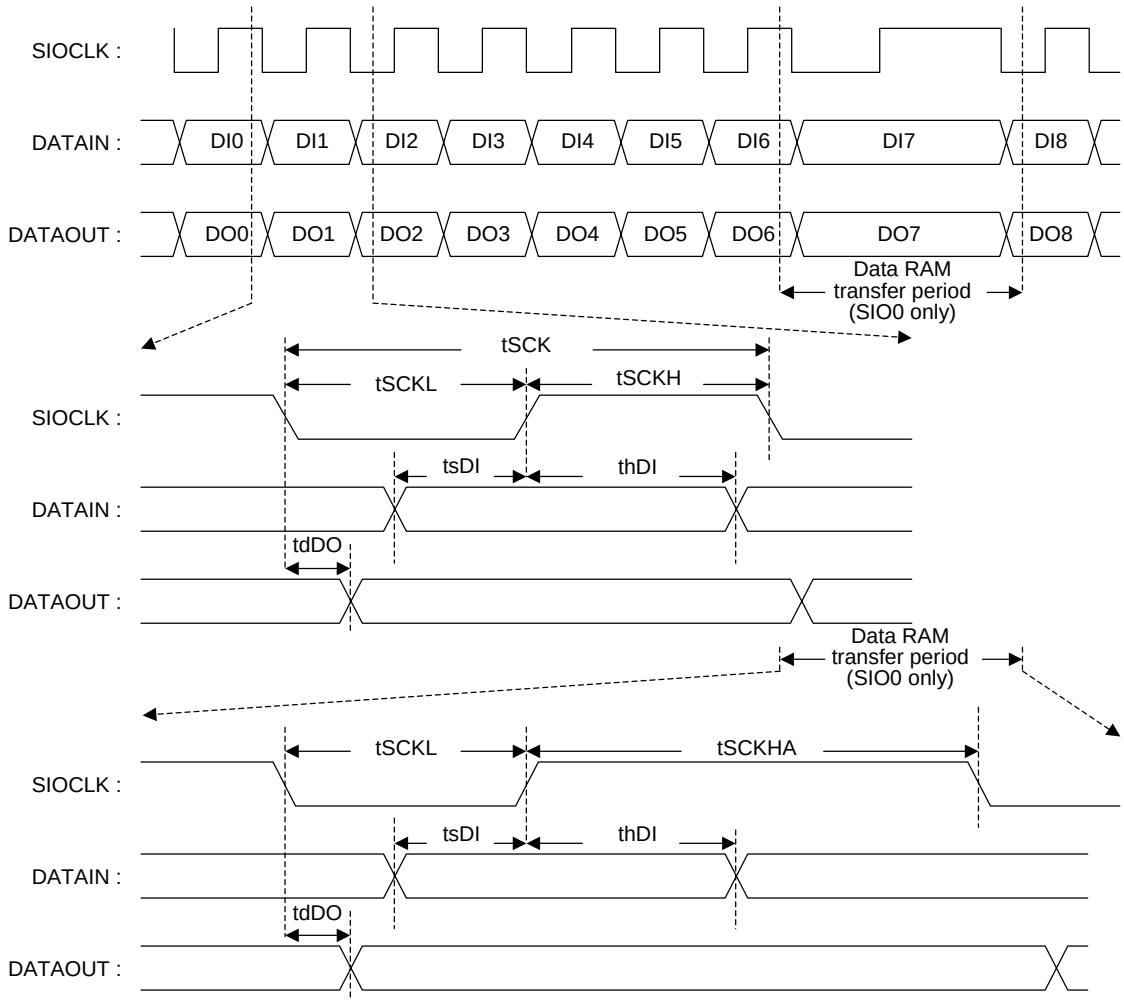


Figure 5 Serial I/O Output Waveforms

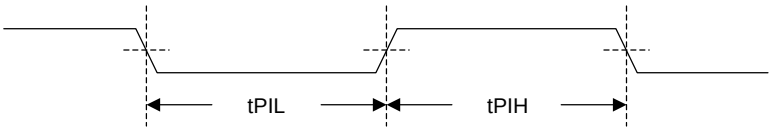


Figure 6 Pulse Input Timing Signal Waveform 1

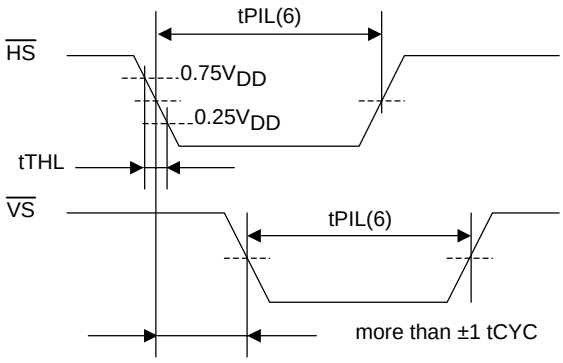
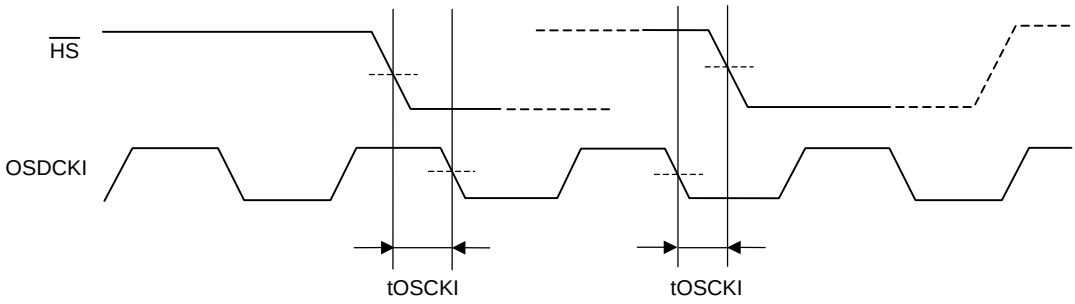
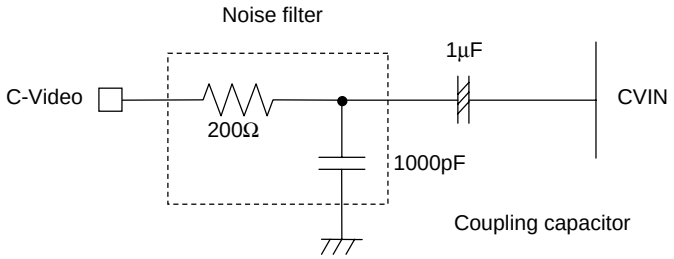


Figure 7 Pulse Input Timing Signal Waveform 2



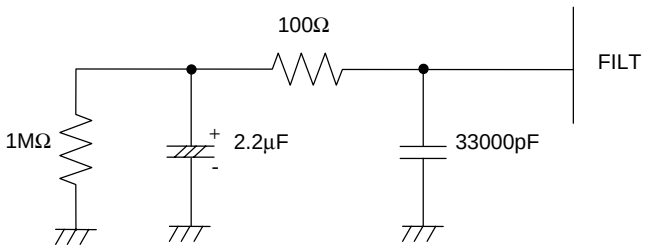
Note: Last transition of the t0SCKI must be saving constant.

Figure 8 Pulse Input Timing Signal Waveform 3



Note: The output impedance of the C-Video side as viewed from the input of the noise filter must be 100Ω or less.

Figure 9 Recommended CVIN Circuit



Note: Place the components to be connected to the FILT pin so that their trace length is minimum.

Figure 10 Recommended Filter Circuit