⊞ HARRIS

HD-15531

CMOS Manchester Encoder-Decoder

Features

- Support of MIL-STD-1553
- 2.5 Megabit/Sec Data Rate (15531B)
- 1.25 Megabit/Sec Data Rate (15531)
- Sync Identification and Lock-in
- Clock Recovery
- Variable Frame Length to 32-Bits
- Manchester II Encode, Decode
- Separate Encode and Decode
- Low Operating Power .... 50mW @ 5 Volts
- Full -55°C to +125°C Temperature Range Operation

Description

The Harris HD-15531 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate independently of each other, except for the master reset and word length functions.

This circuit provides many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.
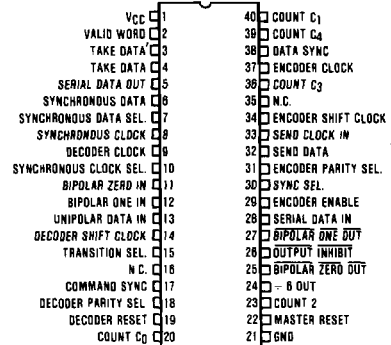
The HD-15531 also surpasses the requirements of MIL-STD-1553 by allowing the word length to be programmable (from 2 to 28 data bits). A frame consists of three bits for sync followed by the data word (2 to 28 data bits) followed by one bit of parity, thus the frame length will vary from 6 to 32 bit periods. This chip also allows selection of either even or odd parity for the Encoder and Decoder separately.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. For high speed applications the 15531B will support a 2.5 Megabit/sec data rate.
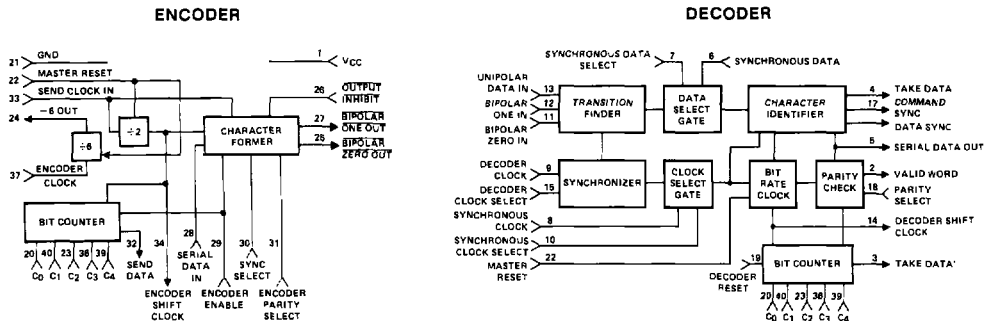
The HD-15531 can also be used in many party line digital data communications applications, such as a local area network or an environmental control system driven from a single twisted pair of fiber optic cable throughout a building.

Pinout

TOP VIEW

V_CC	1	40	COUNT C_1
VALID WORD	2	39	COUNT C_4
TAKE DATA'	3	38	DATA SYNC
TAKE DATA	4	37	ENCODER CLOCK
SERIAL DATA OUT	5	36	COUNT C_3
SYNCHRONOUS DATA	6	35	N.C.
SYNCHRONOUS DATA SEL.	7	34	ENCODER SHIFT CLOCK
SYNCHRONOUS CLOCK	8	33	SEND CLOCK IN
DECODER CLOCK	9	32	SEND DATA
SYNCHRONOUS CLOCK SEL.	10	31	ENCODER PARITY SEL.
BIPOLAR ZERO IN	11	30	SYNC SEL.
BIPOLAR ONE IN	12	29	ENCODER ENABLE
UNIPOLAR DATA IN	13	28	SERIAL DATA IN
DECODER SHIFT CLOCK	14	27	BIPOLAR ONE OUT
TRANSITION SEL.	15	26	OUTPUT INHIBIT
N.C.	16	25	BIPOLAR ZERO OUT
COMMAND SYNC	17	24	÷ 6 OUT
DECODER PARITY SEL	18	23	COUNT 2
DECODER RESET	19	22	MASTER RESET
COUNT C_0	20	21	GND

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Block Diagrams

ENCODER

DECODER

Caution These devices are sensitive to electronic discharge Proper I.C. handling procedures should be followed

Absolute Maximum Ratings

Supply Voltage..+7.0 Volts
Input, Output or I/O Voltage Applied ....GND -0.3V to VCC +0.3V
Storage Temperature Range ....-65°C to +150°C
Maximum Package Power Dissipation..1 Watt
θ_{jc}........................17°C/W (CERDIP package), 23°C/W (LCC package)

θ_{ja}.........................45°C/W (CERDIP package), 50°C/W (LCC package)
Gate Count .... 456 Gates
Junction Temperature..+150°C
Lead Temperature (Soldering, Ten Seconds)..................................+275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V	
Operating Temperature Range	
HD-15531-9 .... -40°C to +85°C	
HD-15531-2/-8 .... -55°C to +125°C	

Electrical Specifciations   T$_A$ = -40°C to +85°C (HD-15531-9),   T$_A$ = -55°C to +125°C (HD-15531-2/-8)

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	V$_{IH}$	Logical "1" Input Voltage	70% V$_{CC}$			V	
	V$_{IL}$	Logical "0" Input Voltage			20% V$_{CC}$	V	
	V$_{IHC}$	Logical "1" Input Voltage (Clock)	V$_{CC}$ -0.5			V	
	V$_{ILC}$	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	II	Input Leakage	-1.0		+1.0	μA	V$_{IN}$ = V$_{CC}$ or GND, DIP Pins 6-13, 15, 18, 19, 20, 22, 23, 26, 28-31, 33, 36 37, 39, 40
	V$_{OH}$	Logical "1" Output Voltage	2.4			V	I$_{OH}$ = -3mA
	V$_{OL}$	Logical "0" Output Voltage			0.4	V	I$_{OL}$ = 1.8mA
	I$_{CCSB}$	Supply Current Standby		0.5	2.0	mA	V$_{IN}$ = V$_{CC}$ = 5.5V Outputs Open
	I$_{CCOP}$	Supply Current Operating*		8.0	10.0	mA	V$_{CC}$ = 5.5V f = 15MHz
	C$_{IN}$	Input Capacitance		10		pF	All measurements are referenced to device
	C$_O$	Output Capacitance		14		pF	GND, T$_A$ = +25°C, F = 1MHz
		*Guaranteed and sampled but not 100% tested					
A.C.	**ENCODER TIMING** VCC = 5.0V ± 10%						
	(1) F$_{EC}$	Encoder Clock Frequency	0		15	MHz	C$_L$ = 50pF
	(2) F$_{ESC}$	Send Clock Frequency	0		2.5	MHz	
	(3) T$_{ECR}$	Encoder Clock Rise Time			8	ns	
	(4) T$_{ECF}$	Encoder Clock Fall Time			8	ns	
	(5) F$_{ED}$	Data Rate	0		1.25	MHz	
	(6) T$_{MR}$	Master Reset Pulse Width	150			ns	
	(7) T$_{E1}$	Shift Clock Delay			125	ns	
	(8) T$_{E2}$	Serial Data Setup	75			ns	
	(9) T$_{E3}$	Serial Data Hold	75			ns	
	(10) T$_{E4}$	Enable Setup	90			ns	
	(11) T$_{E5}$	Enable Pulse Width	100			ns	
	(12) T$_{E6}$	Sync Setup	55			ns	
	(13) T$_{E7}$	Sync Pulse Width	150			ns	
	(14) T$_{E8}$	Send Data Delay	0		50	ns	
	(15) T$_{E9}$	Bipolar Ouput Delay			130	ns	
	(16) T$_{E10}$	Enable Hold	10			ns	
	(17) T$_{E11}$	Sync Hold	95			ns	
A.C.	**DECODER TIMING** VCC = 5.0V ± 10%						
	(18) F$_{DC}$	Decoder Clock Frequency	0		15	MHz	C$_L$ = 50pF
	(19) F$_{DS}$	Decoder Sync Clock	0		2.5	MHz	
	(20) T$_{DCR}$	Decoder Clock Rise Time			8	ns	
	(21) T$_{DCF}$	Decoder Clock Fall Time			8	ns	
	(22) F$_{DD}$	Data Rate	0		1.25	MHz	
	(23) T$_{DR}$	Decoder Reset Pulse Width	150			ns	
	(24) T$_{DRS}$	Decoder Reset Setup Time	75			ns	
	(25) T$_{DRH}$	Decoder Reset Hold Time	10			ns	
	(26) T$_{MR}$	Master Reset Pulse	150			ns	
	(27) T$_{D1}$	Bipolar Data Pulse Width	T$_{DC}$ +10			ns	(Note 1)
	(28) T$_{D2}$	Sync Transition Span		18T$_{DC}$		ns	(Note 1)
	(29) T$_{D3}$	One Zero Overlap			TDC -10	ns	(Note 1)
	(30) T$_{D4}$	Short Data Transition Span		6T$_{DC}$		ns	(Note 1)
	(31) T$_{D5}$	Long Data Transition Span		12T$_{DC}$		ns	(Note 1)
	(32) T$_{D6}$	Sync Delay (ON)	-20		110	ns	
	(33) T$_{D7}$	Take Data Delay (ON)	0		110	ns	
	(34) T$_{D8}$	Serial Data Out Delay			80	ns	
	(35) T$_{D9}$	Sync Delay (OFF)	0		110	ns	
	(36) T$_{D10}$	Take Data Delay (OFF)	0		110	ns	
	(37) T$_{D11}$	Valid Word Delay	0		110	ns	
	(38) T$_{D12}$	Sync Clock to Shift Clock Delay			75	ns	
	(39) T$_{D13}$	Sync Data Setup	75			ns	

NOTE 1. TDC = Decoder Clock Period = $\dfrac{1}{FDC}$,   (These parameters are guaranteed but not 100% tested)

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Absolute Maximum Ratings

Supply Voltage .... +7.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.3V to VCC +0.3V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θjc .... 17°C/W (CERDIP package), 23°C/W (LCC package)

θja .... 45°C/W (CERDIP package), 50°C/W (LCC package)
Gate Count .... 456 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
HD-15531B-9 .... -40°C to +85°C
HD-15531B-2/-8 .... -55°C to +125°C

Electrical Specifications

T_A = -40°C to +85°C (HD-15531B-9), T_A = -55°C to +125°C (HD-15531B-2/-8)

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
	V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
	V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
	V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	II	Input Leakage	-1.0		+1.0	µA	V_{IN} = V_{CC} or GND, DIP Pins 6-13, 15, 18, 19, 20, 22, 23, 26, 28-31. 33, 36, 37, 39, 40
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
	V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
	I_{CCSB}	Supply Current Standby		0.5	2.0	mA	V_{IN} = V_{CC} = 5.5V Outputs Open
	I_{CCOP}	Supply Current Operating*		8.0	10.0	mA	V_{CC} = 5.5V f = 15MHz All measurements are referenced to device GND, T_A = +25°C, F = 1MHz
	C_{IN}	Input Capacitance		10		pF	
	C_O	Output Capacitance		14		pF	

*Guaranteed and sampled but not 100% tested

ENCODER TIMING VCC = 5.0V ± 10%

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
A.C.	(1) F_{EC}	Encoder Clock Frequency	0		30	MHz	C_L = 50pF
	(2) F_{ESC}	Send Clock Frequency	0		5.0	MHz	
	(3) T_{ECR}	Encoder Clock Rise Time			8	ns	
	(4) T_{ECF}	Encoder Clock Fall Time			8	ns	
	(5) F_{ED}	Data Rate	0		2.5	MHz	
	(6) T_{MR}	Master Reset Pulse Width	150			ns	
	(7) T_{E1}	Shift Clock Delay			80	ns	
	(8) T_{E2}	Serial Data Setup	50			ns	
	(9) T_{E3}	Serial Data Hold	50			ns	
	(10) T_{E4}	Enable Setup	90			ns	
	(11) T_{E5}	Enable Pulse Width	100			ns	
	(12) T_{E6}	Sync Setup	55			ns	
	(13) T_{E7}	Sync Pulse Width	150			ns	
	(14) T_{E8}	Send Data Delay	0		50	ns	
	(15) T_{E9}	Bipolar Ouput Delay			130	ns	
	(16) T_{E10}	Enable Hold	10			ns	
	(17) T_{E11}	Sync Hold	95			ns	

DECODER TIMING VCC = 5.0V ± 10%

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
A.C.	(18) F_{DC}	Decoder Clock Frequency	0		30	MHz	C_L = 50pF
	(19) F_{DS}	Decoder Sync Clock	0		5.0	MHz	
	(20) T_{DCR}	Decoder Clock Rise Time			8	ns	
	(21) T_{DCF}	Decoder Clock Fall Time			8	ns	
	(22) F_{DD}	Data Rate	0		2.50	MHz	
	(23) T_{DR}	Decoder Reset Pulse Width	150			ns	
	(24) T_{DRS}	Decoder Reset Setup Time	75			ns	
	(25) T_{DRH}	Decoder Reset Hold Time	10			ns	
	(26) T_{MR}	Master Reset Pulse	150			ns	
	(27) T_{D1}	Bipolar Data Pulse Width	T_{DC} +10			ns	(Note 1)
	(28) T_{D2}	Sync Transition Span		18T_{DC}		ns	(Note 1)
	(29) T_{D3}	One Zero Overlap			T_{DC} -10	ns	(Note 1)
	(30) T_{D4}	Short Data Transition Span		6T_{DC}		ns	(Note 1)
	(31) T_{D5}	Long Data Transition Span		12T_{DC}		ns	(Note 1)
	(32) T_{D6}	Sync Delay (ON)	-20		110	ns	
	(33) T_{D7}	Take Data Delay (ON)	0		110	ns	
	(34) T_{D8}	Serial Data Out Delay			80	ns	
	(35) T_{D9}	Sync Delay (OFF)	0		110	ns	
	(36) T_{D10}	Take Data Delay (OFF)	0		110	ns	
	(37) T_{D11}	Valid Word Delay	0		110	ns	
	(38) T_{D12}	Sync Clock to Shift Clock Delay			75	ns	
	(39) T_{D13}	Sync Data Setup	75			ns	

NOTE 1. TDC = Decoder Clock Period = $\frac{1}{FDC}$, (These parameters are guaranteed but not 100% tested)

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Pin Description

| PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
1		V_{CC}	Both	Positive supply pin. A 0.1μF decoupling capacitor from V_{CC} (pin 1) to GROUND (pin 21) is recommended.
2	O	VALID WORD	Decoder	Output high indicates receipt of a valid word. (valid parity and no Manchester errors).
3	O	TAKE DATA'	Decoder	A continuous, free running signal provided for host timing or data handling. When data is present on the bus, this signal will be synchronized to the incoming data and will be identical to take data.
4	O	TAKE DATA	Decoder	Output is high during receipt of data after identification of a valid sync pulse and two valid Manchester bits.
5	O	SERIAL DATA OUT	Decoder	Delivers received data in correct NRZ format.
6	I	SYNCHRONOUS DATA	Decoder	Input presents Manchester data directly to character identification logic SYNCHRONOUS DATA SELECT must be held high to use this input. If not used this pin must be held high.
7	I	SYNCHRONOUS DATA SELECT	Decoder	In high state allows the synchronous data to enter the character identification logic. Tie this input low for asynchronous data
8	I	SYNCHRONOUS CLOCK	Decoder	Input provides externally synchronized clock to the decoder, for use when receiving synchronous data. This input must be tied high when not in use
9	I	DECODER CLOCK	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder. Input a frequency equal to 12X the data rate
10	I	SYNCHRONOUS CLOCK SELECT	Decoder	In high state directs the SYNCHRONOUS CLOCK to control the decoder character identification logic. A low state selects the DECODER CLOCK
11	I	BIPOLAR ZERO IN	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the unipolar input is used
12	I	BIPOLAR ONE IN	Decoder	A high input should be applied when the bus is in its positive state This pin must be held low when the unipolar input is used.
13	I	UNIPOLAR DATA IN	Decoder	With pin 11 high and pin 12 low, this pin enters unipolar data into the transition finder circuit If not used this input must be held low
14	O	DECODER SHIFT CLOCK	Decoder	Output which delivers a frequency (DECODER CLOCK ÷ 12) synchronous by the recovered serial data stream.
15	I	TRANSITION SELECT	Decoder	A high input to this pin causes the transition finder to synchronize on every transition of input data. A low input causes the transition finder to synchronize only on mid-bit transitions
16		N C	Blank	Not connected.
17	O	COMMAND SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character
18	I	DECODER PARITY SELECT	Decoder	An input for parity sense, calling for even parity with input high and odd parity with input low
19	I	DECODER RESET	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
20	I	COUNT C_0	Both	One of five binary inputs which establish the total bit count to be encoded or decoded.
21		GROUND	Both	Supply pin
22	I	MASTER RESET	Both	A high on this pin clears 2.1 counters in both encoder and decoder, and resets the ÷ 6 circuit.
23	I	COUNT C_2	Both	See pin 20.
24	O	÷ 6 OUT	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK
25	O	BIPOLAR ZERO OUT	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver
26	I	OUTPUT INHIBIT	Encoder	A low on this pin forces pin 25 and 27 high, the inactive states
27	O	BIPOLAR ONE OUT	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver
28	I	SERIAL DATA IN	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
29	I	ENCODER ENABLE	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceding cycle being complete.)
30	I	SYNC SELECT	Encoder	Actuates a Command sync for an input high and Data sync for an input low
31	I	ENCODER PARITY SELECT	Encoder	Sets transmit parity odd for a high input, even for a low input
32	O	SEND DATA	Encoder	Is an active high output which enables the external source of serial data.
33	I	SEND CLOCK IN	Encoder	Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.
34	O	ENCODER SHIFT CLOCK	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI pin-28 on the low-to-high transition of ESC.
35		N C	Blank	Not connected
36	I	COUNT C3	Both	See pin 20.
37	I	ENCODER CLOCK	Encoder	Input to the 6:1 divider, a frequency equal to 12 times the data rate is usually input here.
38	O	DATA SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a data synchronizing character
39	I	COUNT C4	Both	See pin 20
40	I	COUNT C1	Both	See pin 20

I = Input   O = Output

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Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK. The frame length is set by programming the COUNT inputs. Parity is selected by programming ENCODER PARITY SELECT high for odd parity or low for even parity.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or K + 4 ENCODER SHIFT CLOCK periods, where K is the number of bits to be sent. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a Command sync or a low will produce a Data sync for the word ②. When the Encoder is ready to accept data, the SEND DATA output will go high for K ENCODER SHIFT CLOCK periods ④. During these K periods the data should be clocked into the SERIAL DATA input with every high-to-low transition of the ENCODER SHIFT CLOCK ③ - ④ so it can be sampled on the low-to-high transition. After the sync and Manchester II encoded data are transmitted through the BIPOLAR ONE and BIPOLAR ZERO outputs, the Encoder adds on an additional bit with the parity for that word ⑤. If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time ⑤ (as shown) to prevent a consecutive word from being encoded. At any time a low on OUTPUT INHIBIT input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Any time after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.
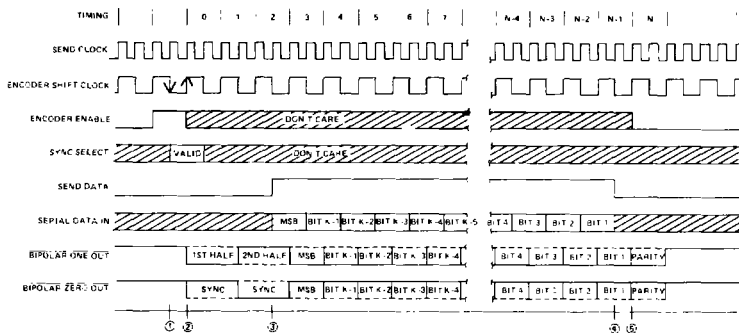
Decoder Operation

To operate the Decoder asynchronously requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. To operate the Decoder synchronously requires a SYNCHRONOUS CLOCK at a frequency 2 times the data rate which is synchronized with the data at every high-to-low transition applied to the SYNCHRONOUS CLK input. The Manchester II coded data can be presented to the Decoder asynchronously in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept noninverted Manchester II coded data. (e.g. from BIPOLAR ONE OUT on an Encoder through an inverter to Unipolar Data Input).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated by a high level at either COMMAND SYNC or DATA SYNC output. If the sync character was a command sync the COMMAND SYNC output will go high ② and remain high for K SHIFT CLOCK periods ③, where K is the number of bits to be received. If the sync character was a data sync the DATA SYNC output will go high. The TAKE DATA output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock ② - ③. Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all K decoded bits have been transmitted ③ the data is checked for parity. A high input on DECODER PARITY SELECT will set the Decoder to check for even parity or a low input will set the Decoder to check for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately K + 4 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown ①.

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.
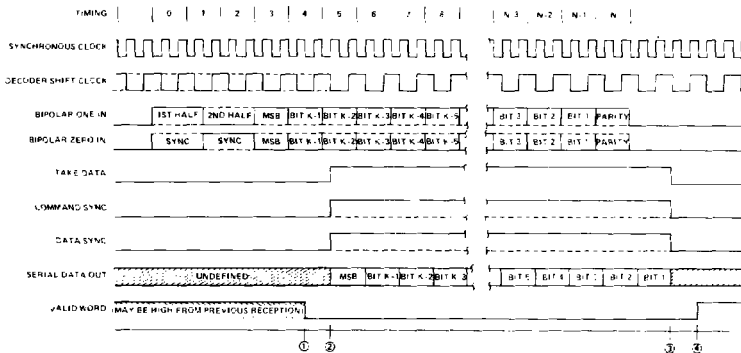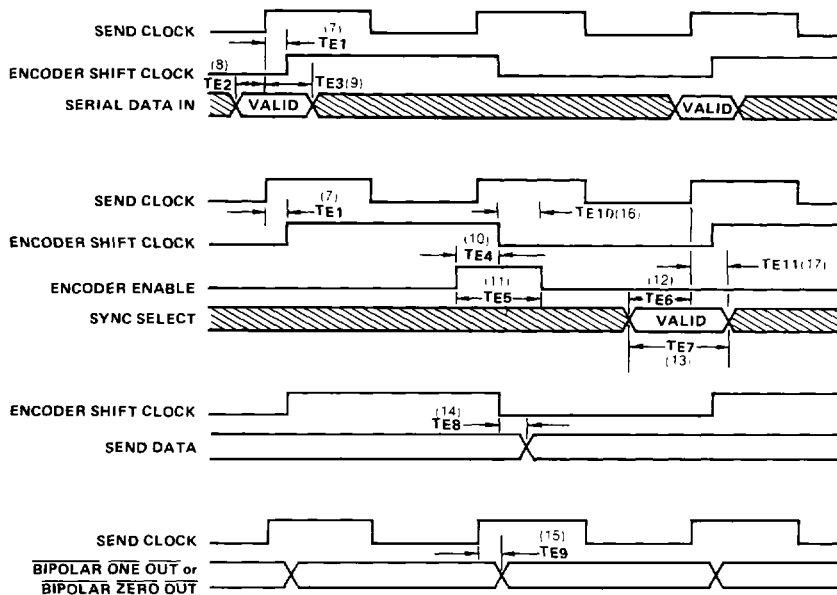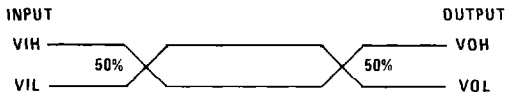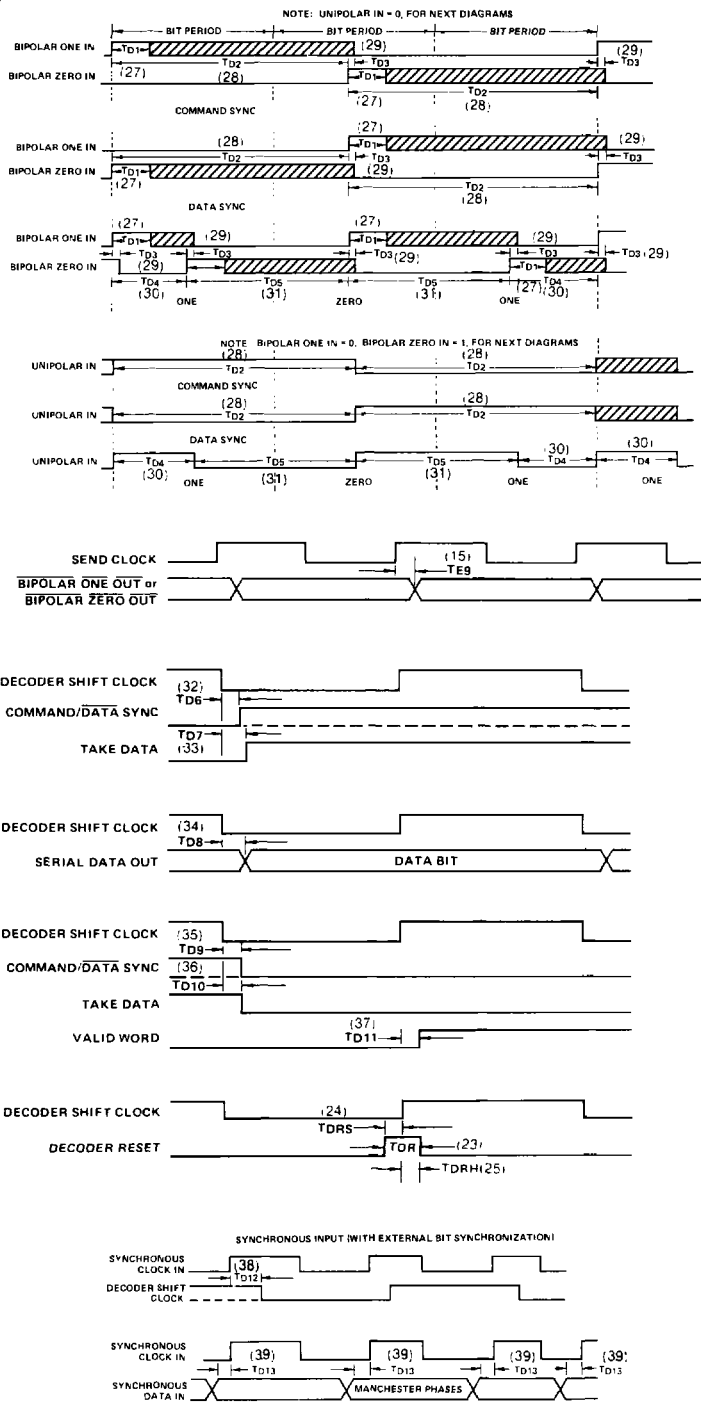
Encoder Timing

A.C. Testing Input, Output Waveform

A.C. Testing. All inputs signals must switch between VIL and VIH
Input rise and fall times are driven at 1nsec per volt

Decoder Timing

Frame Counter

DATA BITS	FRAME LENGTH (BIT PERIODS)	C_4	C_3	C_2	C_1	C_0
2	6	L	L	H	L	H
3	7	L	L	H	H	L
4	8	L	L	H	H	H
5	9	L	H	L	L	L
6	10	L	H	L	L	H
7	11	L	H	L	H	L
8	12	L	H	L	H	H
9	13	L	H	H	L	L
10	14	L	H	H	L	H
11	15	L	H	H	H	L
12	16	L	H	H	H	H
13	17	H	L	L	L	L
14	18	H	L	L	L	H
15	19	H	L	L	H	L

DATA BITS	FRAME LENGTH (BIT PERIODS)	C_4	C_3	C_2	C_1	C_0
16	20	H	L	L	H	H
17	21	H	L	H	L	L
18	22	H	L	H	L	H
19	23	H	L	H	H	-
20	24	H	L	H	H	H
21	25	H	H	L	L	L
22	26	H	H	L	L	H
23	27	H	H	L	H	L
24	28	H	H	L	H	H
25	29	H	H	H	L	L
26	30	H	H	H	L	H
27	31	H	H	H	H	L
28	32	H	H	H	H	H

The above Table demonstrates all possible combinations of frame lengths ranging from 6 to 32 bits. The pin word described here is common to both the Encoder and Decoder.

Applications

How to Make Our MTU Look Like a Manchester Encoded UART
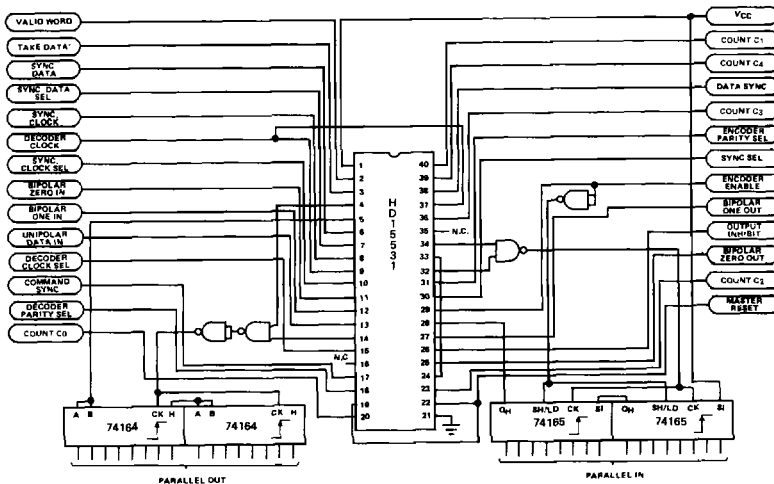
Typical Timing Diagram for a Manchester Encoded UART

ENCODER TIMING

DECODER TIMING
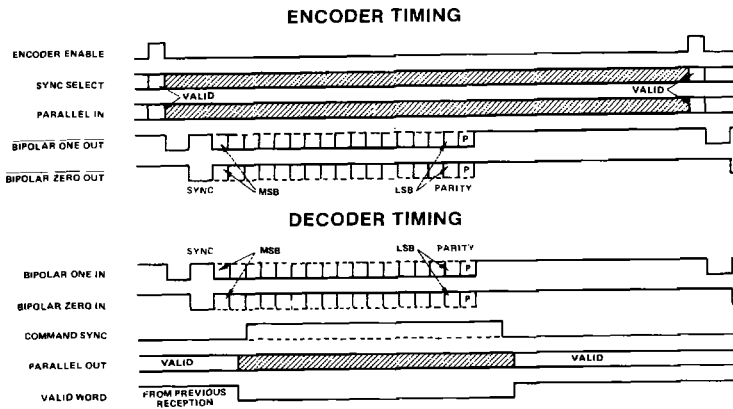
MIL-STD-1553

The 1553 standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HD-15531 supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words, and Data. Terminals respond with Status Words, and Data. Each word is preceded by a synchronizing pulse, and followed by parity bit, occupying a total of 20μ sec. The word formats are shown in Figure 4. The special abbreviations are as follows:

P   Parity, which is defined to be odd, taken across all 17 bits.

R/T Receive on logical zero, transmit on ONE.

ME   Message Error if logical 1.

TF   Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553, and do not completely describe its bus requirements, timing or protocols.
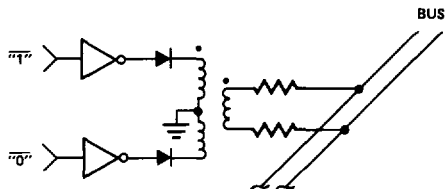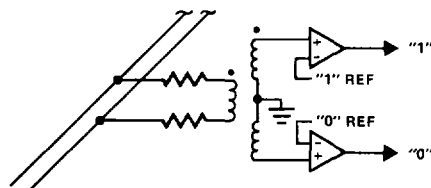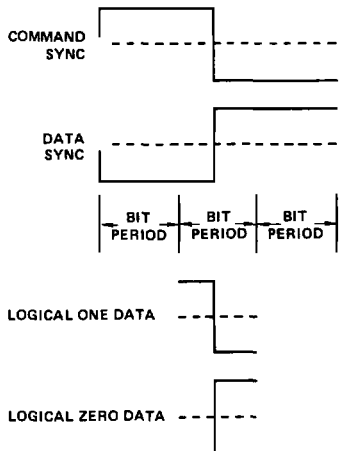

FIGURE 1. SIMPLIFIED MIL-STD-1553 DRIVER

FIGURE 2. SIMPLIFIED MIL-STD-1553 RECEIVER
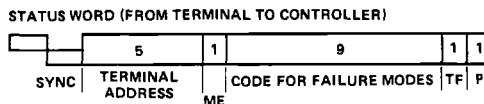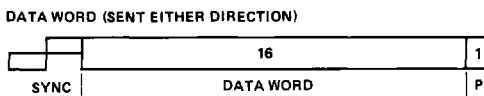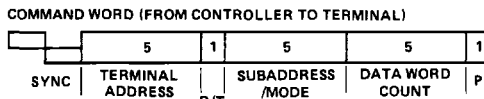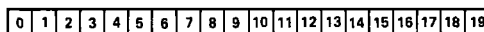

FIGURE 3. MIL-STD-1553 CHARACTER FORMATS

FIGURE 4. MIL-STD-1553 WORD FORMATS

NOTE: This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HD-15531.