

6.0V~28V, 1.2A 1ch

1ch Step-Down Switching Regulator

BD9E151NUX

General Description

The BD9E151NUX is a 28V, 1.2A diode-rectification buck converter that integrated internal high-side 30V Power MOSFET. To increase efficiency at light loads, a pulse skipping is automatically activated. Furthermore, the 0uA shutdown supply current allows the device to be used in battery powered application. Current mode control with internal slope compensation simplifies the external component count while allowing the use of ceramic output capacitors.

Features

- High and Wide Input Range (VIN=6V~28V)
- 30V/80mΩ Internal Power MOSFET
- 600kHz Fixed Operating Frequency
- Feedback Pin Voltage 1.0V±1.0%
- Internal Over Current Protection(OCP), Under Voltage Locked Out(UVLO), Over Voltage Protection(OVP), Thermal Shut down(TSD)
- 0μA Low Shutdown Supply Current
- VSON008X2030 package

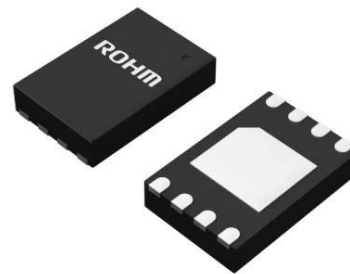
Key Specifications

■ Input Voltage	6 ~ 28 [V]
■ Ref. Precision (Ta=25°C)	±1.0[%]
■ Max Output Current	1.2 [A] (Max.)
■ Operating Temperature	-40°C~85°C
■ Operating Junction Temperature	-55°C ~ 125°C

Packages

VSON008X2030

2.00mm x3.00mm x 0.60mm



VSON008X2030

Applications

- Surveillance Camera Applications
- OA Applications
- 12V, 24V Distributed Power Systems

Typical Application Circuits

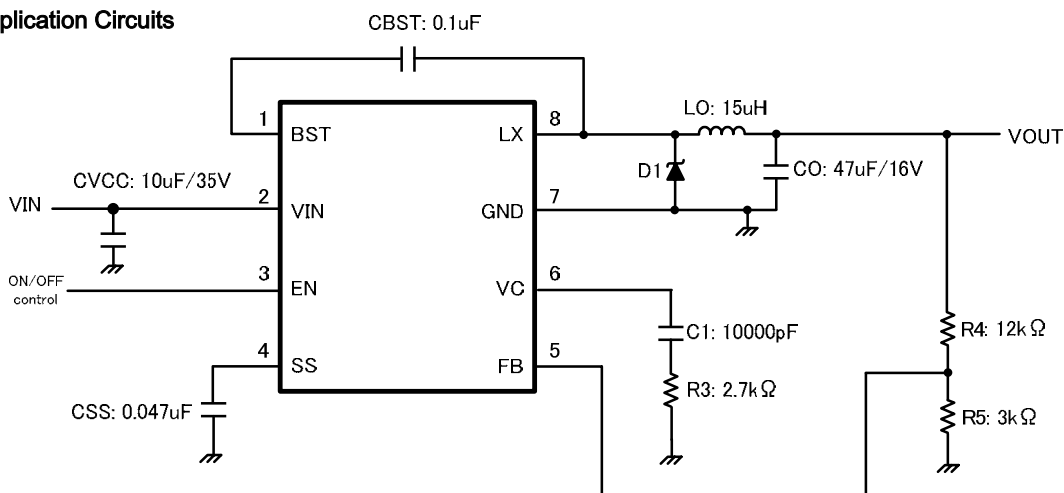


Figure 1. Typical Application Circuit

○Structure : Silicon Monolithic Integrated Circuit ○This product is not designed for normal operation within a radioactive

Pin Configuration

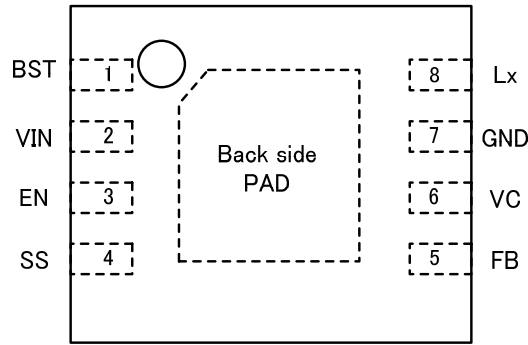


Figure 2. Pin Configuration (TOP VIEW)

Pin Description

Pin No.	Pin Name	Description
1	BST	The pin is power supply for floating Power NMOS driver. Connect bypass capacitor between the pin and LX pin for bootstrap operation.
2	VIN	Input supply. Place bypass capacitor as close as possible to this pin.
3	EN	Enable input pin. Apply more than 2.4V to start-up the DCDC. This pin is pulled down by 700kΩ, apply less than 0.8V or open to shutdown the DCDC.
4	SS	Soft start pin. An external capacitor connected to this pin sets output rise time.
5	FB	Inverting node of the gm amplifier.
6	VC	Error amplifier output, and input to the PWM comparator. Connect phase compensation components to this pin.
7	GND	Ground.
6	LX	Place schottky barrier diode as close as possible and inductor to this pin.
-	Back side PAD	PAD for radiation of heat. Connect to GND is recommended.

Block Diagram

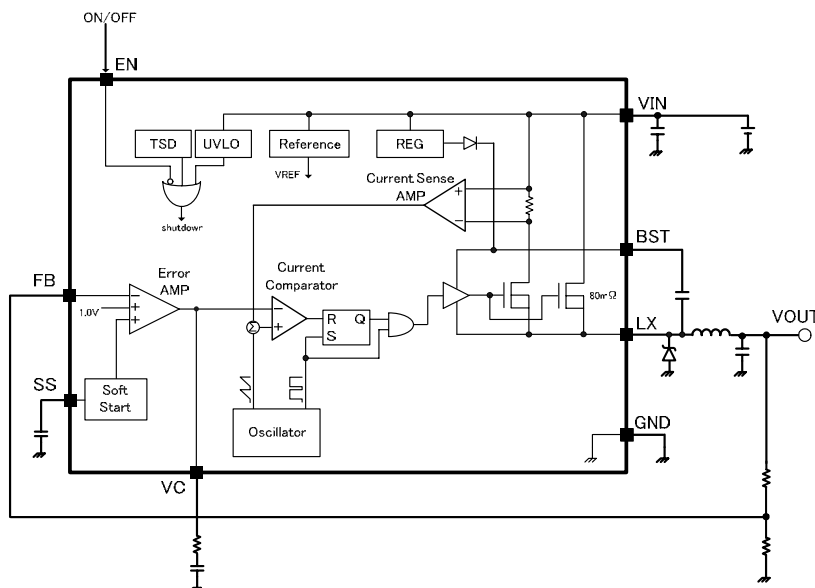


Figure 3. Block Diagram

Description of Blocks

1. Reference
This block generates reference voltage and current. It start operation by applying EN=H.
It provides reference voltage and current to error amplifier, oscillator, and etc.
2. REG
This is a gate drive voltage generator and 5.5V regulator for internal circuit power supply.
3. OSC
This is a precise wave oscillation circuit with operation frequency fixed to 600 kHz
4. Soft Start
This block does Soft Start to the output voltage of DC/DC converter, and prevents in-rush current during Start-up.
Soft Start Time set by the capacitor connected to SS pin and SS charge current is the time from EN Pin start-up to reaching to 1.0V.
5. ERROR AMP
This is an error amplifier that detects output signal, and outputs PWM control signal. Internal reference voltage is set to 1.0V. Connect phase compensation components between this pin and ground (ref. p.11).
6. OVP
The OVP circuit includes an overvoltage comparator to compare the FB pin voltage and internal thresholds. When the FB pin voltage goes above $110\% \times FB$, the high-side MOSFET will be forced off. When the FB pin voltage falls below 105%, the high-side MOSFET will be enabled again.
7. ICOMP
The BD9E151NUX implements current mode control that uses the VC pin voltage to turn off the high-side MOSFET on a cycle by cycle basis. Every cycle the switch current and the COMP pin voltage are compared; when the peak inductor current intersects the VC pin voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, causing the switch current to increase.
8. OCP
This is a circuit to protect the high-side FET from overcurrent. Every cycle the switch current and the reference voltage of overcurrent protection are compared; when the peak inductor current intersects the reference voltage, the high-side switch is turned off. Once overcurrent is detected, the device will stop and VC pin voltage will be reset and SS pin voltage will be discharged by 2uA (hiccup operation). Then SS pin voltage reaches to less than 0.1V, IC will restart.
9. High-side MOSFET
This is a 30V/80mΩ high-side MOSFET that converts inductor current of DC/DC converter.
Because the current limiting of this FET is 1.6A included ripple current, please use at within 1.6A.
10. UVLO
This is a low voltage error prevention circuit.
This prevents internal circuit error during increase of power supply voltage and during decline of power supply voltage.
It monitors VIN pin voltage and internal REG voltage, and when VIN voltage becomes 5.2V and below, it turns OFF all output FET and turns OFF DC/DC comparator output and Soft Start circuit resets.
Now this Threshold has hysteresis of 200mV.
11. TSD
This is a heat protect circuit.
When it detects an abnormal temperature exceeding maximum junction temperature ($T_j=150^\circ\text{C}$), it turns OFF all Output FET, and turns OFF DC/DC converter output. When temperature falls, it automatically returns.
12. EN
When a Voltage of 2.4V or more is applied, it turns ON, at Open or 0V application, it turns OFF.
About 700kΩ Pull-down Resistance is contained within the Pin.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
VIN to GND	VIN	30	V
BST to GND	VBST	37	V
BST to LX	Δ VBST	7	V
EN to GND	VEN	30	V
LX to GND	VLX	30	V
FB to GND	VFB	7	V
VC to GND	VSS	7	V
SS to GND	VSS	7	V
High-side FET Drain Current	IDH	1.6	A
Power Dissipation	Pd	2 ^(*1)	W
Operating Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-55 ~ +125	°C
Junction Temperature	Tjmax	150	°C

(*1)During mounting of 70×70×1.6^t mm 4layer board.Reduce by 20mW for every 1°C increase. (Above 25°C)

Operating Ratings

Item	Symbol	Ratings			Unit
		Min	Typ	Max	
Input Voltage	VIN	6	-	28	V
Output Voltage	VOUT	1.0 ^(*2)	-	VIN×0.7 or VIN-5	V
Output Current	IOUT	-	-	1.2	A

(*2)Restricted by minimum on pulse typ. 100nsec

Electrical Characteristics (Unless otherwise specified Ta=25°C, VIN=12V, VOUT=5V)

Parameter	Symbol	Limits			Unit	Conditions	
		Min.	Typ.	Max			
【Circuit current】							
Stand-by current of VIN	Ist	-	0	10	uA	VEN=0	
Circuit current of VIN	Icc	-	0.8	1.6	mA	FB=1.5V	
【Under voltage Lock out (UVLO)】							
Reset threshold voltage	Vuv	5.0	5.4	5.8	V	VIN rising	
Hysteresis width	Vuvhy	-	200	400	mV		
【Oscillator】							
Oscillating frequency	fsw	540	600	660	kHz		
Max duty cycle	Dmax	85	91	-	%		
【Error amplifier】							
FB threshold voltage	VFB	0.990	1.000	1.010	V		
Input bias current	IFB	-1.0	0	1.0	uA	VFB=0V	
Error amplifier DC gain	AVEA	-	600	6000	V/V		
Error amplifier transconductance	GEA	-	250	500	uA/V	IVC=±10uA, VC=1.0V	
【Current sense amplifier】							
VC to switch current transconductance	Gcs	-	10	20	A/V		
【Output】							
High-side MOSFET ON resistance	RonH	-	80	160	mΩ		
Over current detect current	Iocp	1.6	2.2	-	A		
【CTL】							
EN pin control voltage	ON	VEN	2.4	-	VIN	V	Ta=-40~85°C VIN=6~28V
	OFF	VENOFF	-0.3	-	0.8	V	
EN pin input current	REN	6.0	7.0	15.0	uA	VEN=5V	
【SOFT START】							
Charge current	Iss	1	2	4	uA		

©Not designed to withstand radiation.

Typical Performance Characteristics (Unless otherwise specified, Ta=25°C, VCC=12V, Vo=5V,)

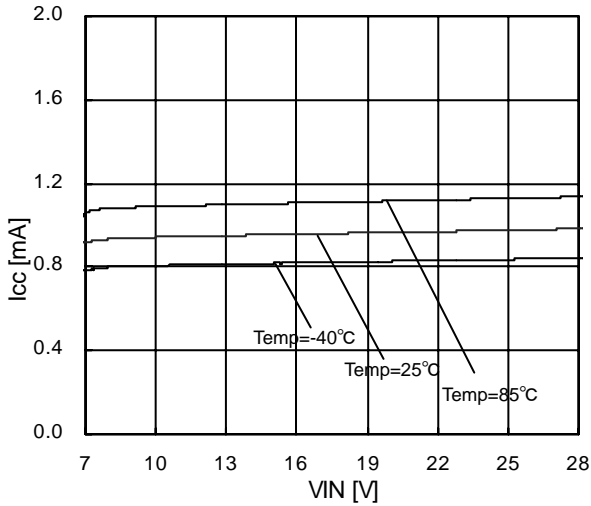


Figure 4. Operating Current - Input Voltage

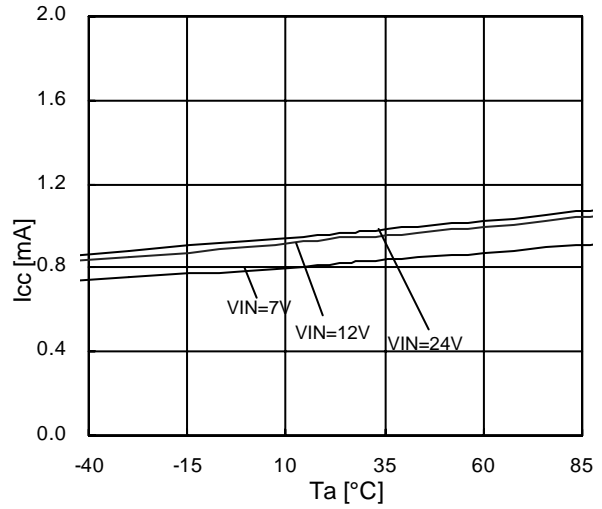


Figure 5. Operating Current - Temperature

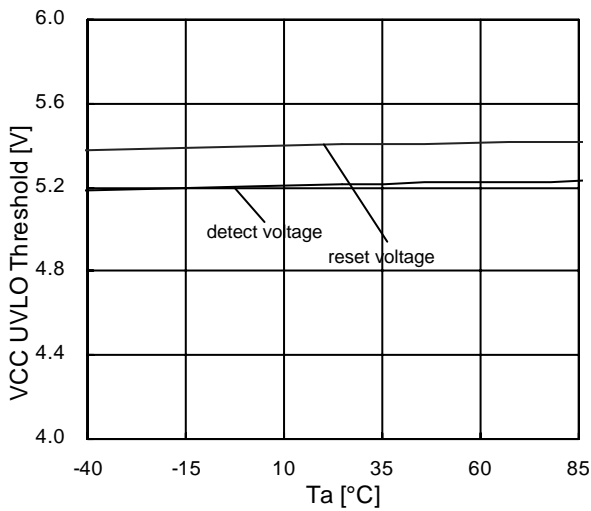


Figure 6. UVLO Threshold - Temperature

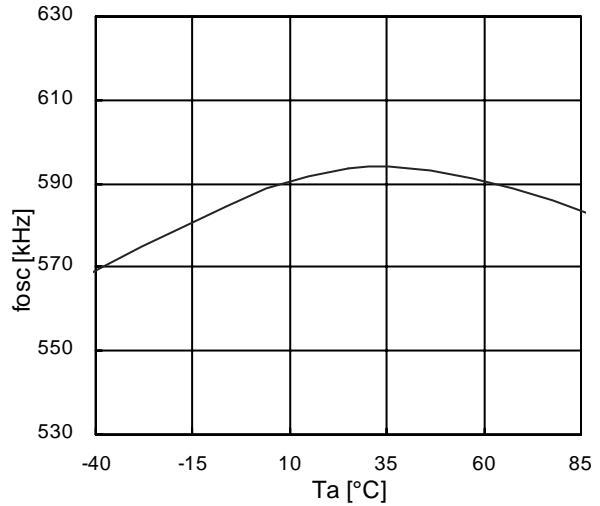


Figure 7. Switching Frequency - Temperature

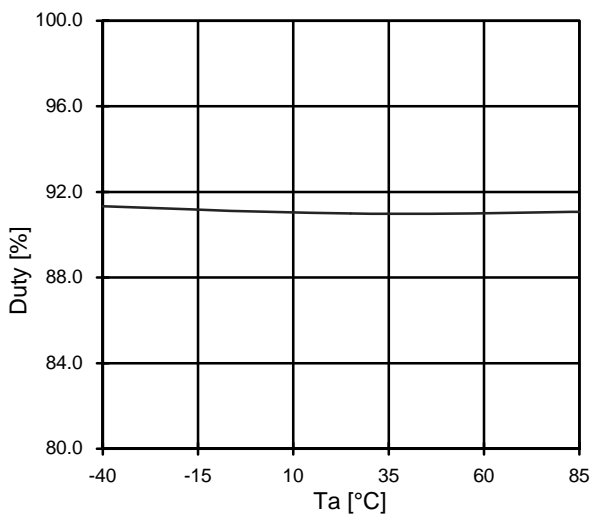


Figure 8. Max Duty - Temperature

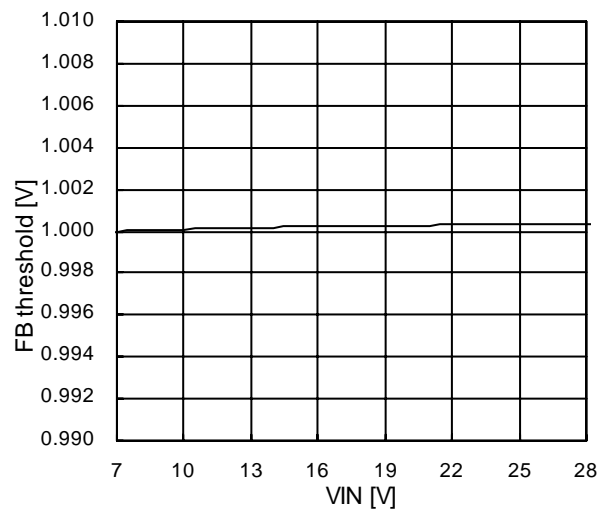


Figure 9. FB Pin Reference Voltage - Input Voltage

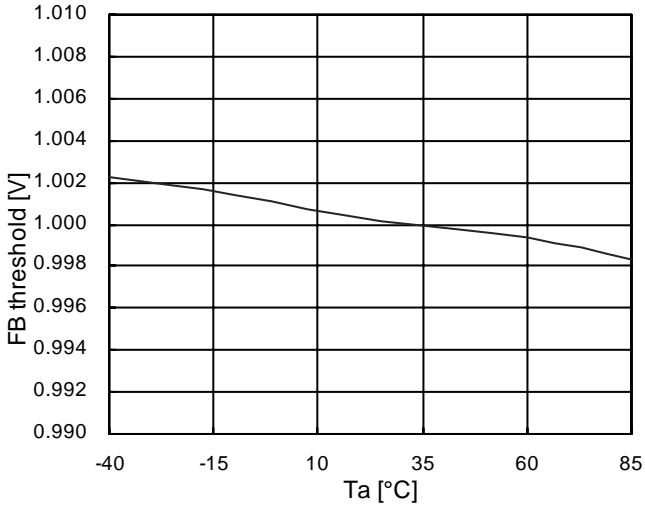


Figure 10. FB Pin Reference Voltage - Temperature

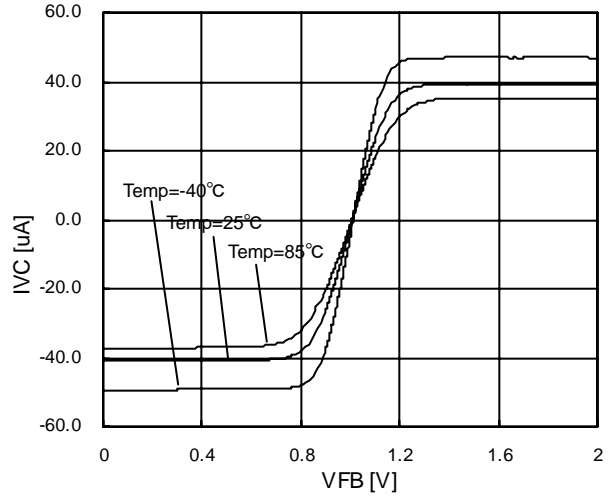


Figure 11. FB Pin Voltage – VC Pin Current

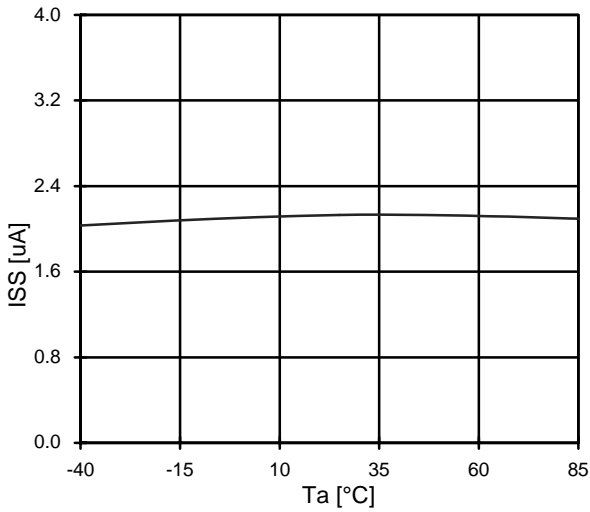


Figure 12. SS Pin Charge Current - Temperature

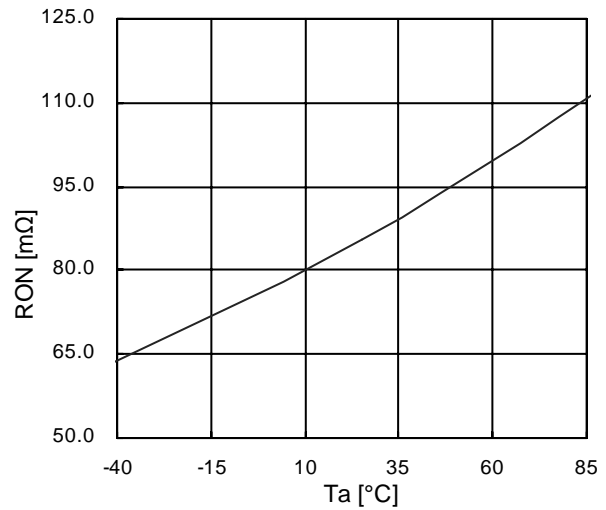


Figure 13. High-side FET Ron - Temperature

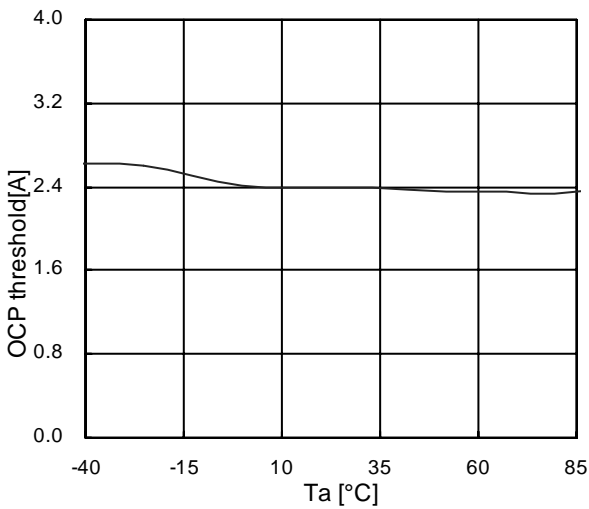


Figure 14. OCP Detect Current - Temperature

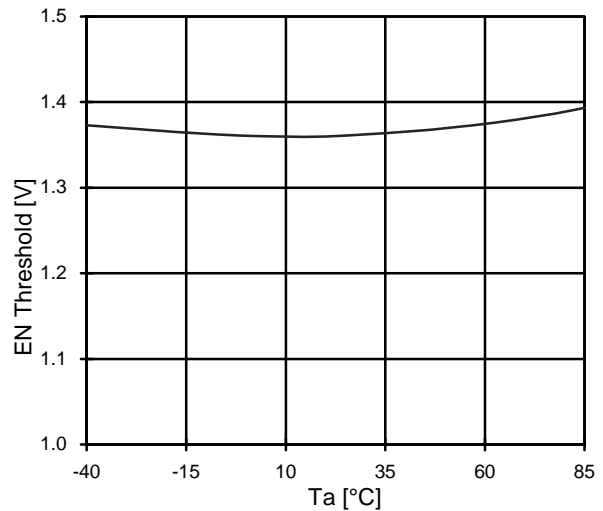
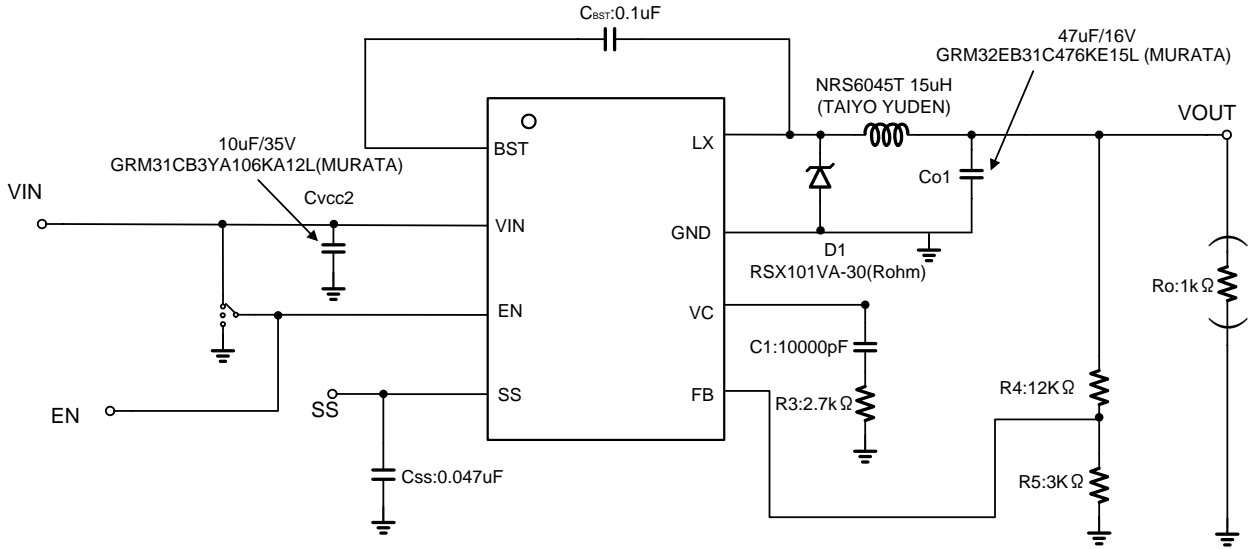


Figure 15. EN Threshold Voltage - Temperature

Reference Characteristics of typical Application Circuits (VIN=12V, VOUT=5V IOUT=1A)



(Back side PAD is recommended connecting to GND)

Figure 16. Typical Application Circuit (VOUT=5V)

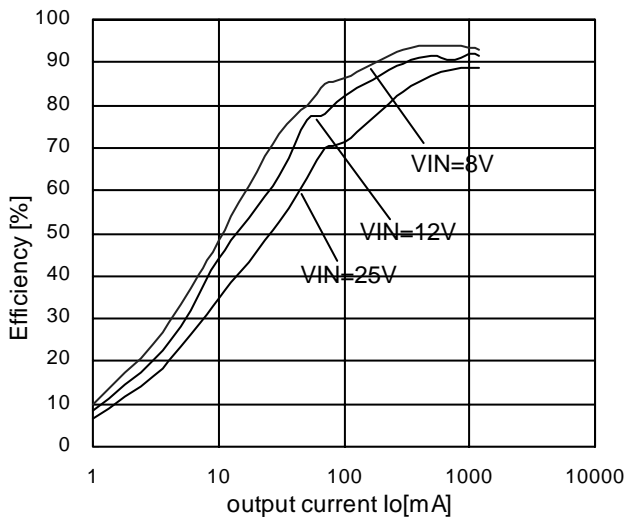


Figure 17. Efficiency - Output Current

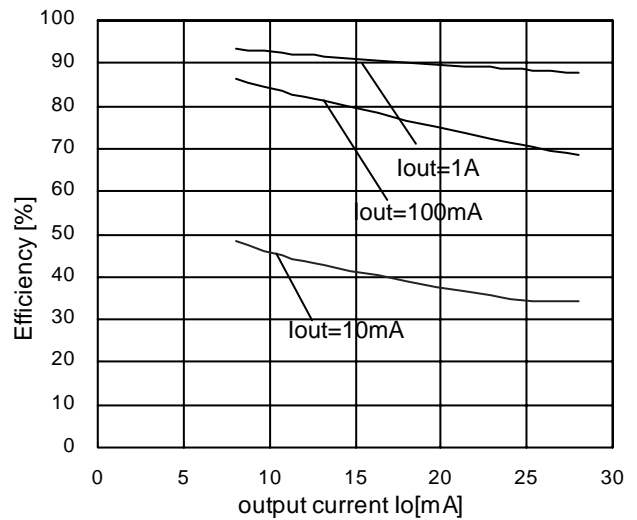


Figure 18. Efficiency - Input Voltage

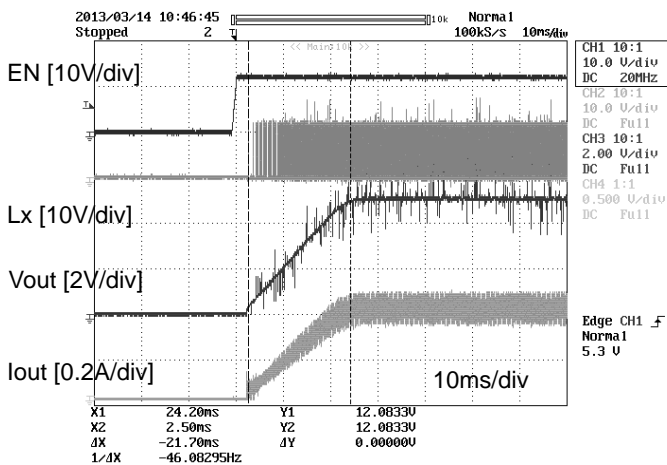


Figure 19. Start-up Characteristics

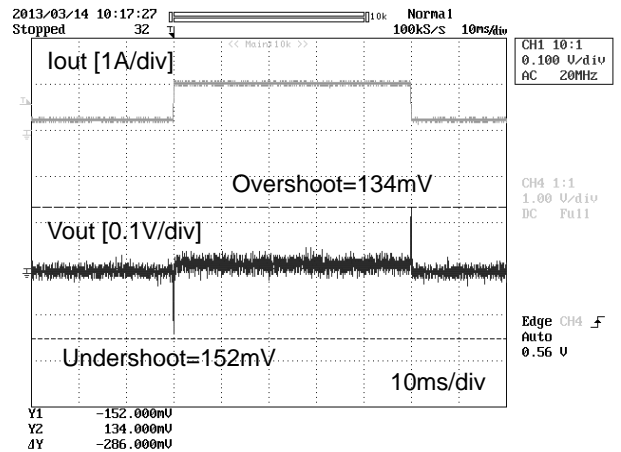


Figure 20. Load Response

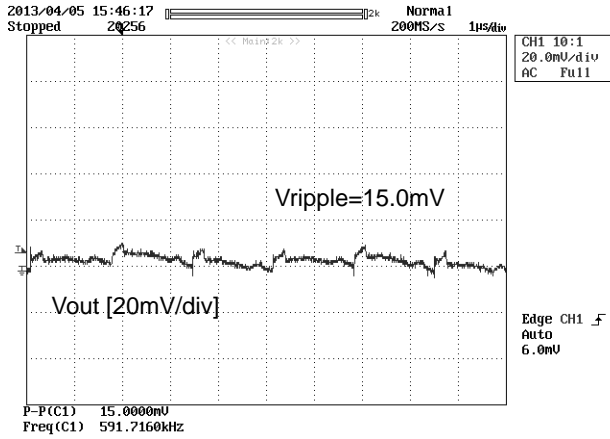


Figure 21. LX Switching/ Vout Ripple
 $I_o = 100\text{mA}$

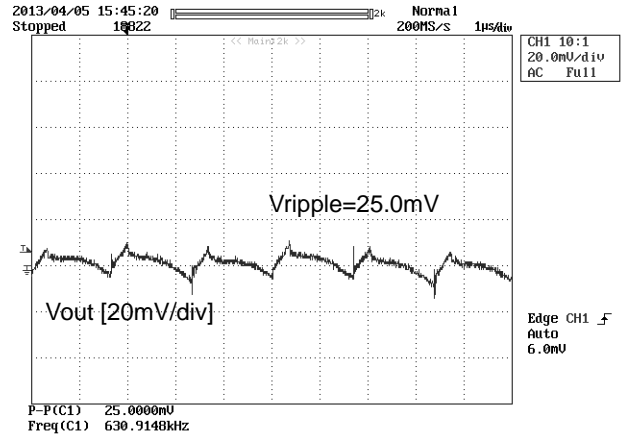


Figure 22. LX Switching/ Vout Ripple
 $I_o = 1\text{A}$

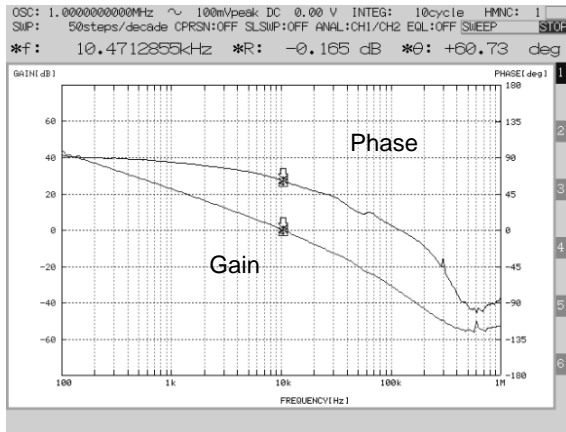


Figure 23. Frequency Response $I_o = 1\text{A}$

Application parts list 1
(VIN=12V, VOUT=5V IOU=1A)

Symbol	Value	Part name	Company	comments
[Capacitor]				
CVCC	10uF/35V	CRM31CB3YA106KA12L	MURATA	
CSS	0.047uF/25V	GRM155B31E473KA87	MURATA	
C1	10000pF/50V	GRM155B31H103KA88	MURATA	
CBST	0.1uF/10V	GRM155B31C104KA87	MURATA	
CO	47uF/16V	GRM32EB31C476KE15L	MURATA	
[Resistor]				
R3	2.7k Ω	MCR03 series	ROHM	
R4	12k Ω	MCR03 series	ROHM	
R5	3k Ω	MCR03 series	ROHM	
[Diode]				
D0	-	RSX101VA-30	ROHM	
[Inductor]				
L0	15uH	NRS6045T150	TAIYO YUDEN	

Application parts list 2 (When load current are light and make a point of total area)
(VIN=12V, VOUT=5V, IOU=300mA)

Symbol	Value	Part name	Company	comments
[Capacitor]				
CVCC	10uF/25V	GRM188R61E106MA73	MURATA	
CSS	0.047uF/25V	GRM155B31E473KA87	MURATA	
C1	22000pF/50V	GRM155B31H223KA12	MURATA	
CBST	0.1uF/10V	GRM155B31C104KA87	MURATA	
CO	22uF/10V	GRM21BB31A226ME51	MURATA	
[Resistor]				
R3	2.2k Ω	MCR006 series	ROHM	
R4	12k Ω	MCR006 series	ROHM	
R5	3k Ω	MCR006 series	ROHM	
[Diode]				
D0	-	RSX101VA-30	ROHM	
[Inductor]				
L0	15uH	DEM3518C series	TOKO	

Application Components Selection Method

(1) Inductors

Something of the shield type that fulfills the current rating (Current value Ipecac below), with low DCR is recommended. Value of Inductance influences Inductor Ripple Current and becomes the cause of Output Ripple. In the same way as the formula below, this Ripple Current can be made small for as big as the L value of Coil or as high as the Switching Frequency.

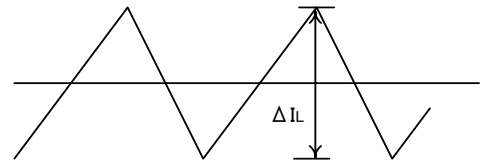


Figure 24. Inductor Current

$$I_{peak} = I_{OUT} + \frac{\Delta I_L}{2} \dots (1)$$

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f} \dots (2)$$

(ΔI_L : Output Ripple Current, V_{IN} : Input Voltage, V_{OUT} : Output Voltage, f : Switching Frequency)
 For design value of Inductor Ripple Current, please carry out design tentatively with about 20% ~ 50% of Maximum Input Current

(2) Output Capacitor

In order for capacitor to be used in output to reduce output ripple, Low ceramic capacitor of ESR is recommended. Also, for capacitor rating, on top of putting into consideration DC Bias characteristics, please use something whose maximum rating has sufficient margin with respect to the Output Voltage. Output ripple voltage is looked for using the following formula. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the crossover frequency of the design and LC corner frequency of the output filter. In general, it is desirable to keep the crossover frequency at less than 1/5 of the switching frequency. With high switching frequencies such as the 600kHz frequency of this design, internal circuit limitations of the BD9E151NUX limit the practical maximum crossover frequency to about 30kHz. In general, the crossover frequency should be higher than the corner frequency determined by the load impedance and the output capacitor. This limits the minimum capacitor value for the output filter to:

$$C_{OUT_min} = \frac{1}{2\pi \times R_l \times f_{c_max}} \dots (3)$$

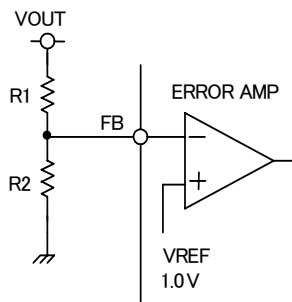
Where: R_l is the output load resistance and f_{c_max} is the maximum crossover frequency. The output ripple voltage can be estimated by:

$$V_{pp} = \Delta I_L \times \frac{1}{2\pi \times f \times C_{OUT}} + \Delta I_L \times R_{ESR} \dots (4)$$

Please design in a way that it is held within Capacity Ripple Voltage.
 In the BD9E151NUX, it is recommended a ceramic capacitor more than 10 μ F.

(3) Output Voltage Setting

ERROR AMP internal Standard Voltage is 1.0V. Output Voltage is determined as seen in (5) formula



$$V_{OUT} = \frac{R1 + R2}{R2} \dots (5)$$

Figure 25. Output Voltage Setting

(4) Bootstrap Capacitor

Please connect from 0.047 μ F to 0.47 μ F (Laminate Ceramic Capacitor) between BST Pin and LX Pin.

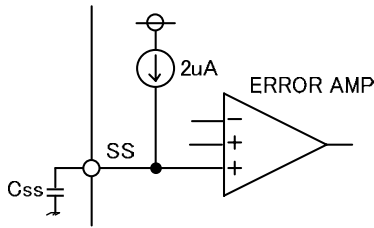
(5) Soft Start Function

Figure 26. Soft Start Time Setting

It is highly recommended to program the soft start time externally to prevent high inrush current because no soft start time is implemented internally. A capacitor (C_{SS}) connected between the SS pin and ground implements a soft start time. The BD9E151NUX has an internal pull-up current source of 2uA that charges the external soft start capacitor. The equation for the soft start time (10% to 90 %) is shown in below Equation. The I_{SS} current is 2uA.

$$T_{SS} = \frac{C_{SS} \times 0.1}{I_{SS}} \dots (6)$$

(6) Catch Diode

The BD9E151NUX is designed to operate using an external catch diode between LX and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the LX pin, which is $V_{INMAX} + 0.5$ V. Peak current must be greater than $I_{OUTMAX} + \frac{1}{2}I_L$ plus on half the peak to peak inductor current. Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses.

(7) Input Capacitor

The BD9E151NUX requires an input capacitor and depending on the application. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but low-ESR electrolytic capacitors may also suffice. The typical recommended value for the decoupling capacitor is 10uF. Please place this capacitor as possible as close to the VIN pin. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{CC} = \frac{I_{OUT}}{f \times C_{VCC}} \times \frac{V_{OUT}}{V_{CC}} \times \left[1 - \frac{V_{OUT}}{V_{CC}} \right] \dots (7)$$

Since the input capacitor (C_{VIN}) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CVCC} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{CC}} \times \left(1 - \frac{V_{OUT}}{V_{CC}} \right)} \dots (8)$$

The worst case condition occurs at $V_{IN} = 2V_{OUT}$, where

$$I_{CVCC_max} = \frac{I_{OUT}}{2} \dots (9)$$

(8) About Adjustment of DC/DC Comparator Frequency Characteristics

Role of Phase compensation element C1, C2, R3 (See P.8 Example of Reference Application Circuit)

Stability and Responsiveness of Loop are controlled through VC Pin which is the output of Error Amp.

The combination of zero and pole that determines Stability and Responsiveness is adjusted by the combination of resistor and capacitor that are connected in series to the VC Pin.

DC Gain of Voltage Return Loop can be calculated for using the following formula.

$$A_{dc} = R_I \times G_{cs} \times A_{EA} \times \frac{V_{FB}}{V_{out}} \dots (10)$$

Here, V_{FB} is Feedback Voltage (1.0V). A_{EA} is Voltage Gain of Error amplifier (typ : 60 dB),

G_{cs} is the Trans-conductance of Current Detect (typ : 10A/V), and R_I is the Output Load Resistance value.

There are 2 important poles in the Control Loop of this DC/DC.
The first occurs with through the output resistance of Phase compensation Capacitor (C1) and Error amplifier.
The other one occurs with through the Output Capacitor and Load Resistor.
These poles appear in the frequency written below.

$$fp1 = \frac{G_{EA}}{2\pi \times C1 \times A_{EA}} \quad \dots (11)$$

$$fp2 = \frac{1}{2\pi \times COUT \times RI} \quad \dots (12)$$

Here, G_{EA} is the trans-conductance of Error amplifier (typ : 250uA/V).

Here, in this Control Loop, one zero becomes important.
With the zero which occurs because of Phase compensation Capacitor C1 and Phase compensation Resistor R3, the Frequency below appears.

$$fz1 = \frac{1}{2\pi \times C1 \times R3} \quad \dots (13)$$

Also, if Output Capacitor is big, and that ESR (RESR) is big, in this Control Loop, there are cases when it has an important, separate zero (ESR zero).

This ESR zero occurs due to ESR of Output Capacitor and Capacitance, and exists in the Frequency below.

$$fz_{ESR} = \frac{1}{2\pi \times COUT \times RESR} \quad \dots (14) \quad (\text{ESR zero})$$

In this case, the 3rd pole determined with the 2nd Phase compensation Capacitor (C2) and Phase Correction Resistor (R3) is used in order to correct the ESR zero results in Loop Gain.

This pole exists in the frequency shown below.

$$fp3 = \frac{1}{2\pi \times C2 \times R3} \quad \dots (15) \quad (\text{pole that corrects ESR zero})$$

The target of Phase compensation design is to create a communication function in order to acquire necessary band and Phase margin.

Cross-over Frequency (band) at which Loop gain of Return Loop becomes "0" is important.

When Cross-over Frequency becomes low, Power supply Fluctuation Response, Load Response, etc worsens.

On the other hand, when Cross-over Frequency is too high, instability of the Loop can occur.

Tentatively, Cross-over Frequency is targeted to be made 1/20 or below of Switching Frequency. Selection method of Phase Compensation constant is shown below.

1. Phase Compensation Resistor (R3) is selected in order to set to the desired Cross-over Frequency.
Calculation of RC is done using the formula below.

$$R3 = \frac{2\pi \times COUT \times fc}{G_{EA} \times G_{CS}} \times \frac{V_{out}}{V_{FB}} \quad \dots (16)$$

Here, fc is the desired Cross-over Frequency. It is made about 1/20 and below of the Normal Switching Frequency (f_s).

2. Phase compensation Capacitor (C1) is selected in order to achieve the desired phase margin.
In an application that has a representative Inductance value (about several 10uH ~ 22uH), by matching zero of compensation to 1/4 and below of the Cross-over Frequency, sufficient Phase margin can be acquired. C1 can be calculated using the following formula.

$$C1 > \frac{4}{2\pi \times R3 \times fc} \quad \dots (17)$$

RC is Phase compensation Resistor.

3. Examination whether the second Phase compensation Capacitor C2 is necessary or not is done. If the ESR zero of Output Capacitor exists in a place that is smaller than half of the Switching Frequency, a second Phase compensation Capacitor is necessary. In other words, it is the case wherein the formula below happens.

$$\frac{1}{2\pi \times COUT \times RESR} < \frac{fs}{2} \dots (18)$$

In this case, add the second Phase compensation Capacitor C2, and match the frequency of the third pole to the Frequency fp3 of ESR zero.

C2 is looked for using the following formula.

$$C2 = \frac{COUT \times RESR}{R3} \dots (19)$$

Output Voltage Restriction

BD9E151NUX have a function of BSTUVLO to prevent malfunction at low voltage between BST and LX. Therefore OUTPUT voltage is restricted by BSTUVLO and Max Duty Cycle (min 85 %).

① Restriction by BST-UVLO

When the voltage between BST and Lx is lower than 2.5V, High-Side FET will be made turned off and the charge will provide from VIN to BST directly to reset BSTUVLO (path①). The below formula is needed to be satisfied to reset BSTUVLO.

$$VIN \geq VOUT + VF + BSTUVLO \text{ reset} \dots (20)$$

Here, BSTUVLO reset: BSTUVLO reset voltage, VF: the diode forward bias voltage between VIN and BST
Considering the fluctuation of BSTUVLO reset voltage and VF, maximum voltage is more than 5V.
Therefore maximum output voltage is defined as VIN - 5V.

② Restriction by Max Duty Cycle

Maximum output voltage is restricted by Max Duty Cycle (min85%).
In this time it is needed to consider the effect of NchFET Ron , OUTPUT current and forward voltage of SBD. OUTPUT voltage can be calculated using the following formula.

$$VOUT_{max} = (VIN - Ron \times IOUT) \times 0.85 - VF \times 0.15 \dots (21)$$

Considering the effect of catch diode type and the loss by inductor,
Vomax = (VIN-Ron×Iomax)×0.85 (casually formula)

Considering the negative voltage in the case of pulling diode current,
maximum voltage is more than VIN×0.7.

Therefore maximum output voltage is defined as VIN×0.7.

Considering above restriction, adopt the lower output voltage as maximum voltage

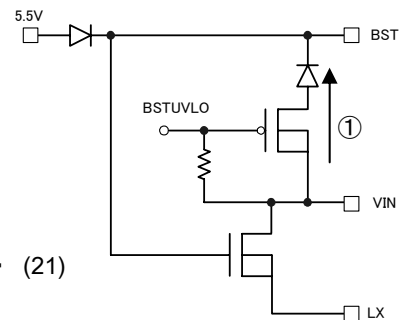


Figure 27. BST charge pass

Cautions on PCB board layout

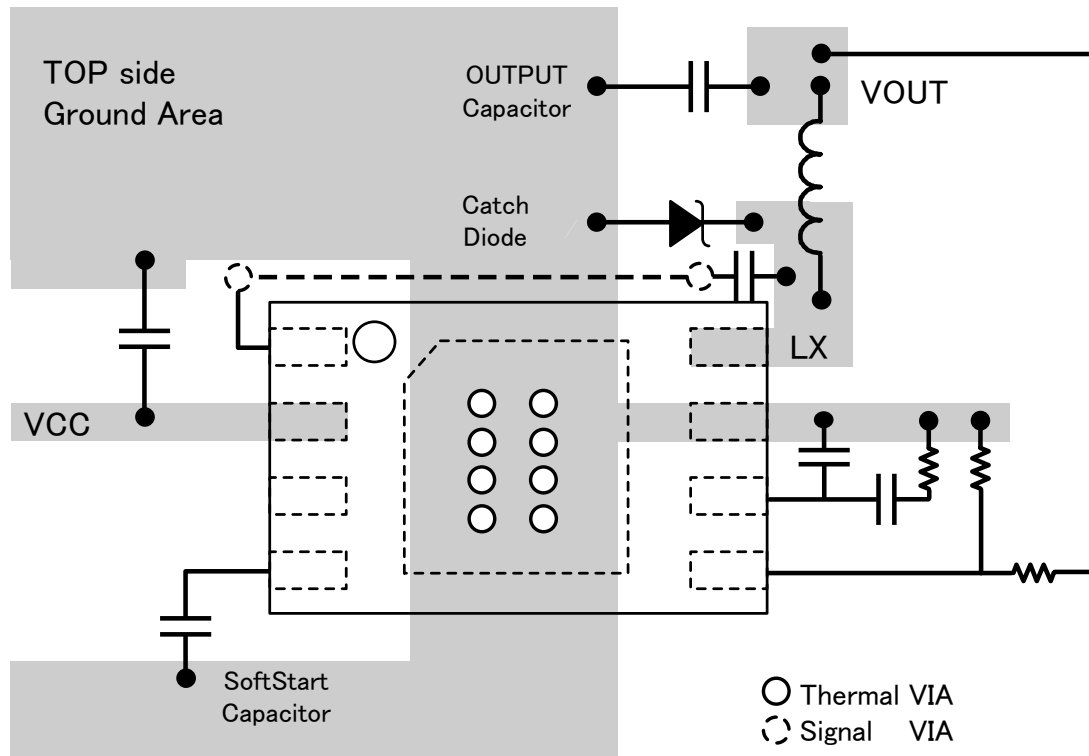


Figure 28. Reference PCB layout

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with B dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. See Fig.28 for a PCB layout example.

In the BD9E151NUX, since the LX connection is the switching node, the catch diode and output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. And GND area should not be connected directly power GND, connected avoiding the high current switch paths. The additional external components can be placed approximately as shown.

Power Dissipation

It is shown below reducing characteristics of power dissipation to mount 70mm×70mm×1.6mm^t PCB

Junction temperature must be designed not to exceed 150°C.

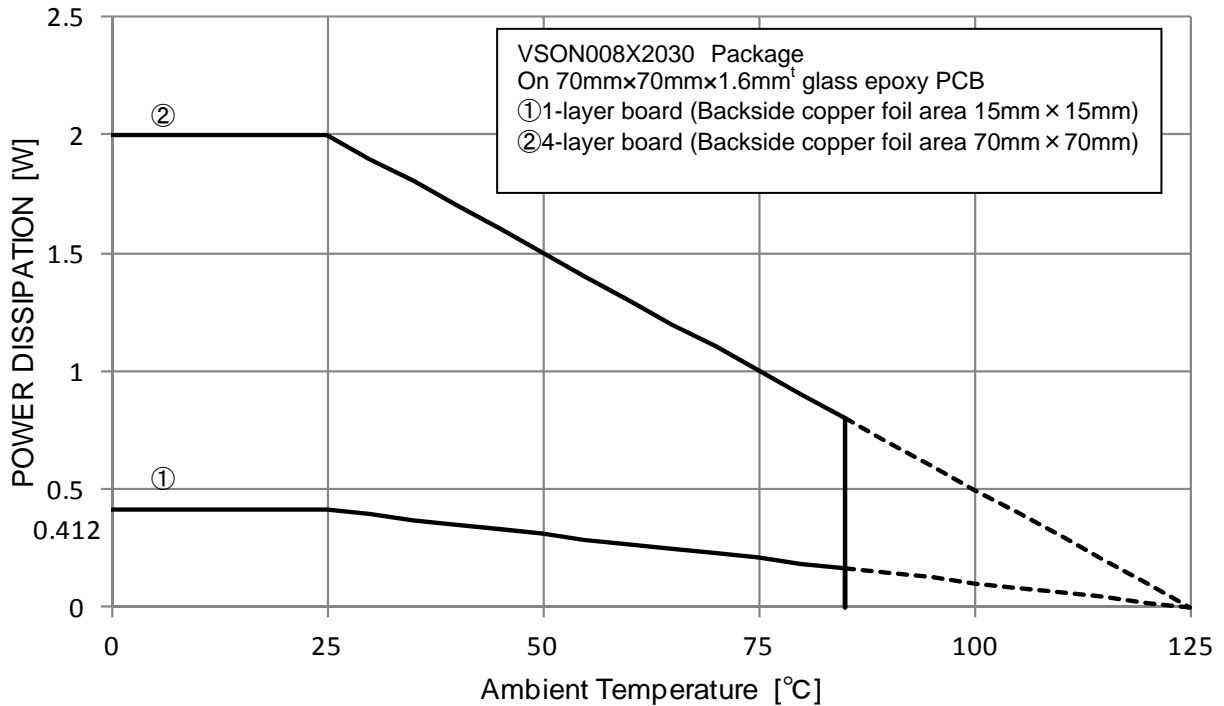


Figure 29. Power Dissipation (70mm × 70mm × 1.6mm^t 1layer PCB)

Power Dissipation Estimate

The following formulas show how to estimate the device power dissipation under continuous mode operations. They should not be used if the device is working in the discontinuous conduction mode.

The device power dissipation includes:

- 1) Conduction loss : $P_{con} = I_{OUT}^2 \times R_{onH} \times V_{OUT}/V_{IN}$
- 2) Switching loss: $P_{sw} = 0.25 \times 10^{-9} \times V_{IN}^2 \times I_{OUT} \times f_{sw}$
- 3) Gate charge loss : $P_{gc} = 22.8 \times 10^{-9} \times f_{sw}$
- 4) Quiescent current loss : $P_q = 0.7 \times 10^{-3} \times V_{IN}$

Where:

I_{OUT} is the output current (A) , R_{onH} is the on-resistance of the high-side MOSFET (Ω) , V_{OUT} is the output voltage (V).
 V_{IN} is the input voltage (V), f_{sw} is the switching frequency (Hz).

Therefore

Power dissipation of IC is the sum of above dissipation.

$$P_d = P_{con} + P_{sw} + P_{gc} + P_q$$

$$\text{For given } T_j, T_j = T_a + \theta_{ja} \times P_d$$

Where:

P_d is the total device power dissipation (W), T_a is the ambient temperature (°C)

T_j is the junction temperature (°C), θ_{ja} is the thermal resistance of the package (°C)

I/O equivalent circuit

Pin. No	Pin Name	Pin Equivalent Circuit	Pin. No	Pin Name	Pin Equivalent Circuit
1 2 7 8	BST VIN GND LX		5	FB	
3	EN		6	VC	
4	SS				

Notes for use

- (1) About Absolute Maximum Rating
When the absolute maximum ratings of application voltage, operating temperature range, etc. was exceeded, there is possibility of deterioration and destruction. Also, the short Mode or open mode, etc. destruction condition cannot be assumed. When the special mode where absolute maximum rating is exceeded is assumed, please give consideration to the physical safety countermeasure for the fuse, etc.
- (2) About GND Electric Potential
In every state, please make the electric potential of GND Pin into the minimum electrical potential. Also, include the actual excessive effect, and please do it such that the pins, excluding the GND Pin do not become the voltage below GND.
- (3) About Heat Design
Consider the Power Dissipation (Pd) in actual state of use, and please make Heat Design with sufficient margin.
- (4) About short circuit between pins and erroneous mounting
When installing to set board, please be mindful of the direction of the IC, phase difference, etc. If it is not installed correctly, there is a chance that the IC will be destroyed. Also, if a foreign object enters the middle of output, the middle of output and power supply GND, etc., even for the case where it is shorted, there is a change of destruction.
- (5) About the operation inside a strong electro-magnetic field
When using inside a strong electro-magnetic field, there is a possibility of error, so please be careful.
- (6) Temperature Protect Circuit (TSD Circuit)
Temperature Protect Circuit (TSD Circuit) is built-in in this IC. As for the Temperature Protect Circuit (TSD Circuit), because it a circuit that aims to block the IC from insistent careless runs, it is not aimed for protection and guarantee of IC. Therefore, please do not assume the continuing use after operation of this circuit and the Temperature Protect Circuit operation.
- (7) About checking with Set boards
When doing examination with the set board, during connection of capacitor to the pin that has low impedance, there is a possibility of stress in the IC, so for every 1 process, please make sure to do electric discharge. As a countermeasure for static electricity, in the process of assembly, do grounding, and when transporting or storing please be careful. Also, when doing connection to the jig in the examination process, please make sure to turn off the power supply, then connect. After that, turn off the power supply then take it off.
- (8) About common impedance
For the power supply and the wire of GND, lower the common impedance, then, as much as possible, make the ripple smaller (as much as possible make the wire thick and short, and lower the ripple from $L \cdot C$), etc. then and please consider it sufficiently.
- (9) In the application, when the mode where the VIN and each pin electrical potential becomes reversed exists, there is a possibility that the internal circuit will become damaged. For example, during cases wherein the condition when charge was given in the external capacitor, and the VIN was shorted to GND, it is recommended to insert the bypass diode to the diode of the back current prevention in the VIN series or the middle of each Pin-VIN (fig.30).
- (10) About IC Pin Input
This IC is a Monolithic IC, and between each element, it has P⁺ isolation for element separation and P board. With the N layer of each element and this, the P-N junction is formed, and the parasitic element of each type is composed.
For example, like the fig.31, when resistor and transistor is connected to Pin,
 - When GND > (PinA) in Resistor, when GND > (PinA), when GND > (PinB) in Transistor (NPN), the P-N junction will operate as a parasitic diode.
 - Also, during GND > (Pin B) in the Transistor (NPN), through the N layer of the other elements connected to the above-mentioned parasitic diode, the parasitic NPN Transistor will operation.
 On the composition of IC, depending on the electrical potential, the parasitic element will become necessary. Through the operation of the parasitic element interference of circuit operation will arouse, and error, therefore destruction can be caused. Therefore please be careful about the applying of voltage lower than the GND (P board) in I/O Pin, and the way of using when parasitic element operating.

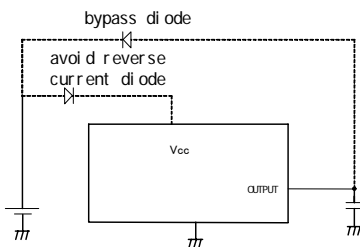


Figure 30. Example of insert diode

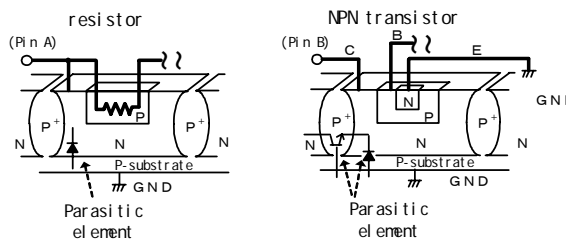
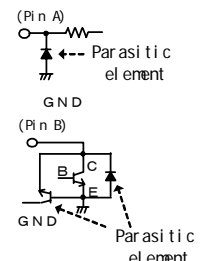
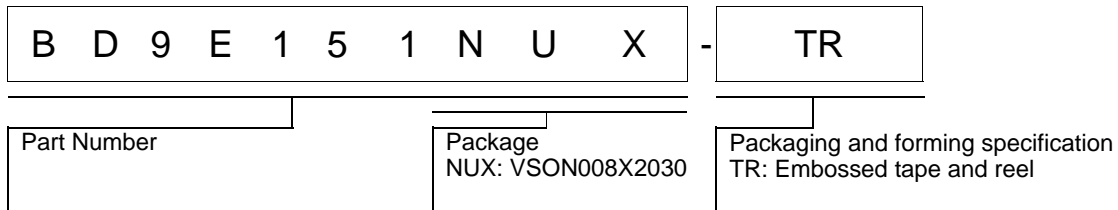


Figure 31. Example of simple structure of Monolithic IC

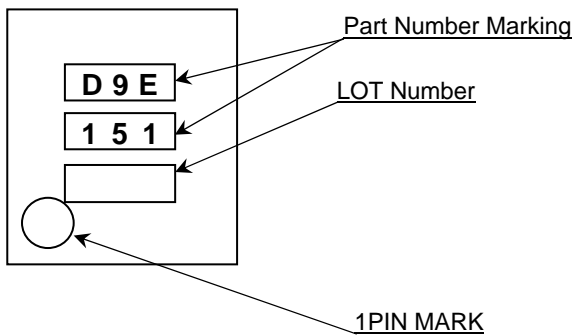


Physical Dimension Tape and Reel Information

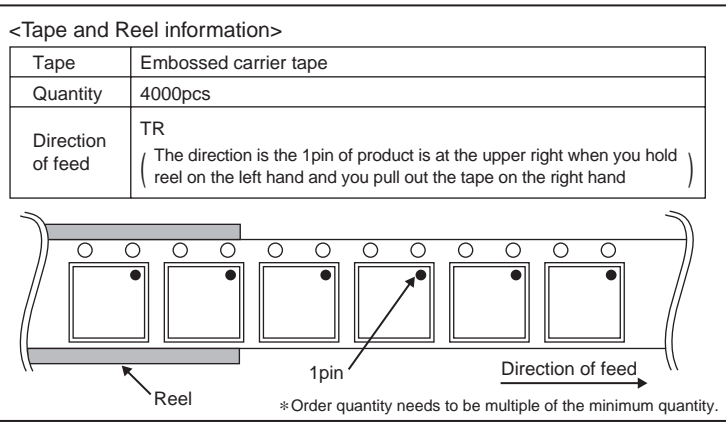
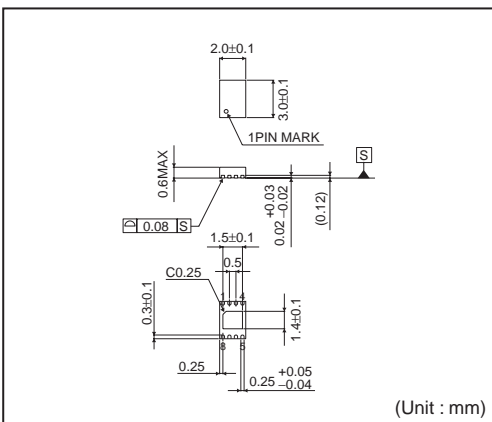


●Marking Diagram

VSON008X2030 (TOP VIEW)



VSON008X2030



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CLASS IV		CLASS III	

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 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
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