

## Synchronous Rectification N-Channel MOSFET Driver for DC/DC Conversion

### DESCRIPTION

SiP41103 is a high-speed synchronous rectification MOSFET driver with adaptive shoot-through protection for use in high frequency, high-current, multiphase DC-DC synchronous rectifier buck converter. It is designed to operate at the switching frequencies up to 1 MHz. The high-side driver is bootstrapped to allow driving N-Channel MOSFET. Adaptive shoot-through protection prevents simultaneous conduction of external MOSFETs. Adding a capacitor to the delay pin can further increase the high-side driver turn-on delay by 1.2 ns/pF for further shoot-through protection.

The SiP41103 is available in both standard and lead (Pb)-free 10-Pin MLP33 packages and is specified to operate over the industrial temperature range of -40 °C to 85 °C.

### FEATURES

- 5 V Gate Drive
- Undervoltage Lockout
- Internal Bootstrap Diode
- Adaptive Shoot-Through Protection
- Synchronous MOSFET Disable
- Adjustable Highside Propagation Delay
- Switching Frequency Up to 1 MHz
- Drive MOSFETs In 4.5 to 50 V Systems

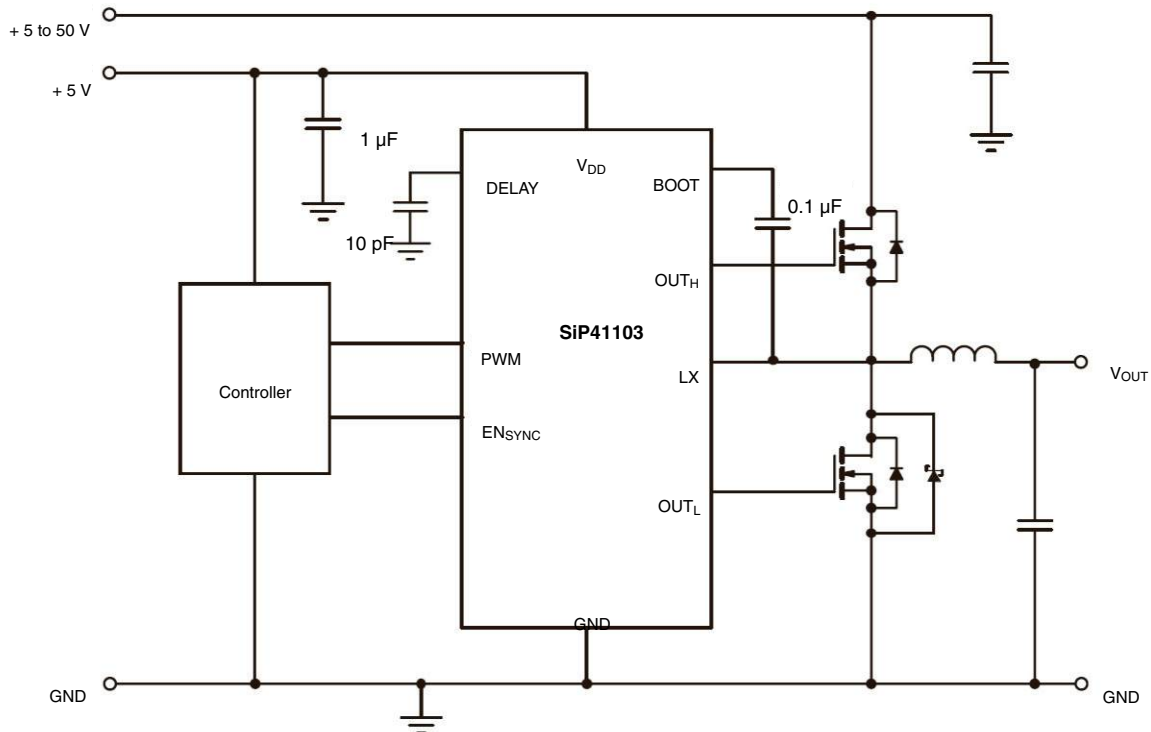


**RoHS\***  
COMPLIANT

### APPLICATIONS

- Multi-Phase DC/DC Conversion
- High Current Synchronous Buck Converters
- High Frequency Synchronous Buck Converters
- Asynchronous-to-Synchronous Adaptations
- Mobile Computer DC/DC Converters
- Desktop Computer DC/DC Converters

### TYPICAL APPLICATION CIRCUIT



\*Pb containing terminations are not RoHS compliant, exemptions may apply

<b>ABSOLUTE MAXIMUM RATINGS</b> (All voltages referenced to GND = 0 V)			
Parameter		Limit	Unit
$V_{DD}$ , PWM, $EN_{SYNC}$ , DELAY		7	V
LX, BOOT		55	
BOOT to LX		7	
Storage Temperature		- 40 to 150	°C
Operating Junction Temperature		125	
Power Dissipation <sup>a,b</sup>	MLP-33	960	mW
Thermal Impedance( $\Theta_{JA}$ ) <sup>a,b</sup>		105	°C/W

Notes:

a. Device mounted with all leads soldered or welded to PC board

b. Derate 9.6 mW/°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

<b>RECOMMENDED OPERATING RANGE</b> (All voltages referenced to GND = 0 V)			
Parameter		Limit	Unit
$V_{DD}$		4.5 to 5.5	V
$V_{BOOT}$		4.5 to 50	
$C_{BOOT}$		100 nF to 1 $\mu$ F	
Operating Temperature Range		- 40 to 85	°C

<b>SPECIFICATIONS<sup>a</sup></b>						
Parameter	Symbol	Test Conditions Unless Specified $V_{DD} = 5\text{ V}$ , $V_{BOOT} - V_{LX} = 5\text{ V}$ , $C_{LOAD} = 3\text{ nF}$ $T_A = -40\text{ to }85\text{ }^\circ\text{C}$	Limits			Unit
			Min <sup>a</sup>	Typ <sup>b</sup>	Max <sup>a</sup>	
<b>Power Supplies</b>						
Supply Voltage	$V_{DD}$		4.5		5.5	V
Quiescent Current	$I_{DDQ}$	$f_{PWM} = 1\text{ MHz}$ , $C_{LOAD} = 0$		2.3	3.0	mA
Shutdown Current	$I_{SD1}$	PWM = 0 V			1	$\mu$ A
	$I_{SD2}$	PWM = 5 V		30	60	
<b>Reference Voltage</b>						
Break-Before-Make	$V_{BBM}$	LX Falling		1		V
<b>PWM Input</b>						
Input High	$V_{IH}$		4.0		$V_{DD}$	V
Input Low	$V_{IL}$				0.5	
Bias Current	$I_B$			$\pm 0.3$	$\pm 1$	$\mu$ A
<b><math>EN_{SYNC}</math> Inputs</b>						
Input High	$V_{IH}$		2.0		$V_{DD}$	V
Input Low	$V_{IL}$				1.0	
Bias Current	$I_B$				$\pm 1$	$\mu$ A
<b>High-Side Undervoltage Lockout</b>						
Threshold	$V_{UVHS}$	Rising or Falling	2.5	3.35	3.75	V
<b>Bootstrap Diode</b>						
Forward Voltage	$V_F$	$I_F = 10\text{ mA}$ , $T_A = 25\text{ }^\circ\text{C}$	0.7	0.76	0.82	V

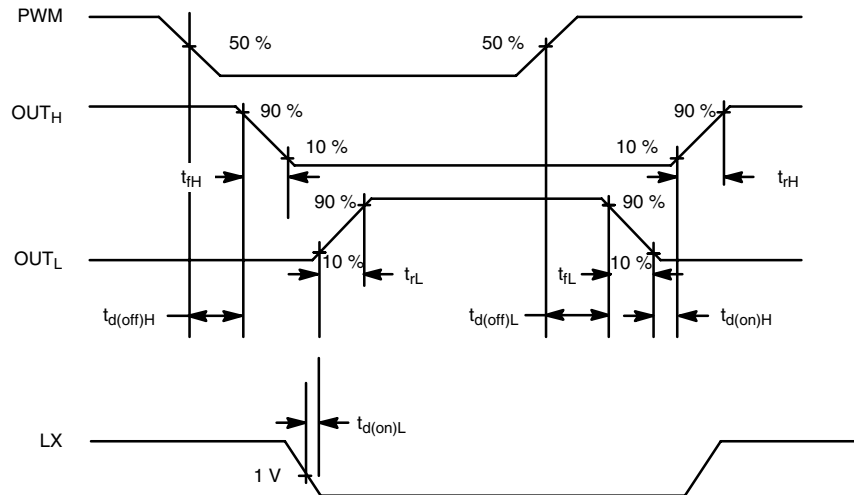


<b>SPECIFICATIONS<sup>a</sup></b>						
Parameter	Symbol	Test Conditions Unless Specified $V_{DD} = 5\text{ V}$ , $V_{BOOT} - V_{LX} = 5\text{ V}$ , $C_{LOAD} = 3\text{ nF}$ $T_A = -40\text{ to }85\text{ }^\circ\text{C}$	Limits			Unit
			Min <sup>a</sup>	Typ <sup>b</sup>	Max <sup>a</sup>	
<b>MOSFET Drivers</b>						
High-Side Drive Current <sup>c</sup>	$I_{PKH(source)}$			0.9		A
	$I_{PKH(sink)}$			1.1		
Low-Side Drive Current <sup>c</sup>	$I_{PKL(source)}$			0.8		
	$I_{PKL(sink)}$			1.5		
High-Side Driver Impedance	$R_{DH(source)}$			2.5	3.8	$\Omega$
	$R_{DH(sink)}$			2.2	3.3	
Low-Side Driver Impedance	$R_{DL(source)}$			3.4	5.1	
	$R_{DL(sink)}$			1.4	2.1	
High-Side Rise Time	$t_{rH}$	10 % - 90 %		32	40	ns
High-Side Fall Time	$t_{fH}$	90 % - 10 %		36	45	
High-Side Propagation Delay <sup>c</sup>	$t_{d(off)H}$	See Timing Waveforms		20		
	$t_{d(on)H}$	See Timing Waveforms		30		
Low-Side Rise Time	$t_{rL}$	10 % - 90 %		45	55	
Low-Side Fall Time	$t_{fL}$	90 % - 10 %		20	30	
Low-Side Propagation Delay <sup>c</sup>	$t_{d(off)L}$	See Timing Waveforms		30		
	$t_{d(on)L}$	See Timing Waveforms		30		
<b>LX Timer</b>						
LX Falling Timeout <sup>c</sup>	$t_{LX}$			420		ns
<b>V<sub>DD</sub> Undervoltage Lockout</b>						
Threshold Rising	$V_{UVLOR}$			4.3	4.5	V
Threshold Falling	$V_{UVLOF}$		3.7	4.1		
Hysteresis				0.4		
Power on Reset Time <sup>c</sup>				2.5		ms
<b>Thermal Shutdown</b>						
Temperature	$T_{SD}$	Temperature Rising		165		$^\circ\text{C}$
Hysteresis	$T_H$	Temperature Falling		25		

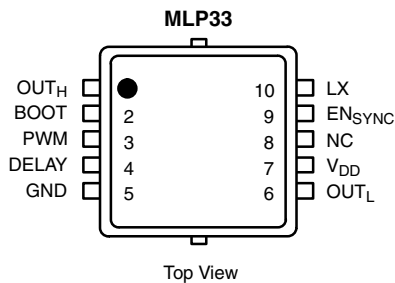
Notes:

- a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum (-40° to 85 °C).
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing and are measured at  $V_{CC} = 5\text{ V}$  unless otherwise noted.
- c. Guaranteed by design.

## TIMING WAVEFORMS



## PIN CONFIGURATION AND TRUTH TABLE



### TRUTH TABLE<sup>a</sup>

PWM	EN <sub>SYNC</sub>	OUT <sub>H</sub>	OUT <sub>L</sub>
L	L	L	L
L	H	L	H
H	X	H	L

Note:

a. After the device is enabled.

## ORDERING INFORMATION

Standard Part Number	Lead (Pb)-Free Part Number	Temperature Range	Marking
SiP41103DM-T1	SiP41103DM-T1-E3	- 40 to 85 °C	41A3

Eval Kit	Temperature Range
SiP41103DB	- 40 to 85 °C

## PIN DESCRIPTION

Pin Number	Name	Function
1	OUT <sub>H</sub>	High-side MOSFET gate drive
2	BOOT	Bootstrap supply for high-side driver. A capacitor connects between BOOT and LX
3	PWM	Input signal for the MOSFET drivers
4	DELAY	Connection for the highside dealy adjustment capacitors
5	GND	Ground
6	OUT <sub>L</sub>	Synchronous or low-side MOSFET gate drive
7	V <sub>DD</sub>	+ 5 V supply
8	NC	No Connect
9	EN <sub>SYNC</sub>	Enables OUT <sub>L</sub> , the driver for the synchronous MOSFET
10	LX	Connection for source of high-side MOSFET, drain of the low-side MOSFET and the inductor

**FUNCTIONAL BLOCK DIAGRAM**

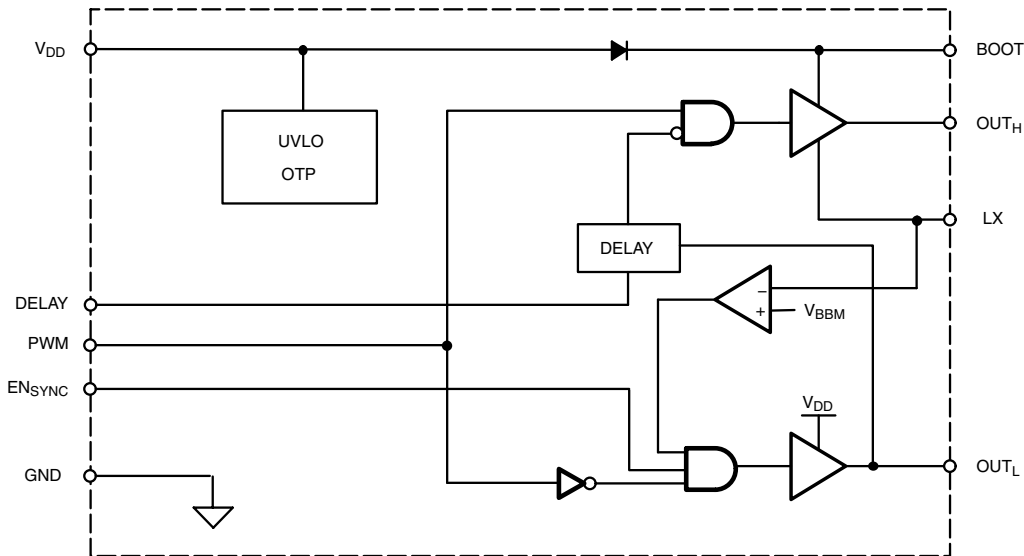


Figure 1.

**DETAILED OPERATION**

**PWM**

The PWM pin controls the switching of the external MOSFETs. The driver logic operates in a noninverting configuration. The PWM input stage should be driven by a signal with fast transition times, like those provided by a PWM controller or logic gate, (< 200 ns). The PWM input functions as a logic input and is not intended for applications where a slow changing input voltage is used to generate a switching output when the input switching threshold voltage is reached.

**Enable**

The device is enabled by edge sensing of transitions on PWM, high or low. A minimum PWM frequency of 2 kHz is required to keep the device enabled. When continuous PWM transitions are present, and after power-on reset time has elapsed, OUT<sub>H</sub> and OUT<sub>L</sub> will become active.

**Low-Side Driver**

The supplies for the low-side driver are V<sub>DD</sub> and GND. During shutdown, OUT<sub>L</sub> is held low.

**High-Side Driver**

The high-side driver is isolated from the substrate to create a floating high-side driver so that an N-Channel MOSFET can be used for the high-side switch. The supplies for the high-side driver are BOOT and LX. The voltage is supplied by a floating bootstrap capaci-

tor, which is continually recharged by the switching action of the output. During shutdown OUT<sub>H</sub> is held low.

**Bootstrap Circuit**

The internal bootstrap diode and a bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode replaces the external Schottky diode and bootstrap only a capacitor is necessary to complete the circuit. The bootstrap capacitor is sized according to:

$$C_{BOOT} = (Q_{Gate} / \Delta V_{BOOT-LX}) \times 10$$

where Q<sub>GATE</sub> is the gate charge needed to turn on the high-side MOSFET and ΔV<sub>BOOT-LX</sub> is the amount of droop allowed in the bootstrap supply voltage when the high-side MOSFET is driven high. The bootstrap capacitor value is typically 0.1 μF to 1 μF. The bootstrap capacitor voltage rating must be greater than V<sub>DD</sub> + 5 V to withstand transient spikes and ringing.

**Shoot-Through Protection**

The external MOSFETs are prevented from conducting at the same time during transitions. Break-before-make circuits monitor the voltages on the LX pin and the OUT<sub>L</sub> pin and control the switching as follows: When the signal on PWM goes low, OUT<sub>H</sub> will go low after an internal propagation delay. After the voltage

on LX falls below 1 V by the inductor action, the low-side driver is enabled and  $OUT_L$  goes high after some delay. When the signal on PWM goes high,  $OUT_L$  will go low after an internal propagation delay. After the voltage on  $OUT_L$  drops below 1 V the high-side driver is enabled  $OUT_H$  will go high after an internal propagation delay. If LX does not drop below 1 V within 400 ns after  $OUT_H$  goes low,  $OUT_L$  is forced high until the next PWM transition.

### Delay

The addition of a capacitor between DELAY and GND will increase the propagation delay time for  $OUT_H$  going high. Delay capacitance may be added to prevent shoot-through current in the low-side MOSFET due to the finite time between  $OUT_L$  going low and the continuing conduction of the low-side MOSFET. Choose a MOSFET with lower gate resistance to reduce this effect. If necessary, choose a capacitor value that prevents MOSFET conduction under worst-case temperature and manufacturing conditions. Propagation delay is increased according to the ratio of 1.2 ns/pF.

### Synchronous MOSFET Enable

Under light load conditions, efficiency can be increased by disabling the synchronous MOSFET, thus avoiding the gate charge losses of the synchronous MOSFET. When  $EN_{SYNC}$  is low,  $OUT_L$  is forced

low. When high, the low-side driver operates normally.  $EN_{SYNC}$  should be driven by a 5-V signal.

### Shutdown

The driver enters shutdown mode when a period of inactivity on PWM elapses. Shutdown current is less than 1  $\mu$ A.

### $V_{DD}$ Bypass Capacitor

MOSFET drivers draw large peak currents from the supplies when they switch. A local bypass capacitor is required to supply this current and reduce power supply noise. Connect a 1  $\mu$ F ceramic capacitor as close as practical between the  $V_{DD}$  and GND pins.

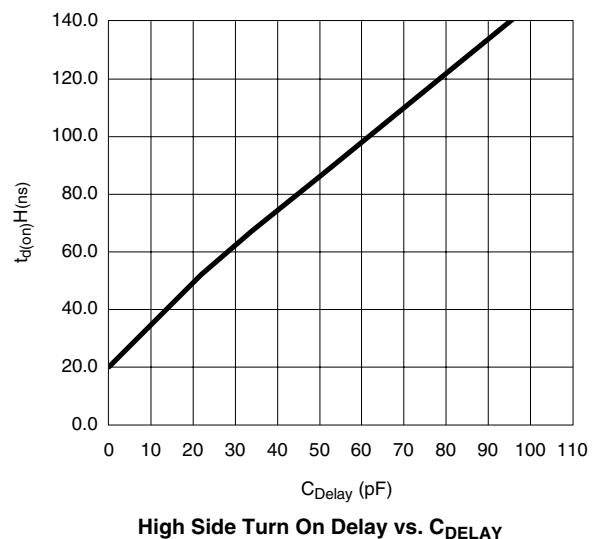
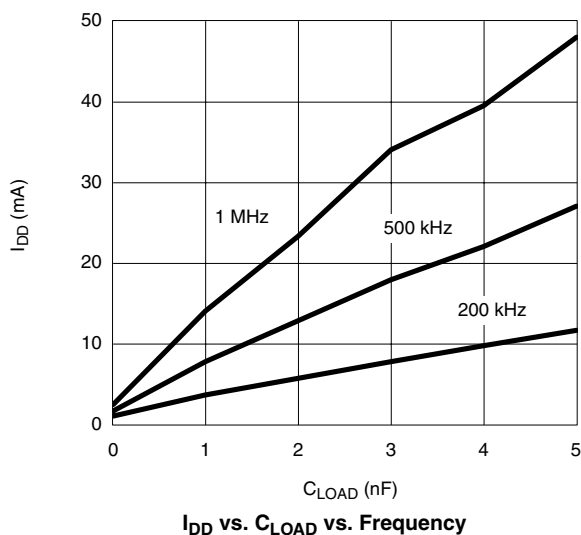
### Undervoltage Lockout

Undervoltage lockout prevents control of the circuit until the supply voltages reach valid operating levels. The UVLO circuit forces  $OUT_L$  and  $OUT_H$  to low when  $V_{DD}$  is below its specified voltage. A separate UVLO forces  $OUT_H$  low when the voltage between BOOT and LX is below the specified voltage.

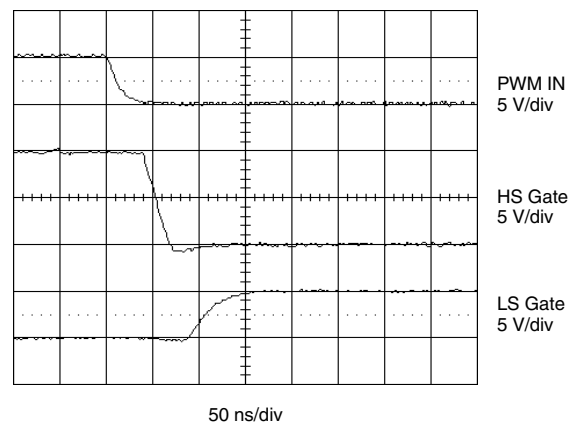
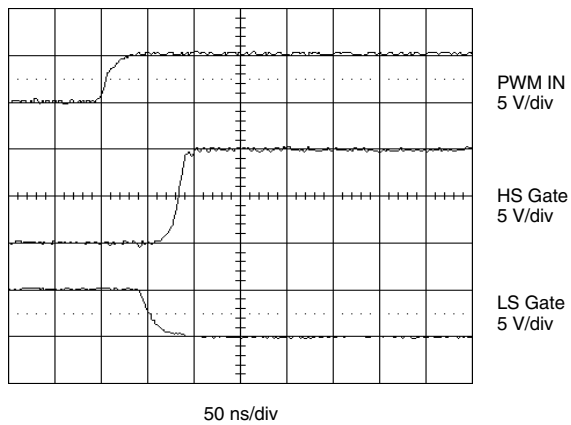
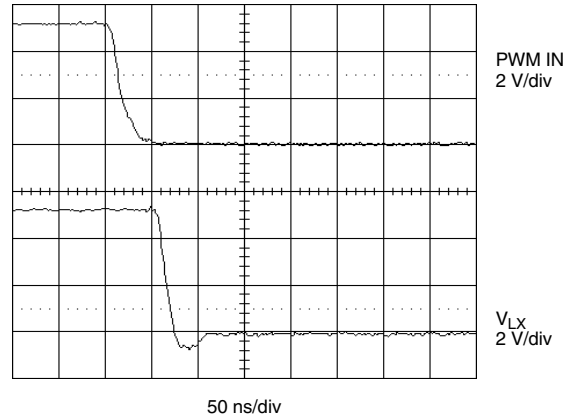
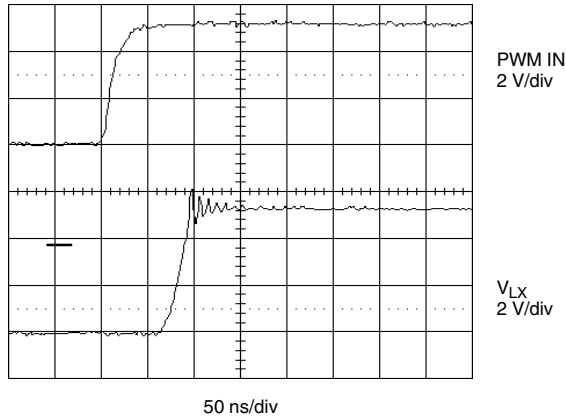
### Thermal Protection

If the temperature rises above 165  $^{\circ}$ C, the thermal protection disables the drivers. The drivers are re-enabled after the temperature has decreased below 140  $^{\circ}$ C.

## TYPICAL CHARACTERISTICS

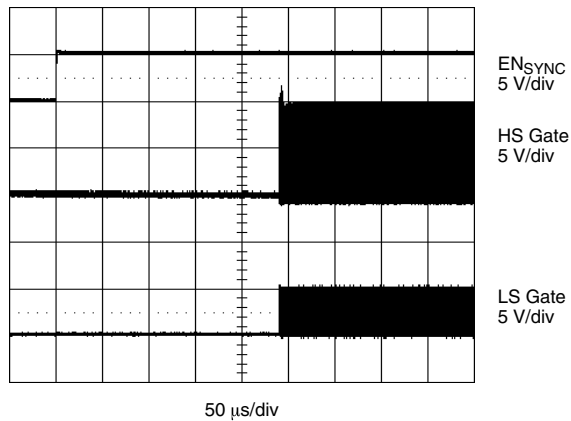


**TYPICAL WAVEFORMS**



**Figure 4. PWM Signal vs. HS Gate and LS Gate (Rising)**

**Figure 5. PWM Signal vs. HS Gate and LS Gate (Falling)**



**Figure 6 EN<sub>SYNC</sub> Delay**

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