KS54AHCT 75/77
KS74AHCT

4-Bit Bistable Latches

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
  I_{OL} = 8mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

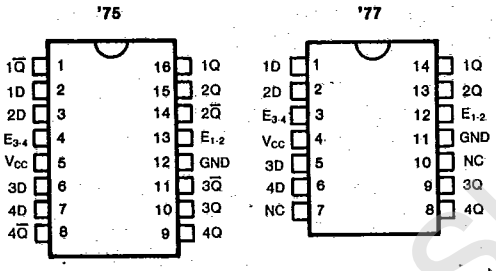
The '75 and '77 consist of 4 high-speed D-type latches that can be used as temporary storage for binary information between processing units. The '75 features complementary Q and $\overline{Q}$ output while the '77 features single nail output. These devices are ideal for high component density application.

The latches are transparent: when the enable (E) is high, the Q output will follow the data input. When the enable goes low, the output latches at the level that was set up at the D-input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

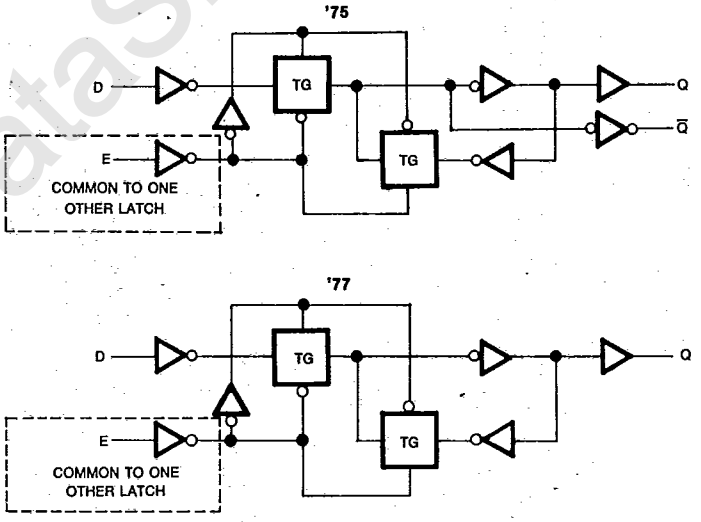


FUNCTION TABLE

Inputs		Outputs	
D	E	Q	$\overline{Q}$*
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

*$\overline{Q}$: '75 only

LOGIC DIAGRAM



KS54AHCT KS74AHCT 75/77

4-Bit Bistable Latches

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ..... ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) .... ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) ..... ±35 mA
Continuous Current Through
V_{CC} or GND pins ..... ±125 mA
Storage Temperature Range, T_{stg} ... −65°C to +150°C
Power Dissipation Per Package, P_d† ..... 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} ..... 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} .. 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f ..... Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

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DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−4mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=4mA I_O=8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input in V_I=2.4V other inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

KS54AHCT 75/77
KS74AHCT

4-Bit Bistable Latches

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT75

Characteristic	Symbol	Conditions†	$T_a=25°C$ $V_{CC}=5.0V$	KS74AHCT $T_a=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$		KS54AHCT $T_a=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay E to Q or $\overline{Q}$	t_{PLH}	$C_L=50pF$	10		16		20	ns
	t_{PHL}		10		16		20	
Propagation Delay D to Q or $\overline{Q}$	t_{PLH}	$C_L=50pF$	9		15		18	ns
	t_{PHL}		9		15		18	
Data Set up Time D to Enable	t_{SU}		6	10		12		ns
Data Hold Time Enable to D	t_h		3		5		6	ns
Input Capacitance	C_{IN}		5					pF
Power disipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT77

Characteristic	Symbol	Conditions†	$T_a=25°C$ $V_{CC}=5.0V$	KS74AHCT $T_a=-40°C$ to $+85°C$ $V_{CC}=5.0V \pm 10\%$		KS54AHCT $T_a=-55°C$ to $+125°C$ $V_{CC}=5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay E to Q	t_{PLH}	$C_L=50pF$	8		14		17	ns
	t_{PHL}		8		14		17	
Propagation Delay D to $\overline{Q}$	t_{PLH}	$C_L=50pF$	8		13		15	ns
	t_{PHL}		8		13		15	
Data Set up Time D to Enable	t_{SU}		6	10		12		ns
Data Hold Time Enable to D	t_h		3		5		6	ns
Input Capacitance	C_{IN}		5					pF
Power disipation Capacitance*	C_{PD}							pF

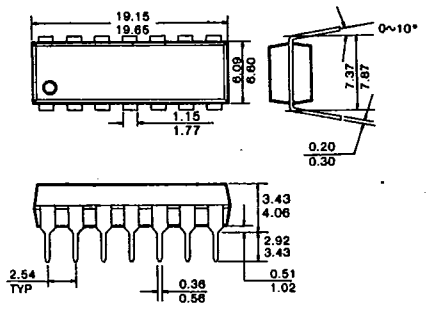
* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

PACKAGE DIMENSIONS

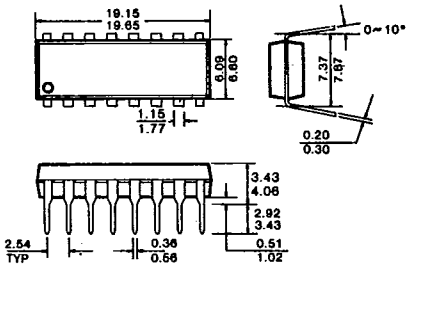
T-90-20

1. PLASTIC PACKAGES

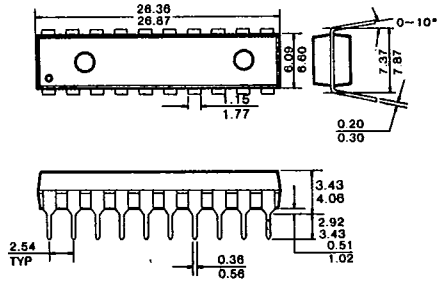
14-Pin Plastic DIP **Units: mm**



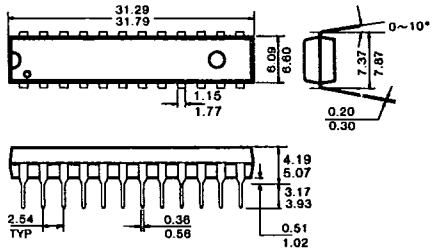
16-Pin Plastic DIP **Units: mm**



20-Pin Plastic DIP **Units: mm**



24-Pin Plastic DIP **Units: mm**



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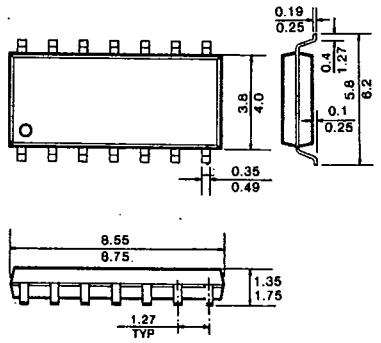
PACKAGE DIMENSIONS

T-90-20

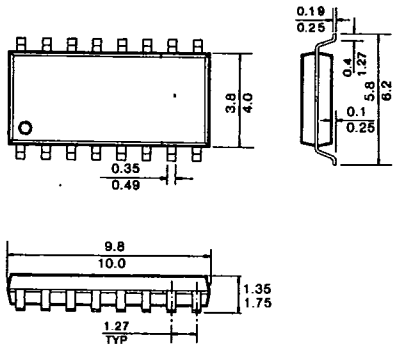
14-Pin SOP

Unit: mm



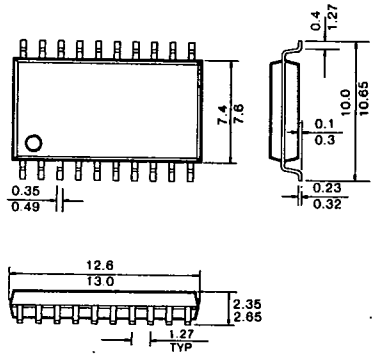
16-Pin SOP

Unit: mm



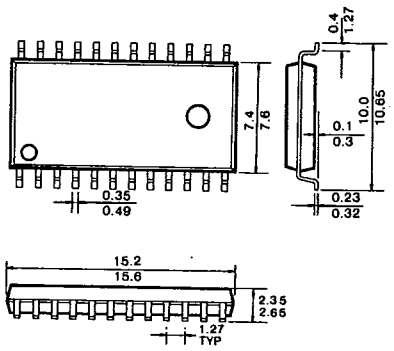
20-Pin SOP

Unit: mm



24-Pin SOP

Unit: mm

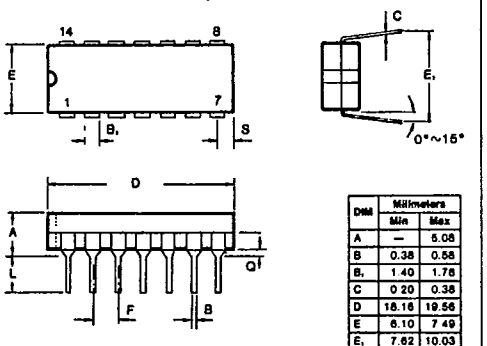


PACKAGE DIMENSIONS

T-90-20

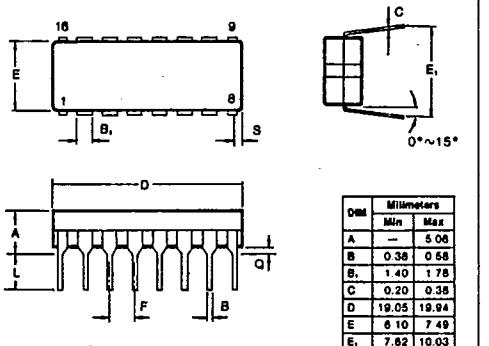
2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm



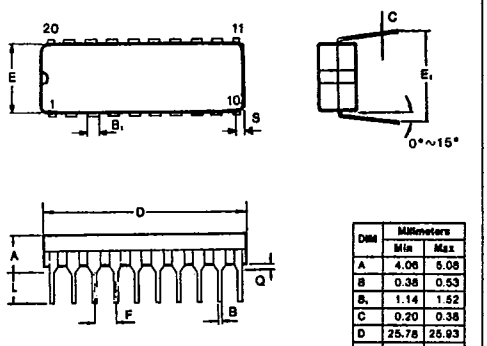
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.16	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm



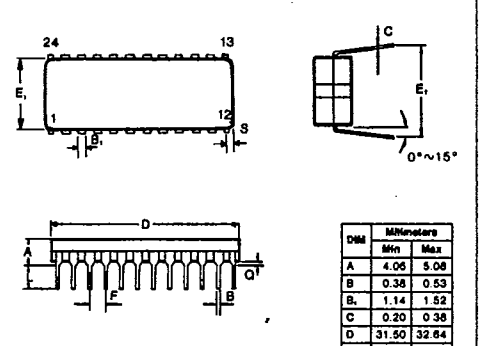
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.16	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	25.78	25.93
E	6.10	6.60
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	31.50	32.64
E	7.24	7.75
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.65	1.93

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