KS57C2408A/2416A
4-BIT CMOS Microcontroller

Product Specification

OVERVIEW

The KS57C2408A/2416A single-chip CMOS microcontroller is designed for very high performance using Samsung's newest 4-bit product development approach, SAM4 (Samsung Arrangeable Microcontrollers). Its main features are an up-to-12-digit LCD direct drive capability, 8-bit × 6-channel A/D converter, and versatile 8-bit and 16-bit counter/ timers. The "2408A/2416A" gives you an excellent design solution for a variety of LCD-related applications.

Up to 50 pins of the available 80-pin QFP packages can be dedicated to I/O. And eight vectored interrupts provide fast response to internal and external events. In addition, the 2408A/2416A's advanced CMOS technology ensures low power consumption and a wide operating voltage range.

FEATURES

Memory

- 512 × 4-bit RAM
- 8192 × 8-bit (KS57C2408A)
  16384 × 8-bit (KS57C2416A)
- Data memory mapped I/O

Oscillation Sources

- Crystal, ceramic, RC (main)
- Crystal for subsystem clock
- Main system clock frequency: 4.19 MHz (typical)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider (4, 8, 64)

Two Power-Down Modes

- Idle (only CPU clock stops)
- Stop (system clock stops)

Interrupts

- 5 internal vectored interrupts
- 3 external vectored interrupts
- 2 quasi-interrupts

50 I/O Pins

- 10 input pins
- 12 output pins
- 20 configurable I/O pins
- 8 n-channel open-drain pins

8-Bit Basic Timer

- 4 interval timer functions

8-Bit Timer/Counter

- Programmable 8-bit timer
- External event counter
- Arbitrary clock output
- External clock signal divider
- Serial I/O clock generator

16-Bit Timer/Counter

- Programmable 16-bit timer
- External event counter
- Arbitrary clock output
- External clock signal divider

Watch Timer

- Real-time and interval time measurement
- Clock generation for LCD
- Four frequency outputs for buzzer sound

LCD Controller/Driver

- Maximum 12-digit LCD direct drive capability
- Display modes: static, 1/2duty (1/2 bias)
- 1/3 duty (1/2 or1/3 bias), 1/4duty (1/3 bias)

A/D Converter

- Six analog input channels
- 19.09-μs conversion speed at 4.19 MHz
- 8-bit conversion resolution

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable
- Internal/external clock source

Instruction Execution Times

- 0.95, 1.91, 15.3 μs at 4.19 MHz (main)
- 122 μs at 32.768 kHz (subsystem)

Operating Temperature Range

- – 40 °C to 85 °C

Operating Voltage Range

- 2.7 V to 6.0 V

Package Type

- 80-pin QFP package

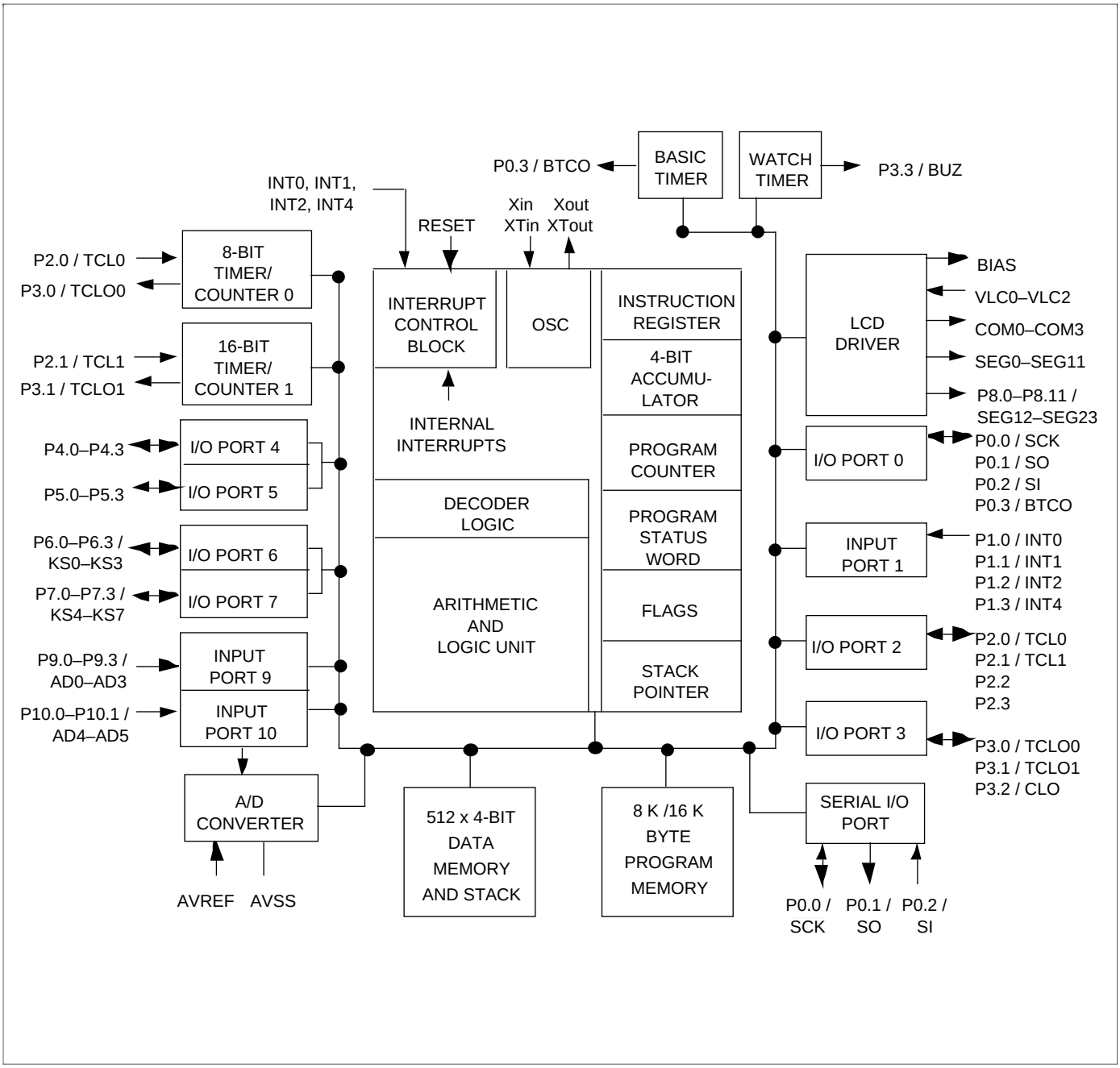

Figure 1. KS57C2408A/2416A Block Diagram

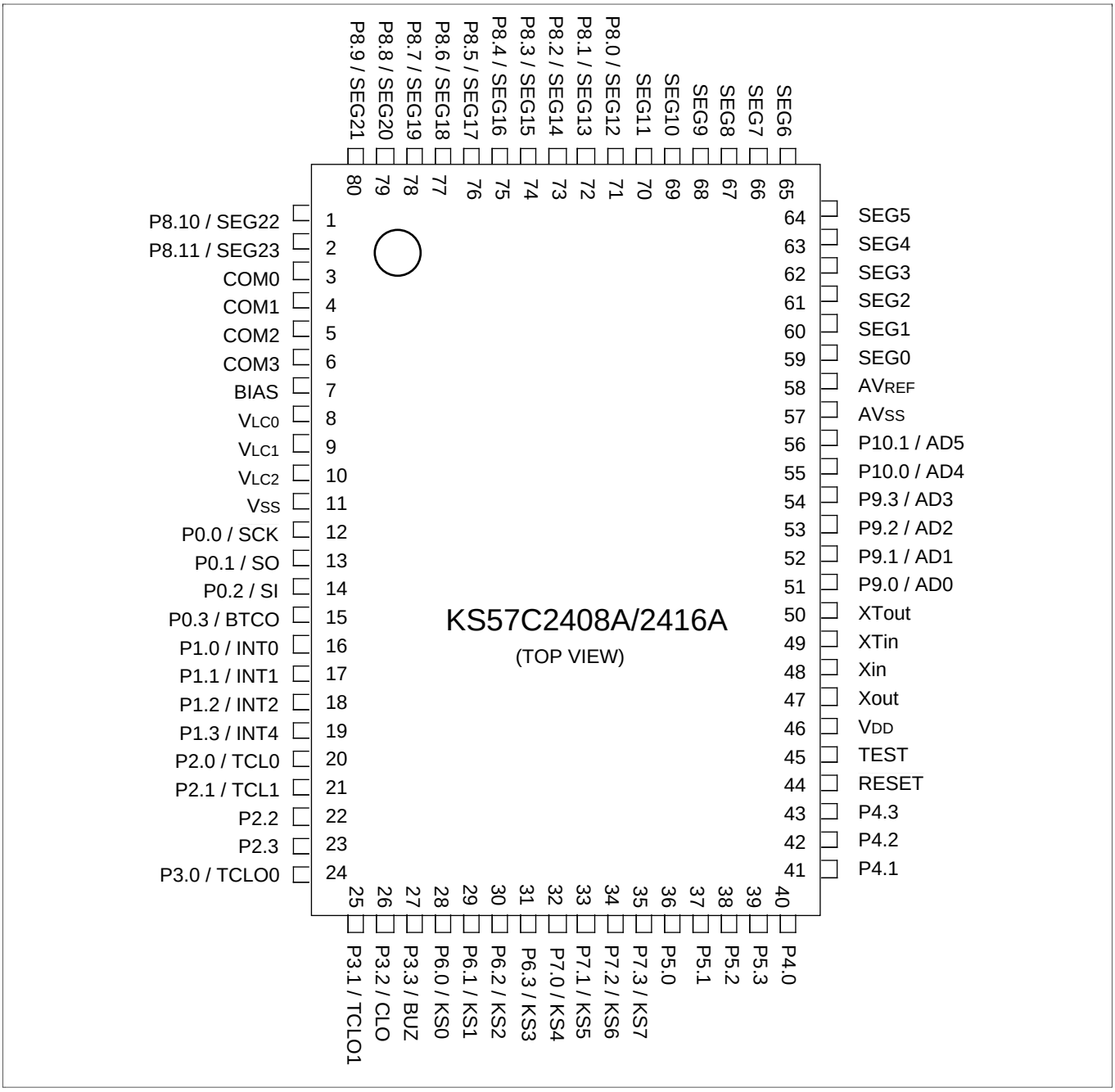

Figure 2. KS57C2408A/2416A Pin Assignments (80–QFP)

Table 1. KS57C2408A/2416A Pin Descriptions

Pin Names	Pin Type	Description	Number (80-QFP)	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable.	12 13 14 15	SCK SO SI BTCO
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. 3-bit pull-up resistors are software assignable to pins P1.0, P1.1, and P1.2.	16 17 18 19	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2 P2.3	I/O	Same as port 0.	20 21 22 23	TCL0 TCL1
P3.0 P3.1 P3.2 P3.3		Same as port 0.	24 25 26 27	TCLO0 TCLO1 CLO BUZ
P4.0–P4.3 P5.0–P5.3		4-bit I/O ports. N-channel open-drain output up to 9volts. 1 -, 4-, and 8-bit read/write and test is possible. Ports 4 and 5 can be paired to support 8-bit data transfer. Pull-up resistors are assignable to individual pins by mask option.	40–43 36–39	— —
P6.0–P6.3 P7.0–P7.3		4-bit I/O ports. Port 6 pins are individually software configurable as input or output. 1-bit and 4-bit read/write and test is possible. 4-bit pull-up resistors are software assignable. Ports 6 and 7 can be paired to enable 8-bit data transfer.	28–31 32–35	KS0–KS3 KS4–KS7
P8.0–P8.11	O	Output port for 1-bit data (for use as CMOS driver only).	71–80, 1–2	SEG12–SEG23
P9.0–P9.3 P10.0–P10.1	I	Input ports for 1-bit or 4-bit data. 1-bit and 4-bit read and test is possible.	51–56	AD0–AD3 AD4–AD5
CLO	I/O	CPU clock output	26	P3.2
BUZ		2, 4, 8, or 16 kHz frequency output for buzzer sound with 4.19 MHz main system clock or 32.768 kHz subsystem clock.	27	P3.3
X_{in}, X_{out}	—	Crystal, ceramic, or RC oscillator signal for main system clock. (For external clock input, use X_{in} and input X_{in}'s reverse phase to X_{out}.)	48, 47	—
XT_{in}, XT_{out}	—	Crystal oscillator signal for subsystem clock. (For external clock input, use XT_{in} and input XT_{in}'s reverse phase to XT_{out}).	49, 50	—
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable. Only INT0 is synchronized with the system clock.	16–17	P1.0, P1.1

Table 1. KS57C2408A/2416A Pin Descriptions (Continued)

Pin Names	Pin Type	Description	Number (80-QFP)	Share Pin
INT2	I	Quasi-interrupt with detection of rising edges	18	P1.2
INT4		External interrupt with detection of rising or falling edges	19	P1.3
KS0–KS7	I/O	Quasi-interrupt input with falling edge detection	28–35	P6.0–P7.3
TCL0		External clock input for timer/counter 0	20	P2.0
TCL1		External clock input for timer/counter 1	21	P2.1
TCLO0		Timer/counter 0 clock output	24	P3.0
TCLO1		Timer/counter 1 clock output	25	P3.1
COM0–COM3	O	LCD common signal output	3–6	—
SEG0–SEG11		LCD segment output	59–70	—
SEG12–SEG23		1-bit LCD segment data output	71–80, 1–2	P8.0–P8.11
BIAS	—	LCD power control	7	—
V_{LC0}–V_{LC2}		LCD power supply. Voltage dividing resistors are assignable by mask option.	8–10	—
AD0–AD5	I	A/D converter analog input channels	51–56	P9.0–P9.3 P10.0–P10.1
AV_{SS}	—	A/D converter ground	57	—
AV_{REF}		A/D converter analog reference voltage	58	—
SCK	I/O	Serial I/O interface clock signal	12	P0.0
SO		Serial data output	13	P0.1
SI		Serial data input	14	P0.2
BTCO		Basic interval timer clock output	15	P0.3
RESET	I	Reset signal	44	—
V_{DD}	—	Main power supply	46	—
V_{SS}		Ground	11	—
TEST		Test signal input (must be connected to $V_{SS)}$	45	—

NOTE: Pull-up resistors for ports 0, 2, 3, 6, and 7 are automatically disabled if they are configured to output mode.

Table 2. Supplemental KS57C2408A/2416A Pin Data

Pin Numbers (80-QFP)	Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
1, 2	P8.10, P8.11	SEG22–SEG23	O	Low	9
3–6	COM0–COM3	—	O	Low	8
7	BIAS	—	—	—	—
8–10	V_{LC0}–V_{LC2}	—	—	—	—
11	V_{SS}	—	—	—	—
12–15	P0.0–P0.3	SCK, SO, SI, BTCO	I/O	Input	6
16–18	P1.0–P1.2	INT0, INT1, INT2	I		3
19	P1.3	INT4	I		2
20, 21	P2.0, P2.1	TCL0, TCL1	I/O		6
22, 23	P2.2, P2.3	—			6
24–27	P3.0–P3.3	TCLO0, TCLO1, CLO, BUZ			5
28–31	P6.0–P6.3	KS0–KS3			6
32–35	P7.0–P7.3	KS4–KS7			6
36–39	P5.0–P5.3	—	I/O	(Note)	10
40–43	P4.0–P4.3	—	I/O	(Note)	10
44	RESET	—	—	—	12
45	TEST	—	—	—	—
46	V_{DD}	—	—	—	—
47, 48	X_{in}, X_{out}	—	—	—	—
49, 50	XT_{in}, XT_{out}	—	—	—	—
51–54	P9.0–P9.3	AD0–AD3	I	Input	11
55, 56	P10.0, P10.1	AD4, AD5	I	Input	11
57, 58	AV_{SS}, AV_{REF}	—	—	—	—
59–70	SEG0–SEG11	—	O	Low	7
71–80	P8.0–P8.9	SEG12–SEG21	O	Low	9

NOTE: High level (when pull-up resistors are provided) or high impedance.