FAIRCHILD SEMICONDUCTOR®

December 2010

FDMS86103L

N-Channel PowerTrench® MOSFET

100 V, 49 A, 8 mΩ

Features

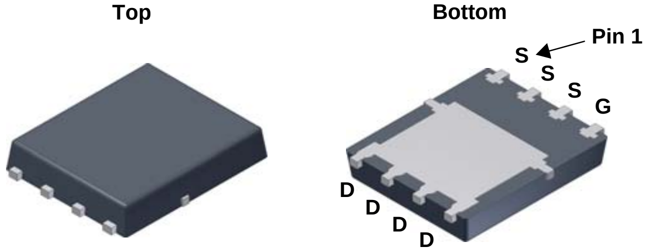
- Max $r_{DS(on)}$ = 8 mΩ at V_{GS} = 10 V, I_D = 12 A
- Max $r_{DS(on)}$ = 11 mΩ at V_{GS} = 4.5 V, I_D = 10 A
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

General Description

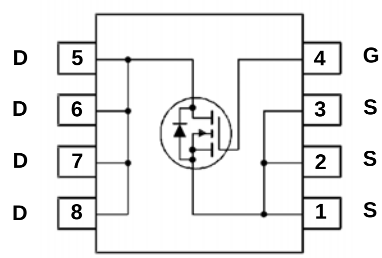
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process thant has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Application

- DC-DC Conversion



Power 56



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			100	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25 °C		49	A
	-Continuous (Silicon limited)	T_C = 25 °C		81	
	-Continuous	T_A = 25 °C	(Note 1a)	12	
	-Pulsed			100	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	312	mJ
P_D	Power Dissipation	T_C = 25 °C		104	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86103L	FDMS86103L	Power 56	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		68		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-7		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 12 A		6.4	8	mΩ
		V_{GS} = 4.5 V, I_D = 10 A		8.4	11	
		V_{GS} = 10 V, I_D = 12 A, T_J = 125 °C		10.6	14	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 12 A		59		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		2790	3710	pF
C_{oss}	Output Capacitance			469	625	pF
C_{rss}	Reverse Transfer Capacitance			22	35	pF
R_g	Gate Resistance			1.3		Ω

Switching Characteristics

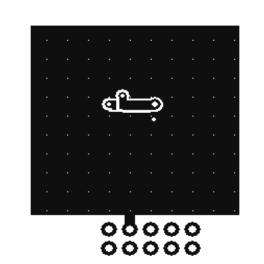
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 12 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		13	23	ns
t_r	Rise Time			7.2	15	ns
$t_{d(off)}$	Turn-Off Delay Time			35	57	ns
t_f	Fall Time			6	13	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 12 A		43	60	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 5 V; V_{DD} = 50 V, I_D = 12 A		23	32	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 50 V, I_D = 12 A		7.5		nC
Q_{gd}	Gate to Drain "Miller" Charge	V_{DD} = 50 V, I_D = 12 A		7		nC

Drain-Source Diode Characteristics

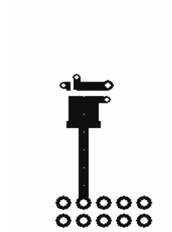
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)		0.70	1.2	V
		V_{GS} = 0 V, I_S = 12 A (Note 2)		0.78	1.3	
t_{rr}	Reverse Recovery Time	I_F = 12 A, di/dt = 100 A/μs		57	90	ns
Q_{rr}	Reverse Recovery Charge			68	108	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. Starting T_J = 25 °C, L = 1 mH, I_{AS} = 25 A, V_{DD} = 90 V, V_{GS} = 10 V

Typical Characteristics T_J = 25 °C unless otherwise noted

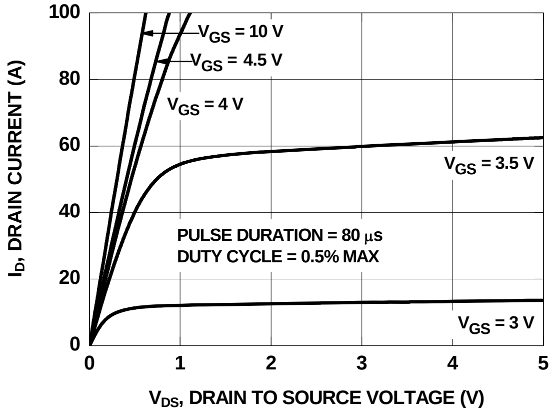


Figure 1. On-Region Characteristics

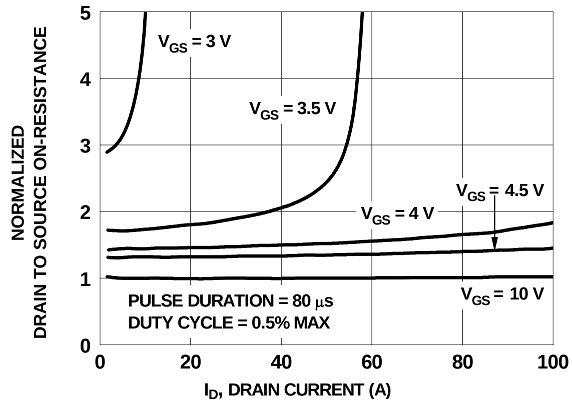


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

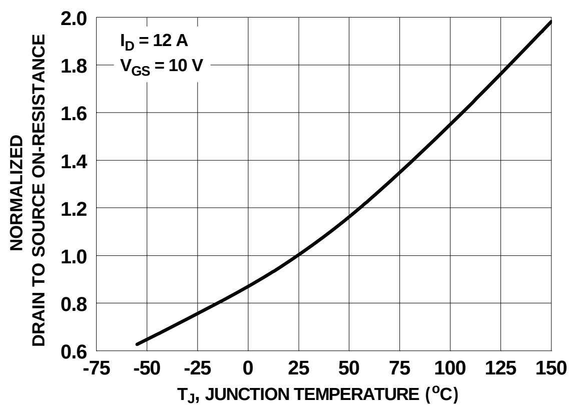


Figure 3. Normalized On-Resistance vs Junction Temperature

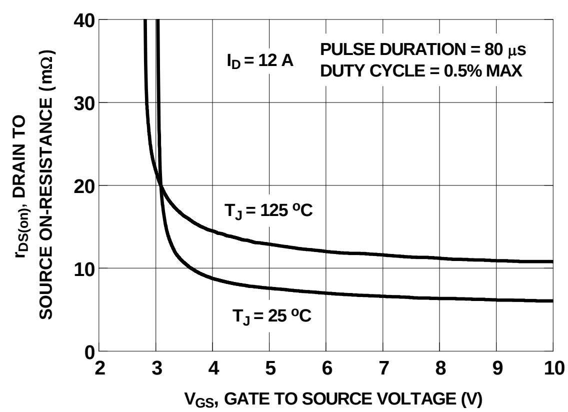


Figure 4. On-Resistance vs Gate to Source Voltage

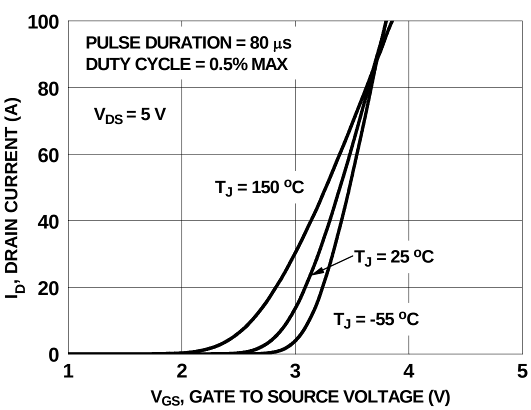


Figure 5. Transfer Characteristics

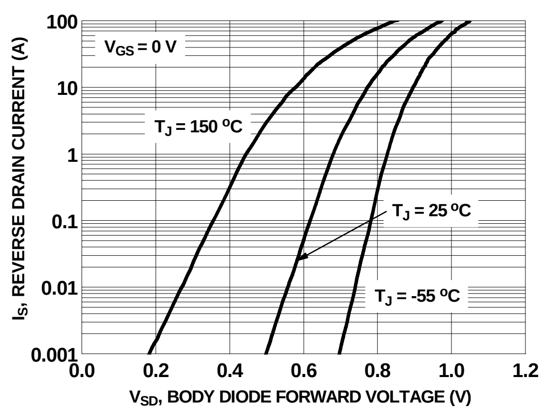


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

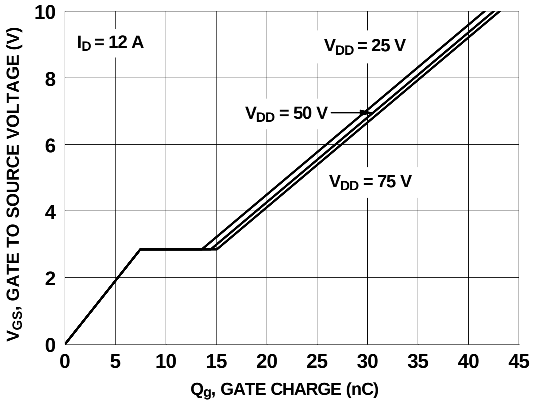


Figure 7. Gate Charge Characteristics

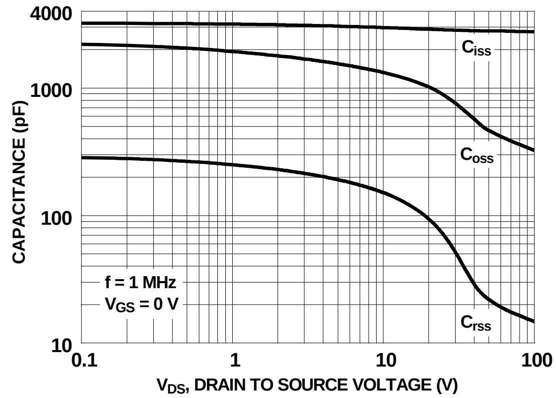


Figure 8. Capacitance vs Drain to Source Voltage

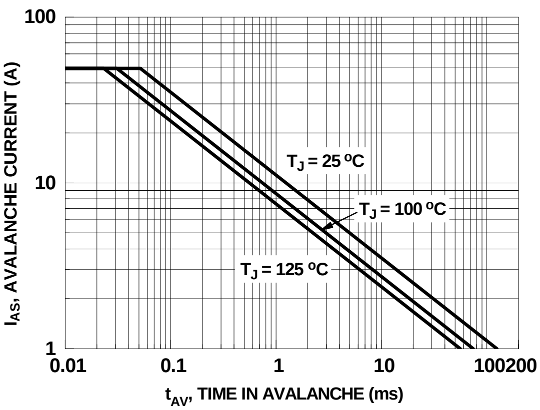


Figure 9. Unclamped Inductive Switching Capability

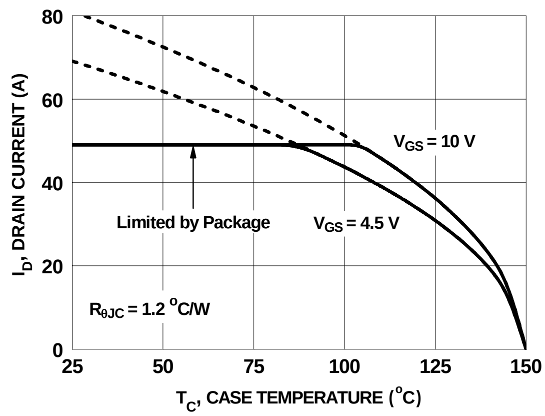


Figure 10. Maximum Continuous Drain Current vs Case Temperature

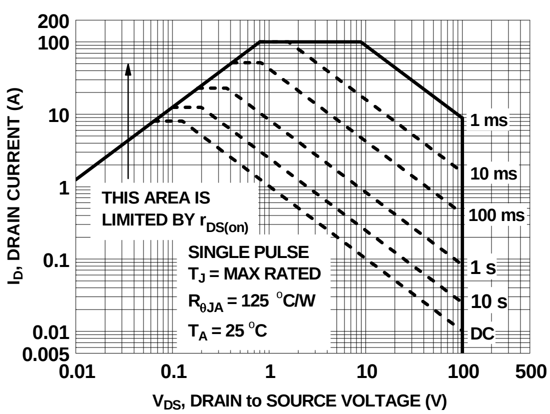


Figure 11. Forward Bias Safe Operating Area

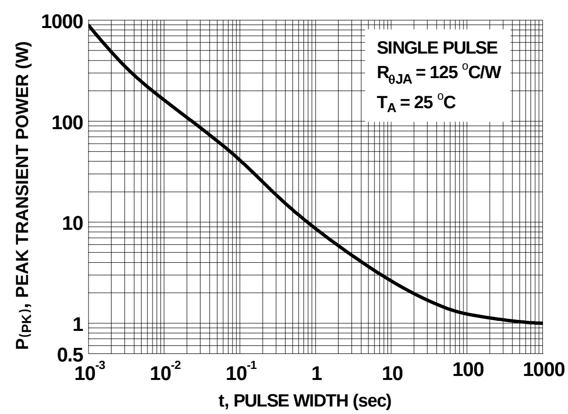


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

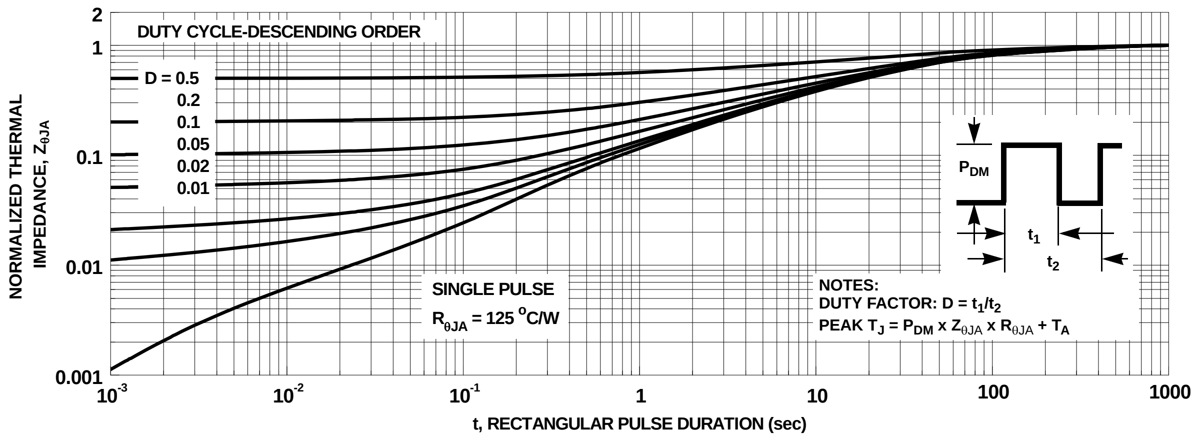
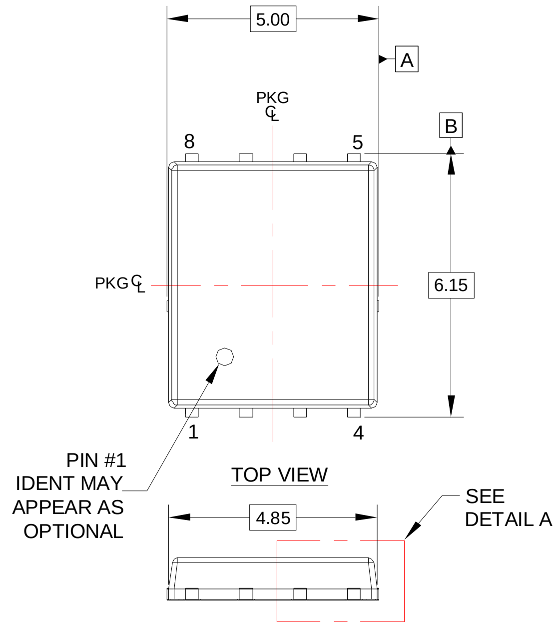


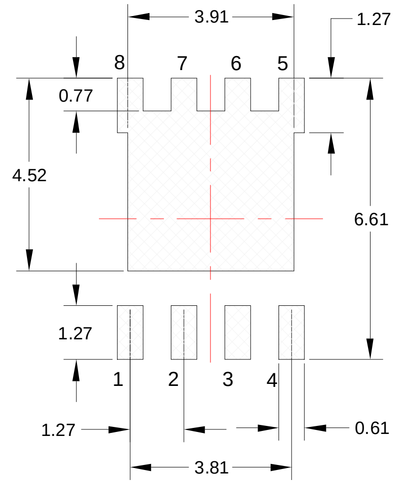
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout

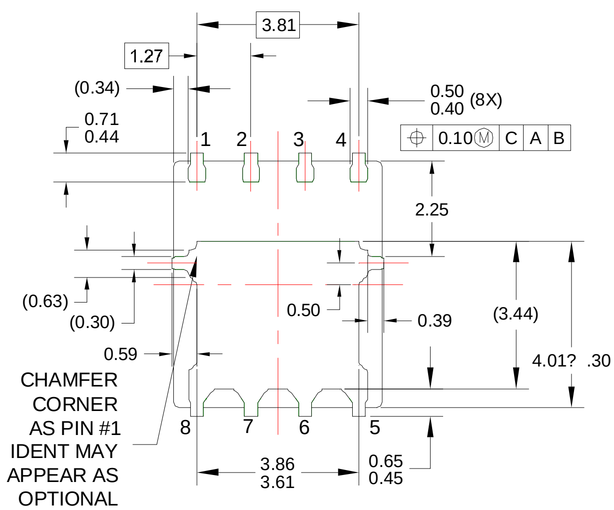


TOP VIEW

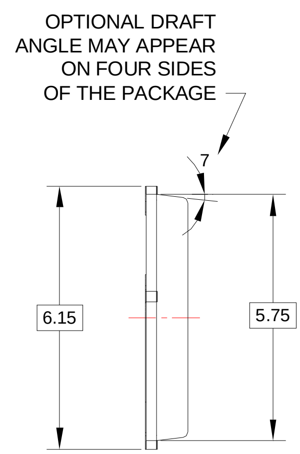
FRONT VIEW



LAND PATTERN RECOMMENDATION



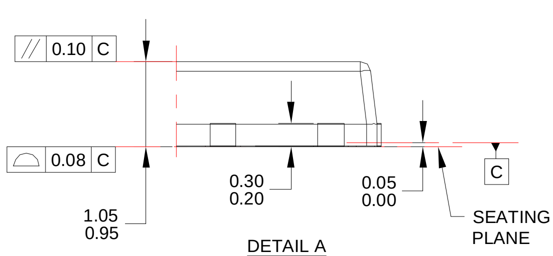
BOTTOM VIEW



SIDE VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
E) DRAWING FILE NAME: MKT-PQFN08FREV1



DETAIL A

SCALE: 2:1

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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