Quad, 16-Bit, 125 MSPS, JESD204B 1.8 V Analog-to-Digital Converter

Data Sheet **AD9656**

FEATURES

SNR = 79.9 dBFS at 16 MHz (V_{REF} = 1.4 V)
SNR = 78.1 dBFS at 64 MHz (V_{REF} = 1.4 V)
SFDR = 86 dBc to Nyquist (V_{REF} = 1.4 V)
JESD204B Subclass 1 coded serial digital outputs
Flexible analog input range: 2.0 V p-p to 2.8 V p-p
1.8 V supply operation
Low power: 197 mW per channel at 125 MSPS (two lanes)
DNL = ±0.6 LSB (V_{REF} = 1.4 V)
INL = ±4.5 LSB (V_{REF} = 1.4 V)
650 MHz analog input bandwidth, full power
Serial port control
- **Full chip and individual channel power-down modes**
- **Built-in and custom digital test pattern generation**
- **Multichip sync and clock divider**
- **Standby mode**

APPLICATIONS

Medical imaging
High speed imaging
Quadrature radio receivers
Diversity radio receivers
Portable test equipment

FUNCTIONAL BLOCK DIAGRAM

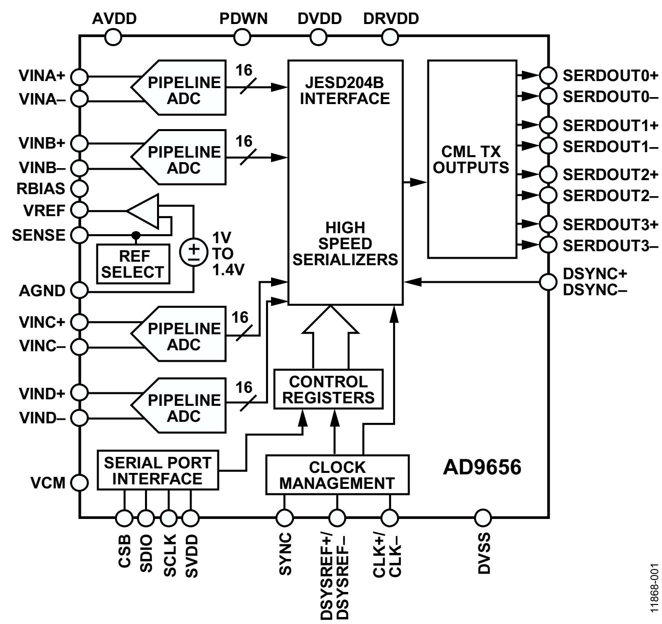

Figure 1.

GENERAL DESCRIPTION

The AD9656 is a quad, 16-bit, 125 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. The device operates at a conversion rate of up to 125 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

Individual channel power-down is supported and typically consumes less than 14 mW when all channels are disabled. The ADC contains several features designed to maximize flexibility and minimize system cost, such as a programmable output clock, data alignment, and digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9656 is available in an RoHS-compliant, nonmagnetic, 56-lead LFCSP.

It is specified over the −40°C to +85°C industrial temperature range. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. It has a small footprint. Four ADCs are contained in a small, 8 mm × 8 mm package.
2. An on-chip phase-locked loop (PLL) allows users to provide a single ADC sampling clock; the PLL multiplies the ADC sampling clock to produce the corresponding JESD204B data rate clock.
3. The configurable JESD204B output block supports up to 6.4 Gbps per lane.
4. JESD204B output block supports one, two, and four lane configurations.
5. Low power of 198 mW per channel at 125 MSPS, two lanes.
6. The SPI control offers a wide range of flexible features to meet specific system requirements.

Rev. 0 Document Feedback

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REVISION HISTORY

12/13—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS, V_{REF} = 1.4 V

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 V p-p full-scale differential input, 1.4 V reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 1.

Parameter[1]	Temperature	Min	Typ	Max	Unit
RESOLUTION			16		Bits
ACCURACY					
No Missing Codes	25°C		Guaranteed		
Offset Error	25°C	−0.1	+0.14	+0.5	% FSR
Offset Matching	25°C	0	0.1	0.4	% FSR
Gain Error	25°C	−1.0	+1.0	+3.1	% FSR
Gain Matching	25°C	0	1.1	2.0	% FSR
Differential Nonlinearity (DNL)	25°C	−0.95	±0.6	+2.54	LSB
Integral Nonlinearity (INL)	25°C	−10.0	±4.5	+10.0	LSB
TEMPERATURE DRIFT					
Gain Error	Full		6.1		ppm/°C
Offset Error	Full		−2		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage	25°C	1.37	1.4	1.41	V
Load Regulation at 1.0 mA	25°C		4		mV
Input Resistance	25°C		7.5		kΩ
INPUT-REFERRED NOISE					
V_{REF} = 1.4 V	25°C		2.1		LSB rms
ANALOG INPUTS					
Differential Input Voltage	25°C		2.8		V p-p
Common-Mode Voltage	25°C		0.9		V
Common-Mode Range	25°C	0.7		1.1	V
Differential Input Resistance	25°C		2.6		kΩ
Differential Input Capacitance	25°C		7		pF
POWER SUPPLY					
AVDD	25°C	1.7	1.8	1.9	V
DVDD, DRVDD	25°C	1.7	1.8	1.9	V
I_{AVDD} (125 MSPS, Two Lanes)[2]	25°C		288	306	mA
I_{DVDD} (125 MSPS, Two Lanes)[2]	25°C		67	72	mA
I_{DRVDD} (125 MSPS, Two Lanes)[2]	25°C		83	88	mA
TOTAL POWER CONSUMPTION					
DC Input (125 MSPS, Four Channels onto Two Lanes)	25°C		706		mW
Sine Wave Input (125 MSPS, Four Channels onto Two Lanes)[2]	25°C		788	839	mW
Power-Down Mode	25°C		14		mW
Standby Mode[3]	25°C		547		mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured with a low input frequency, full-scale sine wave on all four channels.
[3] Standby can be controlled via the SPI.

DC SPECIFICATIONS, V_{REF} = 1.0 V

AVDD = 1.8 V, DRVDD = 1.8 V, 2.0 V p-p full-scale differential input, 1.0 V reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
RESOLUTION			16		Bits
ACCURACY					
No Missing Codes	25°C		Guaranteed		
Offset Error	25°C		0.2		% FSR
Offset Matching	25°C		0.13		% FSR
Gain Error	25°C		1.0		% FSR
Gain Matching	25°C		0.4		% FSR
Differential Nonlinearity (DNL)	25°C		±0.6		LSB
Integral Nonlinearity (INL)	25°C		±6.0		LSB
TEMPERATURE DRIFT					
Gain Error	Full		3.1		ppm/°C
Offset Error	Full		−3		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage	25°C		1.0		V
Load Regulation at 1.0 mA	25°C		2		mV
Input Resistance	25°C		7.5		kΩ
INPUT-REFERRED NOISE					
V_{REF} = 1.0 V	25°C		2.7		LSB rms
ANALOG INPUTS					
Differential Input Voltage	25°C		2.0		V p-p
Common-Mode Voltage	25°C		0.9		V
Common-Mode Range	25°C	0.5		1.3	V
Differential Input Resistance	25°C		2.6		kΩ
Differential Input Capacitance	25°C		7		pF
POWER SUPPLY					
AVDD	25°C	1.7	1.8	1.9	V
DVDD, DRVDD	25°C	1.7	1.8	1.9	V
I_{AVDD} (125 MSPS, Two Lanes)[2]	25°C		276		mA
I_{DVDD} (125 MSPS, Two Lanes)[2]	25°C		69		mA
I_{DRVDD} (125 MSPS, Two Lanes)[2]	25°C		83		mA
TOTAL POWER CONSUMPTION					
DC Input (125 MSPS, Four Channels onto Two Lanes)	25°C		688		mW
Sine Wave Input (125 MSPS, Four Channels onto Two Lanes)	25°C		771		mW
Power-Down Mode	25°C		14		mW
Standby Mode[3]	25°C		520		mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured with a low input frequency, full-scale sine wave on all four channels.
[3] Standby can be controlled via the SPI.

AC SPECIFICATIONS, V_{REF} = 1.4 V

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 V p-p full-scale differential input, 1.4 V reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 3.

Parameter[1]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 9.7 MHz	25°C		80.1		dBFS
f_{IN} = 16 MHz	25°C		79.9		dBFS
f_{IN} = 64 MHz	25°C	75.7	78.1		dBFS
f_{IN} = 128 MHz	25°C		75		dBFS
f_{IN} = 201 MHz	25°C		72.7		dBFS
f_{IN} = 301 MHz	25°C		69.7		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION (SINAD) RATIO					
f_{IN} = 9.7 MHz	25°C		79.6		dBFS
f_{IN} = 16 MHz	25°C		78.4		dBFS
f_{IN} = 64 MHz	25°C	74.8	77.3		dBFS
f_{IN} = 128 MHz	25°C		74.4		dBFS
f_{IN} = 201 MHz	25°C		71		dBFS
f_{IN} = 301 MHz	25°C		68.6		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25°C		12.9		Bits
f_{IN} = 16 MHz	25°C		12.7		Bits
f_{IN} = 64 MHz	25°C	12.1	12.5		Bits
f_{IN} = 128 MHz	25°C		12.1		Bits
f_{IN} = 201 MHz	25°C		11.5		Bits
f_{IN} = 301 MHz	25°C		11.1		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25°C		89		dBc
f_{IN} = 16 MHz	25°C		87		dBc
f_{IN} = 64 MHz	25°C	78	86		dBc
f_{IN} = 128 MHz	25°C		84		dBc
f_{IN} = 201 MHz	25°C		76		dBc
f_{IN} = 301 MHz	25°C		75		dBc
WORST HARMONIC (SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−89		dBc
f_{IN} = 16 MHz	25°C		−87		dBc
f_{IN} = 64 MHz	25°C		−86	−78	dBc
f_{IN} = 128 MHz	25°C		−84		dBc
f_{IN} = 201 MHz	25°C		−76		dBc
f_{IN} = 301 MHz	25°C		−75		dBc
WORST OTHER HARMONIC (EXCLUDING SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−96		dBc
f_{IN} = 16 MHz	25°C		−92		dBc
f_{IN} = 64 MHz	25°C		−90	−87	dBc
f_{IN} = 128 MHz	25°C		−89		dBc
f_{IN} = 201 MHz	25°C		−93		dBc
f_{IN} = 301 MHz	25°C		−90		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—INPUT AMPLITUDE = −7.0 dBFS					
f_{IN1} = 70.5 MHz, f_{IN2} = 72.5 MHz	25°C		−84		dBc

Parameter[1]	Temperature	Min	Typ	Max	Unit
CROSSTALK[2]	25°C		−93		dB
CROSSTALK (OVERRANGE CONDITION)[3]	25°C		−89		dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C		650		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Crosstalk is measured at 70 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[3] Overrange condition is defined as the input being 3 dB above full scale.

AC SPECIFICATIONS, V_{REF} = 1.0 V

AVDD = 1.8 V, DRVDD = 1.8 V, 2.0 V p-p full-scale differential input, 1.0 V reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 4.

Parameter[1]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 9.7 MHz	25°C		78		dBFS
f_{IN} = 16 MHz	25°C		77.9		dBFS
f_{IN} = 64 MHz	25°C		76.8		dBFS
f_{IN} = 128 MHz	25°C		74.3		dBFS
f_{IN} = 201 MHz	25°C		72.1		dBFS
f_{IN} = 301 MHz	25°C		69.3		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION (SINAD) RATIO					
f_{IN} = 9.7 MHz	25°C		78		dBFS
f_{IN} = 16 MHz	25°C		77.7		dBFS
f_{IN} = 64 MHz	25°C		76.1		dBFS
f_{IN} = 128 MHz	25°C		74		dBFS
f_{IN} = 201 MHz	25°C		71.1		dBFS
f_{IN} = 301 MHz	25°C		68.6		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25°C		12.7		Bits
f_{IN} = 16 MHz	25°C		12.6		Bits
f_{IN} = 64 MHz	25°C		12.3		Bits
f_{IN} = 128 MHz	25°C		12.0		Bits
f_{IN} = 201 MHz	25°C		11.5		Bits
f_{IN} = 301 MHz	25°C		11.1		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25°C		99		dBc
f_{IN} = 16 MHz	25°C		92		dBc
f_{IN} = 64 MHz	25°C		89		dBc
f_{IN} = 128 MHz	25°C		87		dBc
f_{IN} = 201 MHz	25°C		78		dBc
f_{IN} = 301 MHz	25°C		78		dBc
WORST HARMONIC (SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−99		dBc
f_{IN} = 16 MHz	25°C		−92		dBc
f_{IN} = 64 MHz	25°C		−89		dBc
f_{IN} = 128 MHz	25°C		−87		dBc
f_{IN} = 201 MHz	25°C		−78		dBc
f_{IN} = 301 MHz	25°C		−78		dBc
WORST OTHER HARMONIC (EXCLUDING SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C		−95		dBc
f_{IN} = 16 MHz	25°C		−95		dBc
f_{IN} = 64 MHz	25°C		−94		dBc
f_{IN} = 128 MHz	25°C		−89		dBc
f_{IN} = 201 MHz	25°C		−91		dBc
f_{IN} = 301 MHz	25°C		−89		dBc

Parameter[1]	Temperature	Min	Typ	Max	Unit
TWO-TONE INTERMODULATION DISTORTION (IMD)—INPUT AMPLITUDE = −7.0 dBFS					
f_{IN1} = 70.5 MHz, f_{IN2} = 72.5 MHz	25°C		−89		dBc
CROSSTALK[2]	25°C		−94		dB
CROSSTALK (OVERRANGE CONDITION)[3]	25°C		−89		dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C		650		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Crosstalk is measured at 70 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[3] Overrange condition is defined as the input being 3 dB above full-scale.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 V p-p differential input, 1.4 V reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 5.

Parameter[1]	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage Range[2]	Full	0.2		3.6	V p-p
Input Voltage Range	Full	AGND − 0.2		AVDD + 0.2	V
Input Common-Mode Voltage	Full		0.9		V
Input Resistance (Differential)	25°C		15		kΩ
Input Capacitance	25°C		4		pF
DSYNC INPUT (DSYNC+/DSYNC−)					
Logic Compliance			LVDS		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage Range	Full	0.3		3.6	V p-p
Input Voltage Range	Full	DGND		DVDD	V
Input Common-Mode Voltage Range	Full	0.9		1.4	V
High Level Input Current	Full	−5		+5	μA
Low Level Input Current	Full	−5		+5	μA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ
DSYSREF INPUT (DSYSREF+/DSYSREF−)					
Logic Compliance			LVDS		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage Range	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Voltage Range	Full	0.9		1.4	V
High Level Input Current	Full	−5		+5	μA
Low Level Input Current	Full	−5		+5	μA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
LOGIC INPUTS (PDWN, SYNC, SCLK)					
Logic 1 Voltage Range	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage Range	Full	0		0.8	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage Range	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage Range	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		2		pF

Parameter[1]	Temperature	Min	Typ	Max	Unit
LOGIC INPUT (SDIO)					
Logic 1 Voltage Range	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage Range	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		5		pF
LOGIC OUTPUT (SDIO)[3]					
Logic 1 Voltage (I_{OH} = 800 μA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 μA)	Full			0.05	V
DIGITAL OUTPUTS (SERDOUTx+, SERDOUTx−)					
Logic Compliance	Full		CML		
Differential Output Voltage (V_{OD})	Full	400	600	750	mV
Output Offset Voltage (V_{OS})	Full	0.75	DRVDD/2	1.05	V

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Specified for LVDS and LVPECL only.
[3] Specified for the SDIO pins on 13 individual AD9656 devices sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 V p-p differential input, 1.4 V reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table 6.

Parameter[1, 2]	Temperature	Min	Typ	Max	Unit
CLOCK[3]					
Input Clock Rate	Full	40		1000	MHz
Conversion Rate	Full	40		125	MSPS
Clock Pulse Width High (t_{EH})	Full		4.00		ns
Clock Pulse Width Low (t_{EL})	Full		4.00		ns
SYNC Setup Time to Clock	Full			1.4	ns
SYNC Hold Time to Clock	Full			−0.4	ns
DSYSREF Setup Time to Clock (t_{REFS})[4]	Full		370	600	ps
DSYSREF Hold Time to Clock (t_{REFH})[4]	Full		−92	0	ps
DATA OUTPUT PARAMETERS					
Data Output Period or Unit Interval (UI)	Full		L/(20 × M × f_S)		Seconds
Data Output Duty Cycle	25°C		50		%
Data Valid Time	25°C		0.81		UI
PLL Lock Time (t_{LOCK})	25°C		25		μs
Wake-Up Time					
Standby	25°C		250		ns
ADC (Power-Down)[5]	25°C		375		μs
Output (Power-Down)[6]	25°C		50		μs
DSYNC Falling Edge to First K.28 Characters	Full	4			Multiframes
CGS Phase K.28 Characters Duration	Full	1			Multiframe
Pipeline Delay					
JESD204B M4, L1 Mode (Latency)	Full		23		Cycles[7]
JESD204B M4, L2 Mode (Latency)	Full		29		Cycles[7]
JESD204B M4, L4 Mode (Latency)	Full		44		Cycles[7]
Data Rate per Lane	Full			6.4	Gbps
Deterministic Jitter (D_J)					
At 6.4 Gbps	Full		8		ps
Random Jitter (R_J)					
At 6.4 Gbps	Full		1.25		ps rms
Output Rise Time/Fall Time	Full		50		ps
Differential Termination Resistance	25°C		100		Ω

Parameter[1, 2]	Temperature	Min	Typ	Max	Unit
APERTURE					
Aperture Delay (t_A)	25°C		1		ns
Aperture Uncertainty (Jitter, t_J)	25°C		135		fs rms
Out-of-Range Recovery Time	25°C		1		Clock cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured on standard FR-4 material.
[3] The clock can be adjusted via the SPI. The conversion rate is the clock rate after the divider.
[4] Refer to Figure 3 for timing diagram.
[5] Time required for the ADC to return to normal operation from power-down mode.
[6] Time required for the JESD204B output to return to normal operation from power-down mode.
[7] ADC conversion rate cycles.

TIMING SPECIFICATIONS

Table 7.

Parameter	Description	Limit	Unit
SPI TIMING REQUIREMENTS	See Figure 70		
t_{DS}	Setup time between the data and the rising edge of SCLK	2	ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB and SCLK	2	ns min
t_H	Hold time between CSB and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLK pulse width low	10	ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in figure)	10	ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in figure)	10	ns min

Timing Diagrams

Refer to the Memory Map Register Table section for SPI register settings.

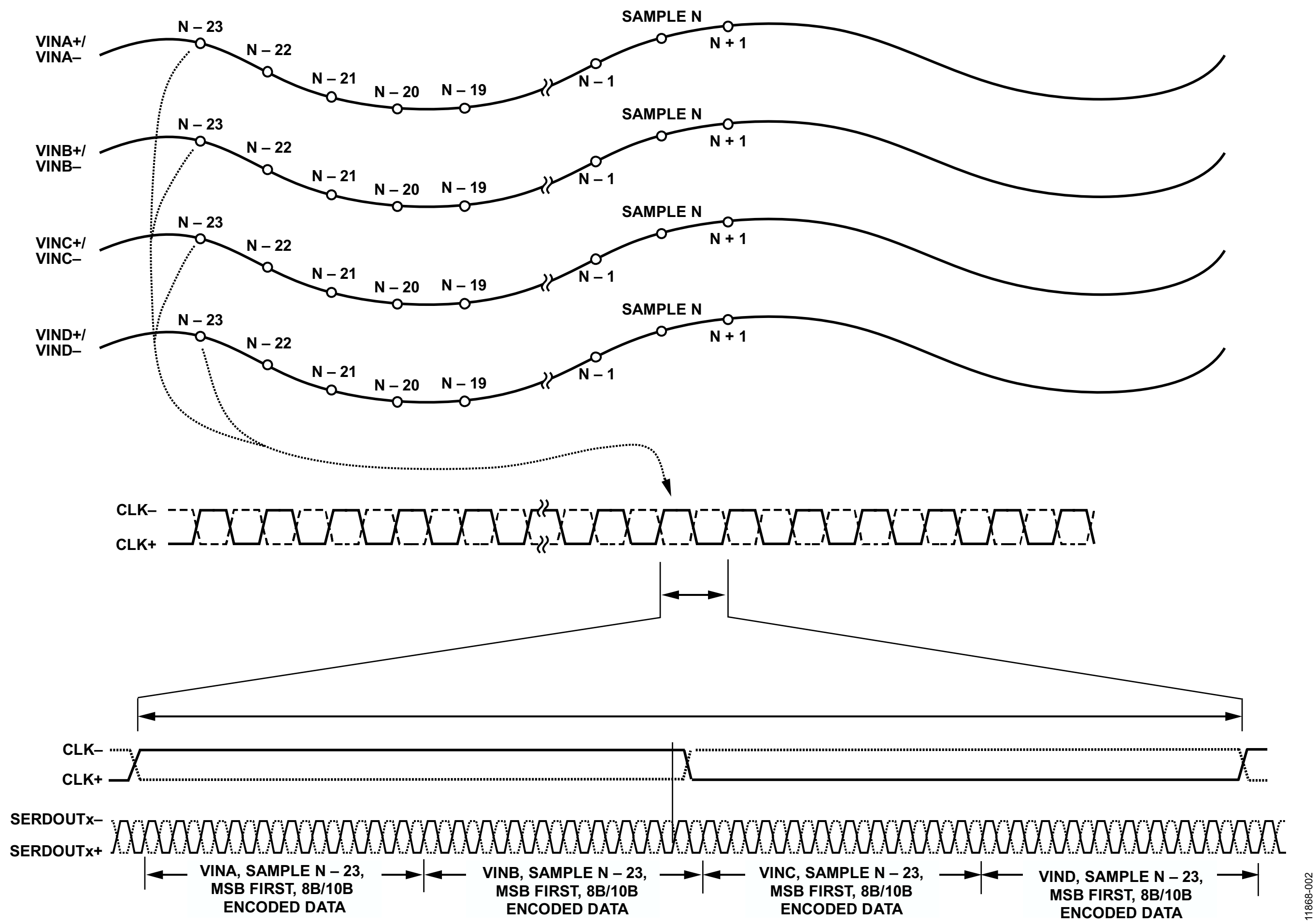

Figure 2. Data Output Timing

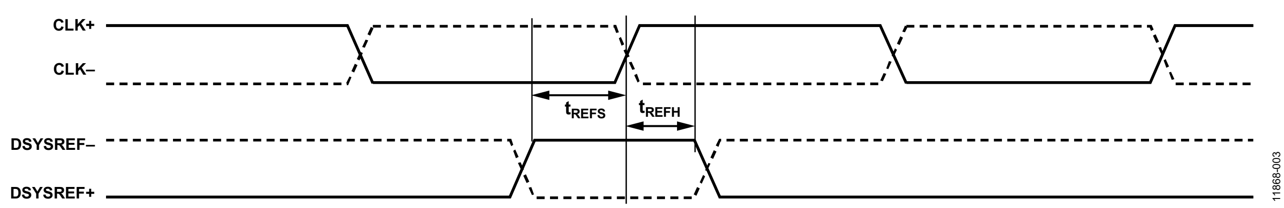

Figure 3. DSYSREF+/DSYSREF– Setup and Hold Timing (Clock Divider = 1)

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
DVDD to DVSS	−0.3 V to +2.0 V
SVDD to AGND	−0.3 V to +2.0 V
Digital Outputs to AGND	−0.3 V to +2.0 V
CLK+, CLK− to AGND	−0.3 V to +2.0 V
VINx+, VINx− to AGND	−0.3 V to +2.0 V
DSYSREF+, DSYSREF− to AGND	−0.3 V to +2.0 V
DSYNC−, DSYNC+ to AGND	−0.3 V to +2.0 V
SCLK, SDIO, CSB, PDWN to AGND	−0.3 V to +3.9 V
SYNC to AGND	−0.3 V to +2.0 V
RBIAS to AGND	−0.3 V to +2.0 V
VCM, VREF, SENSE to AGND	−0.3 V to +2.0 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is for a 4-layer printed circuit board (PCB) with solid ground plane (simulated). The exposed pad is soldered to the PCB ground.

Table 9. Thermal Resistance

Package Type	Air Flow Velocity (m/sec)	θ_{JA} (°C/W)	θ_{JB} (°C/W)[1]	θ_{JC} Top (°C/W)[1]	θ_{JC} Bottom (°C/W)[1]
56-Lead LFCSP, 8 mm × 8 mm	0	22.4	7.7	7.42	2.29
	1	19.0	N/A	N/A	N/A
	2.5	17.6	N/A	N/A	N/A

[1] N/A = not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

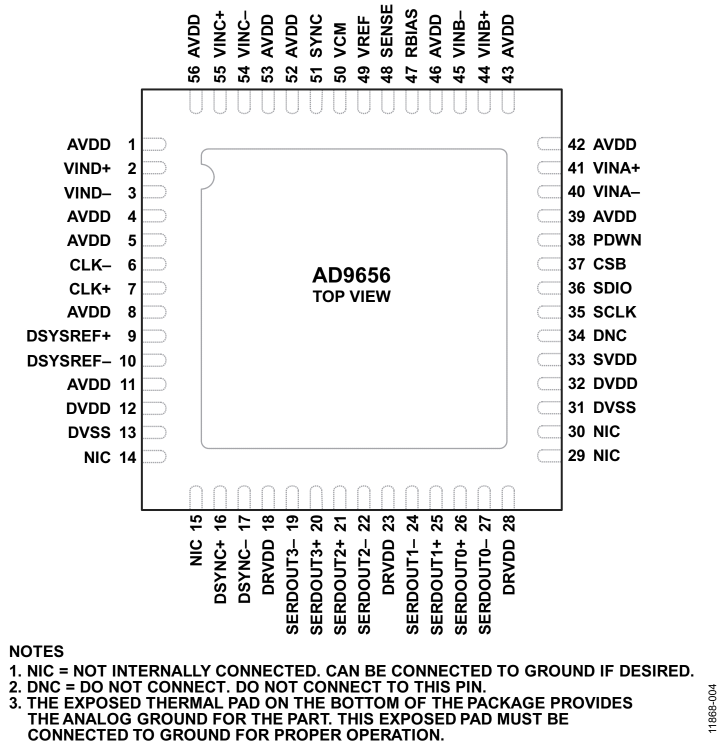

Figure 4. Pin Configuration, Top View

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	AGND, Exposed Pad	Analog Ground, Exposed Pad. The exposed thermal pad on the bottom of the package provides the analog ground for the device. This exposed pad must be connected to ground for proper operation.
1, 4, 5, 8, 11, 39, 42, 43, 46, 52, 53, 56	AVDD	1.8 V Analog Supply Pins.
2	VIND+	ADC D Analog Input True.
3	VIND–	ADC D Analog Input Complement.
6, 7	CLK–, CLK+	Differential Encode Clock. PECL, LVDS, or 1.8 V CMOS inputs.
9	DSYSREF+	Active Low JESD204B LVDS SYSREF Input True.
10	DSYSREF–	Active Low JESD204B LVDS SYSREF Input Complement.
12, 32	DVDD	Digital Supply.
13, 31	DVSS	Digital Ground.
14, 15, 29, 30	NIC	Not Internally Connected. Can be connected to ground if desired.
16	DSYNC+	Active Low JESD204B LVDS SYNC Input True.
17	DSYNC–	Active Low JESD204B LVDS SYNC Input Complement.
18, 23, 28	DRVDD	Digital Output Driver Supply.
19	SERDOUT3–	Lane 3 Digital Output Complement.
20	SERDOUT3+	Lane 3 Digital Output True.
21	SERDOUT2+	Lane 2 Digital Output True.
22	SERDOUT2–	Lane 2 Digital Output Complement.
24	SERDOUT1–	Lane 1 Digital Output Complement.
25	SERDOUT1+	Lane 1 Digital Output True.
26	SERDOUT0+	Lane 0 Digital Output True.
27	SERDOUT0–	Lane 0 Digital Output Complement.
33	SVDD	SPI Supply Pin.

Pin No.	Mnemonic	Description
34	DNC	Do Not Connect. Do not connect to this pin.
35	SCLK	SPI Clock Input.
36	SDIO	SPI Data Input and Output, Bidirectional.
37	CSB	SPI Chip Select Bar. Active low enable; 30 kΩ internal pull-up resistor.
38	PDWN	Digital Input. This pin has a 30 kΩ internal pull-down resistor. PDWN high = power-down device, and PDWN low = run device (normal operation).
40	VINA−	ADC A Analog Input Complement.
41	VINA+	ADC A Analog Input True.
44	VINB+	ADC B Analog Input True.
45	VINB−	ADC B Analog Input Complement.
47	RBIAS	Sets Analog Current Bias. This pin connects a 10 kΩ (1% tolerance) resistor to ground.
48	SENSE	Reference Mode Selection.
49	VREF	Voltage Reference Input and Output.
50	VCM	Analog Input Common-Mode Voltage.
51	SYNC	Digital Input. Synchronous input to clock divider.
54	VINC−	ADC C Analog Input Complement.
55	VINC+	ADC C Analog Input True.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{REF} = 1.4 V

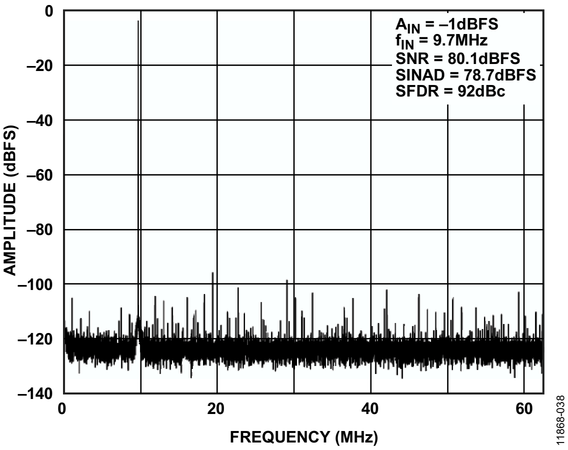

Figure 5. Single-Tone 32k FFT with f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

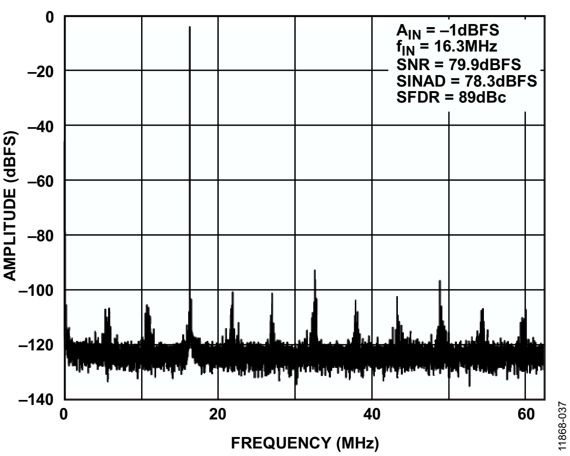

Figure 6. Single-Tone 32k FFT with f_{IN} = 16.3 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

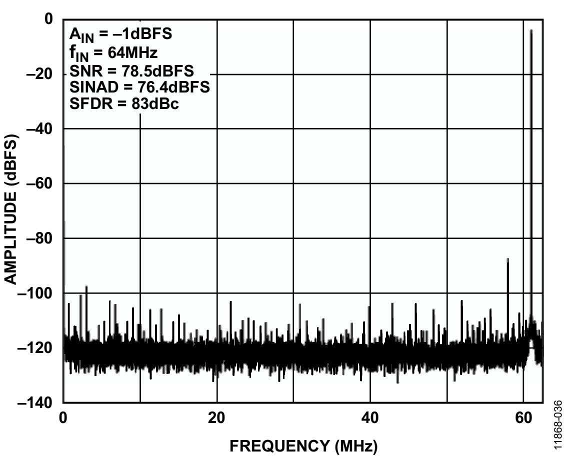

Figure 7. Single-Tone 32k FFT with f_{IN} = 64 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

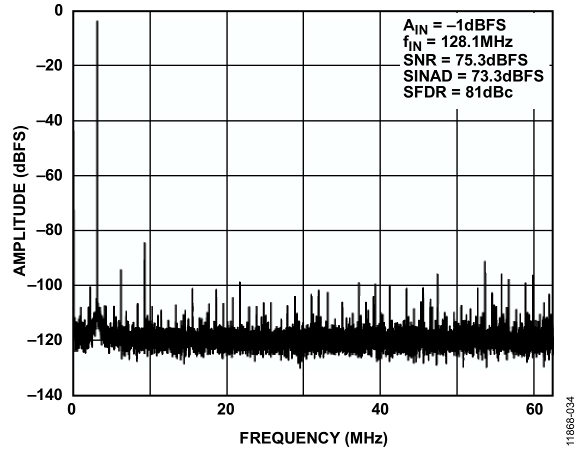

Figure 8. Single-Tone 32k FFT with f_{IN} = 128.1 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

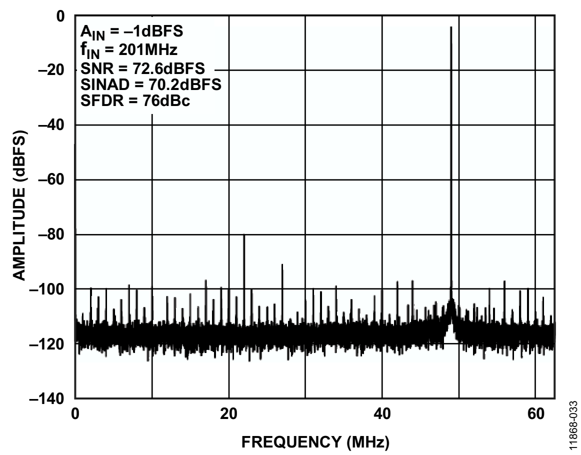

Figure 9. Single-Tone 32k FFT with f_{IN} = 201 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

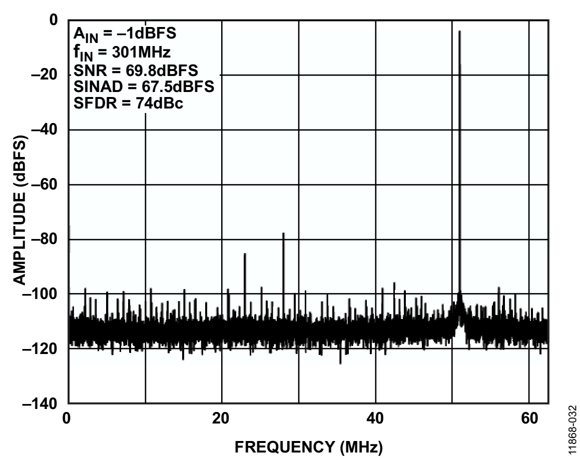

Figure 10. Single-Tone 32k FFT with f_{IN} = 301 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

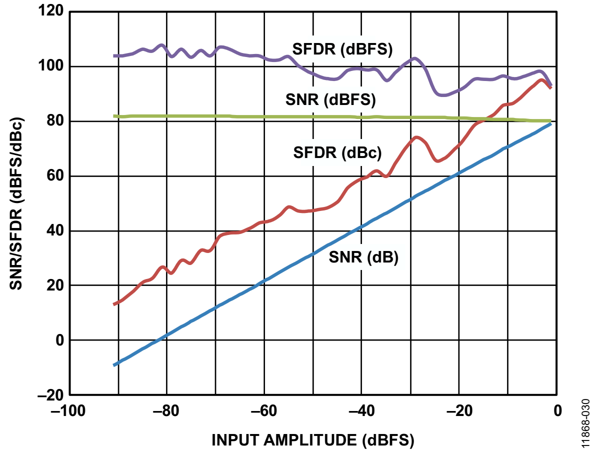

Figure 11. SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

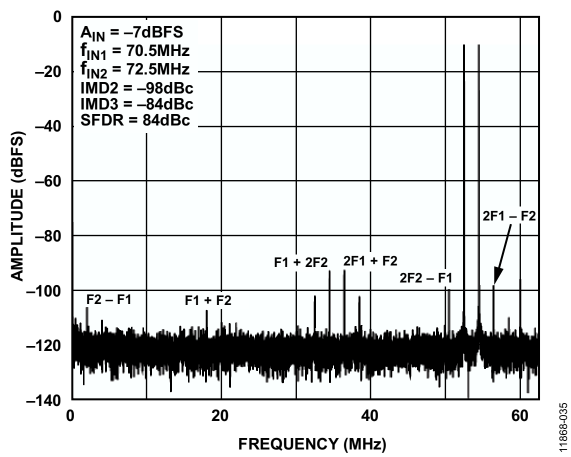

Figure 12. Two-Tone 32k FFT with f_{IN1} = 70.5 MHz and f_{IN2} = 72.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

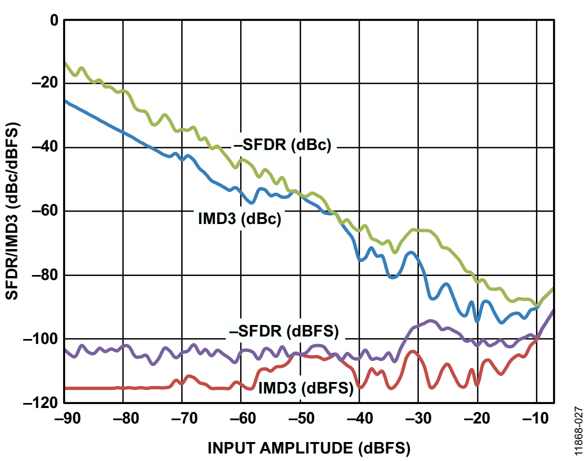

Figure 13. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 70.5 MHz and f_{IN2} = 72.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

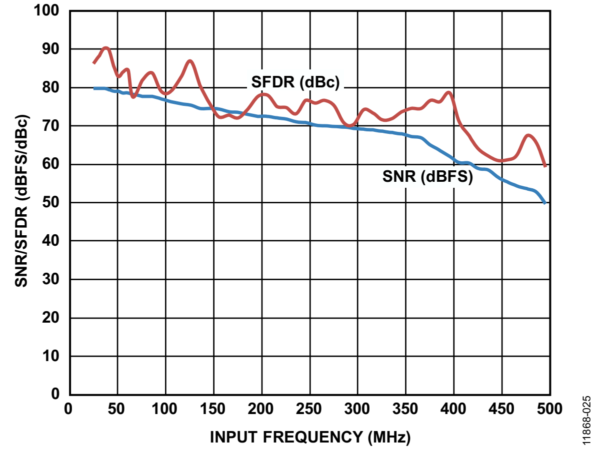

Figure 14. SNR/SFDR vs. Input Frequency (f_{IN}), f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

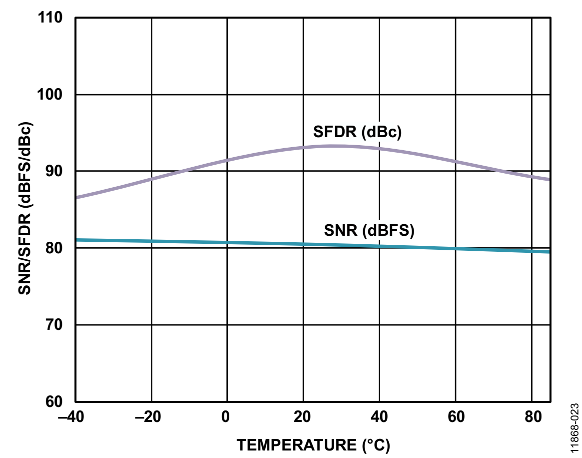

Figure 15. SNR/SFDR vs. Temperature, f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

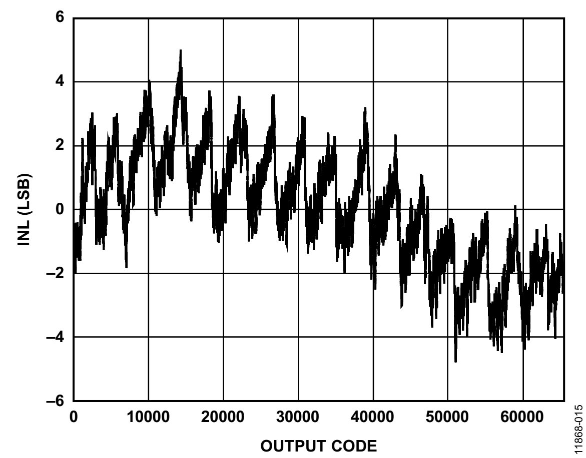

Figure 16. Integral Nonlinearity (INL), f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

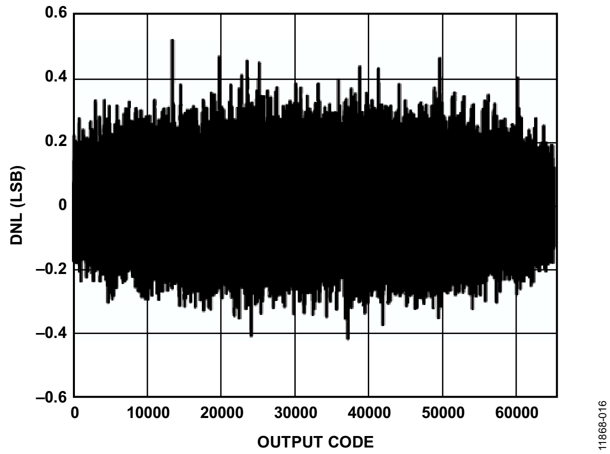

Figure 17. Differential Nonlinearity (DNL), f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

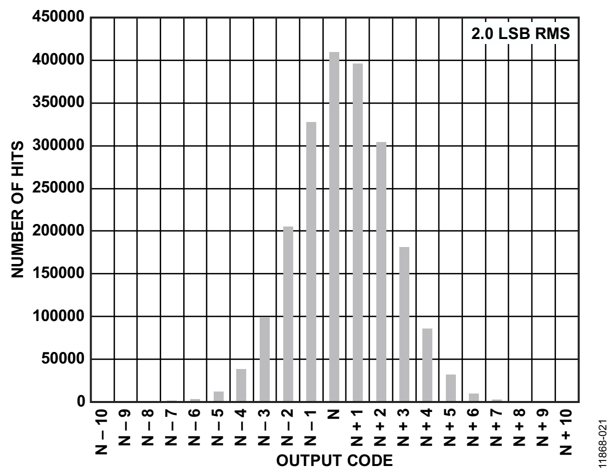

Figure 18. Input Referred Noise Histogram, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

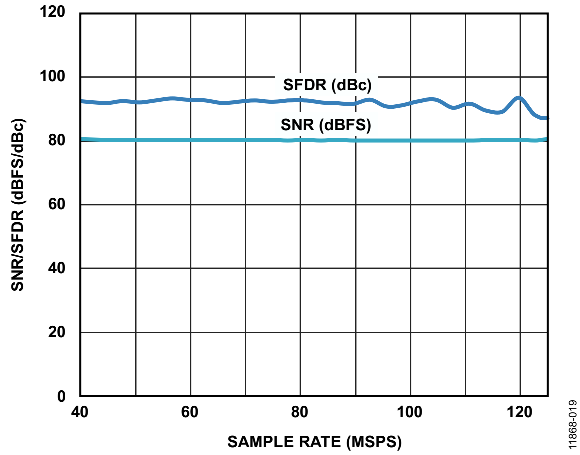

Figure 19. SNR/SFDR vs. Sample Rate, f_{IN} = 9.7 MHz, V_{REF} = 1.4 V

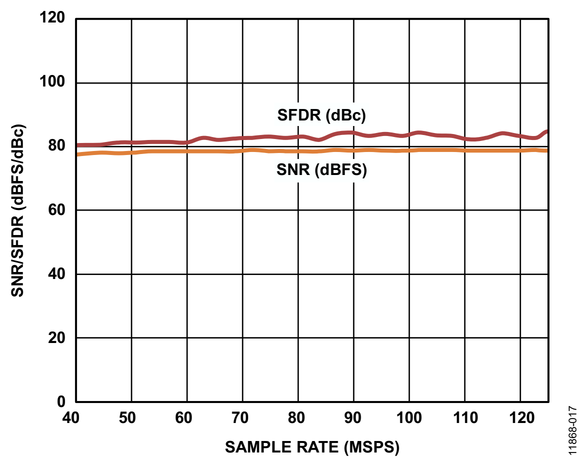

Figure 20. SNR/SFDR vs. Sample Rate, f_{IN} = 64 MHz, V_{REF} = 1.4 V

V_{REF} = 1.0 V

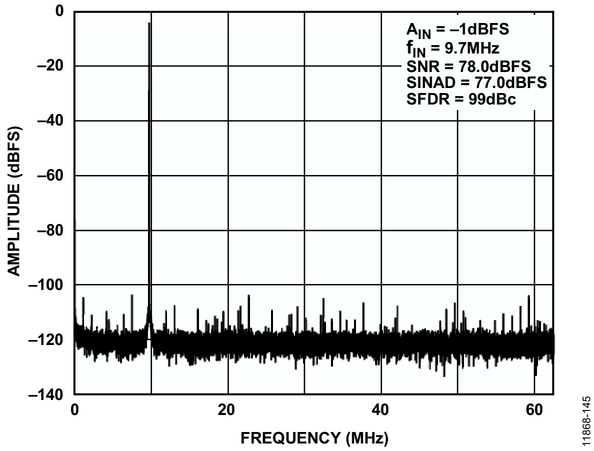

Figure 21. Single-Tone 32k FFT with f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

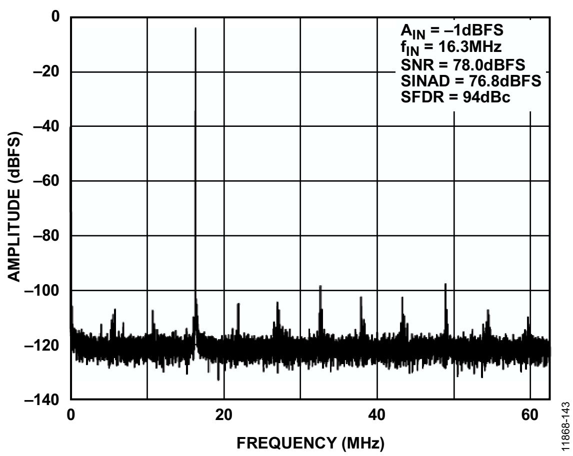

Figure 22. Single-Tone 32k FFT with f_{IN} = 16.3 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

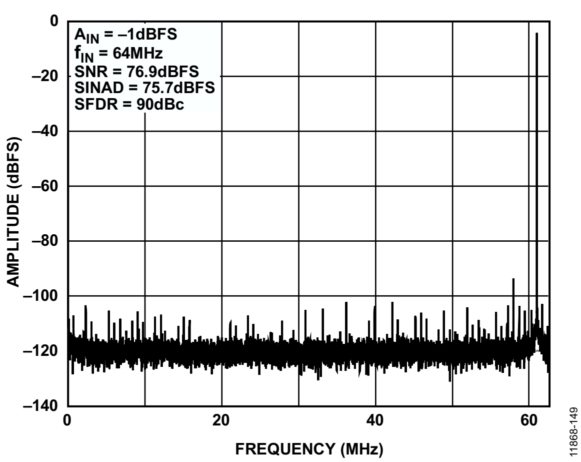

Figure 23. Single-Tone 32k FFT with f_{IN} = 64 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

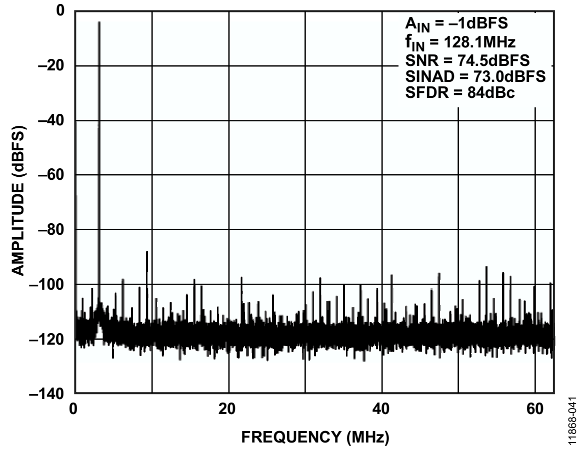

Figure 24. Single-Tone 32k FFT with f_{IN} = 128.1 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

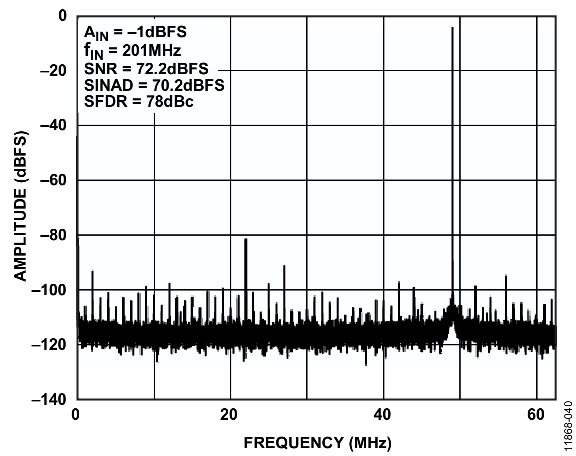

Figure 25. Single-Tone 32k FFT with f_{IN} = 201 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

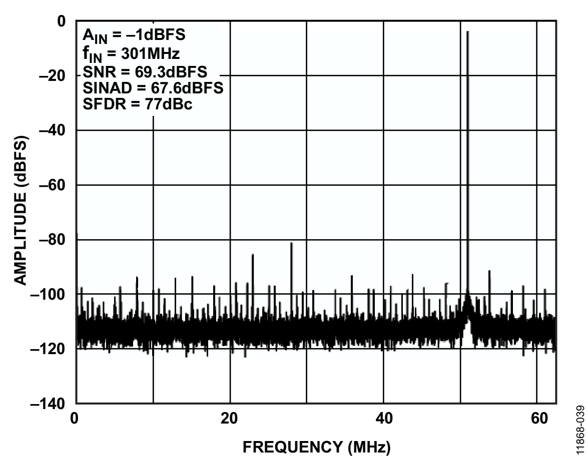

Figure 26. Single-Tone 32k FFT with f_{IN} = 301 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

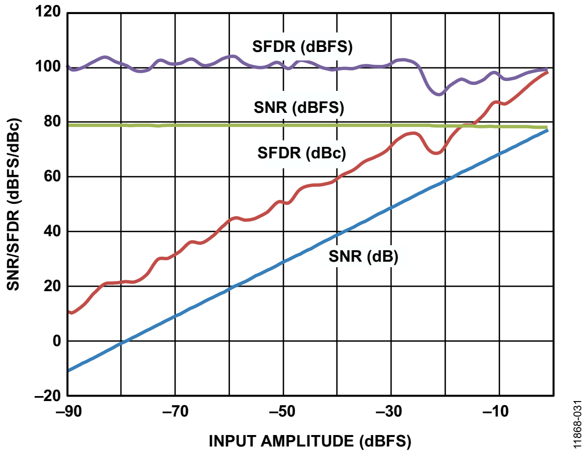

Figure 27. SNR/SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

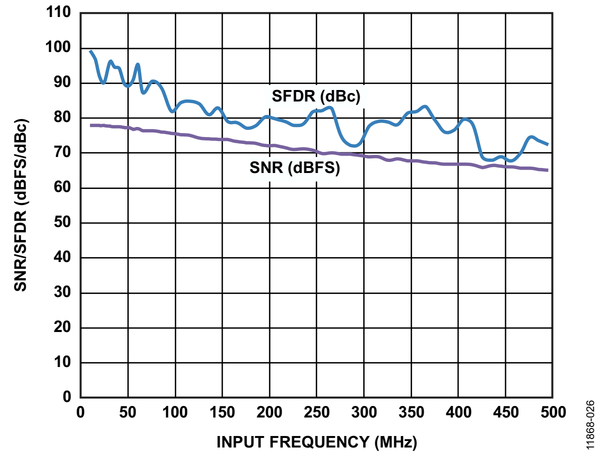

Figure 30. SNR/SFDR vs. Input Frequency (f_{IN}), f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

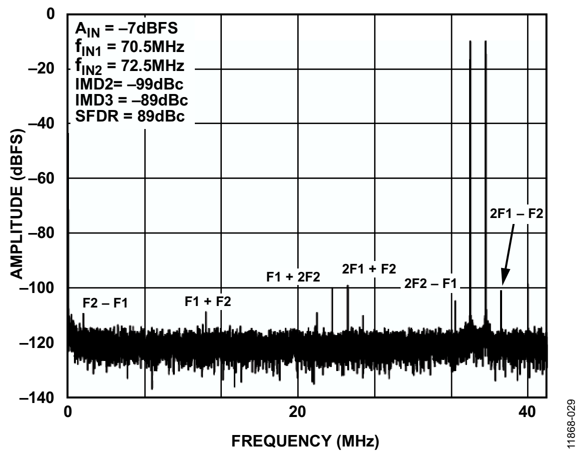

Figure 28. Two-Tone 32k FFT with f_{IN1} = 70.5 MHz and f_{IN2} = 72.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

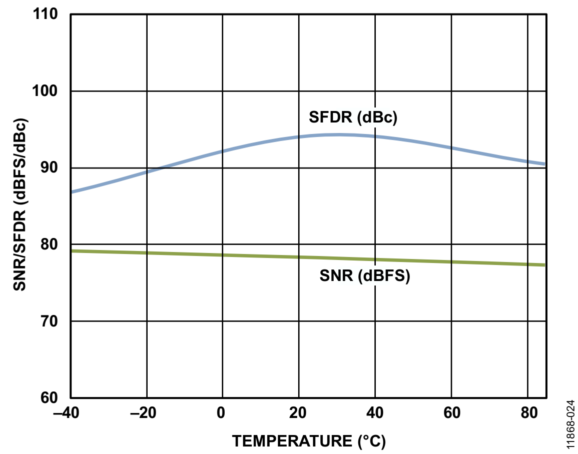

Figure 31. SNR/SFDR vs. Temperature, f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

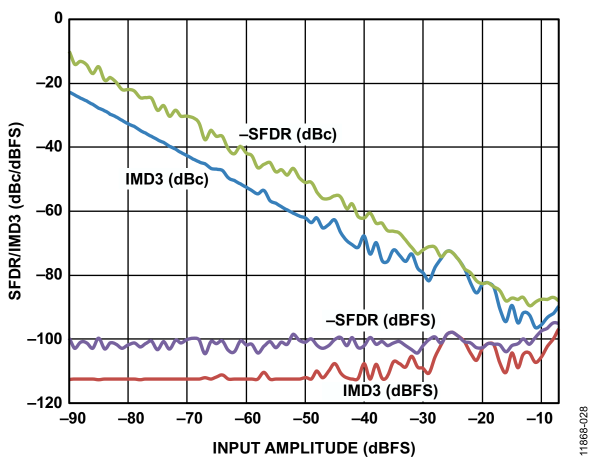

Figure 29. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 70.5 MHz and f_{IN2} = 72.5 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

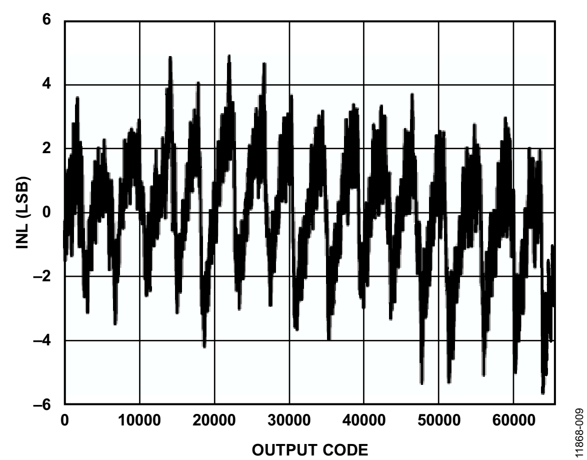

Figure 32. Integral Nonlinearity (INL), f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

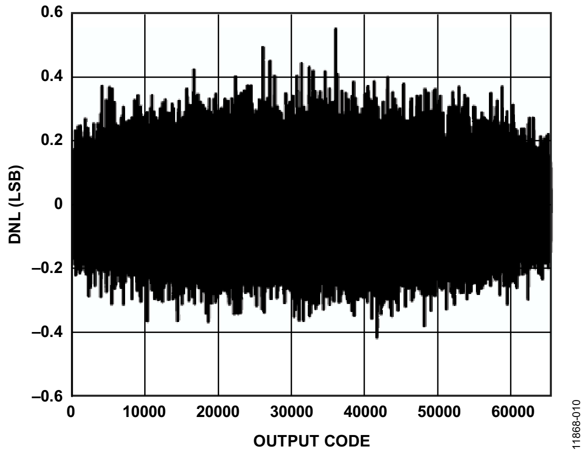

Figure 33. Differential Nonlinearity (DNL), f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

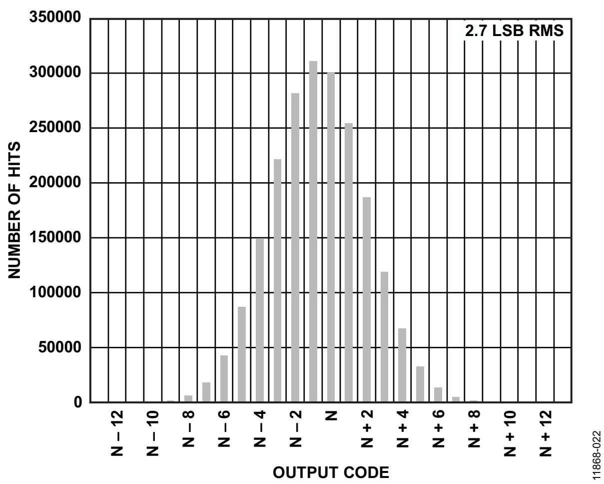

Figure 34. Input Referred Noise Histogram, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

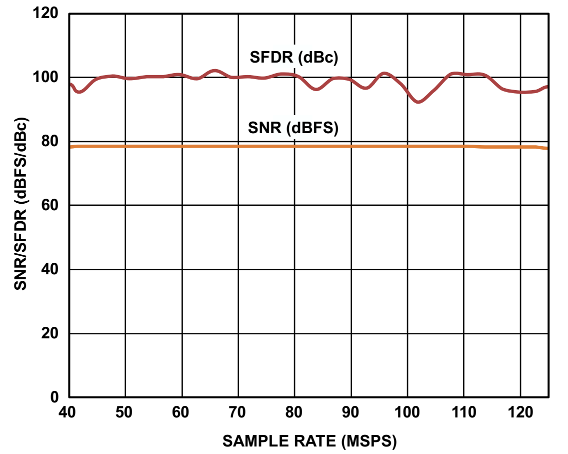

Figure 35. SNR/SFDR vs. Sample Rate, f_{IN} = 9.7 MHz, V_{REF} = 1.0 V

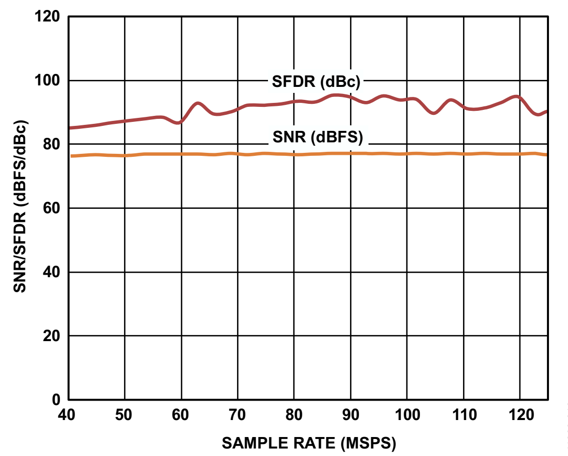

Figure 36. SNR/SFDR vs. Sample Rate, f_{IN} = 64 MHz, V_{REF} = 1.0 V

EQUIVALENT CIRCUITS

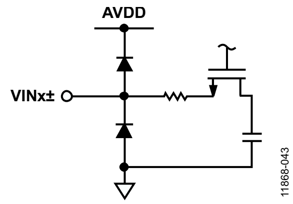

Figure 37. Equivalent Analog Input Circuit

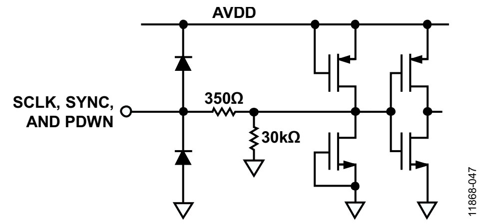

Figure 41. Equivalent SCLK, SYNC, and PDWN Input Circuit

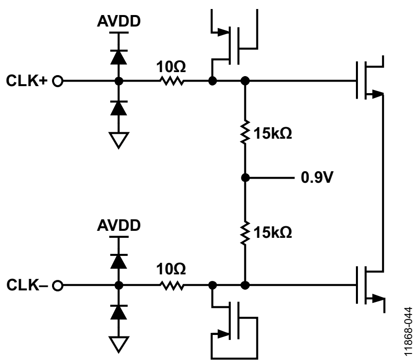

Figure 38. Equivalent Clock Input Circuit

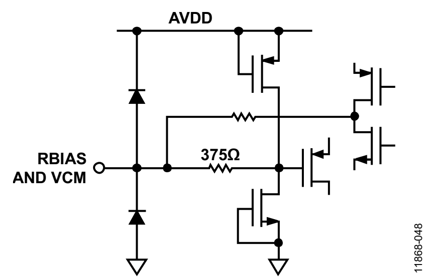

Figure 42. Equivalent RBIAS and VCM Circuit

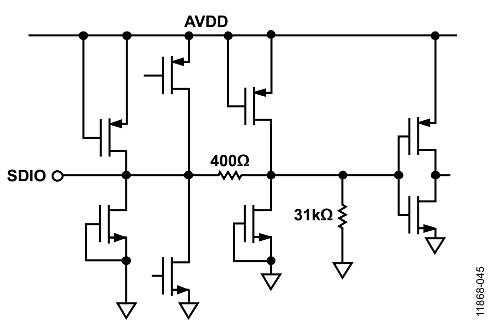

Figure 39. Equivalent SDIO Input Circuit

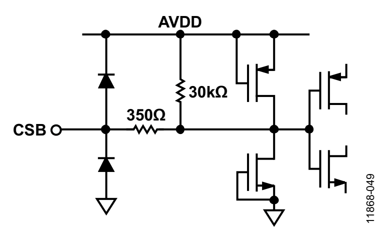

Figure 43. Equivalent CSB Input Circuit

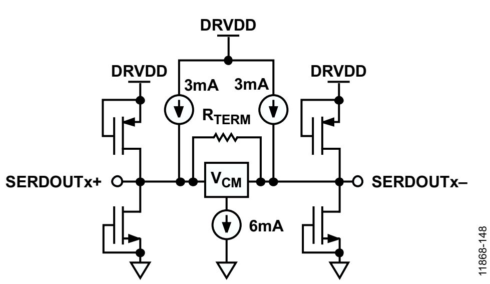

Figure 40. Equivalent SERDOUTx± Circuit

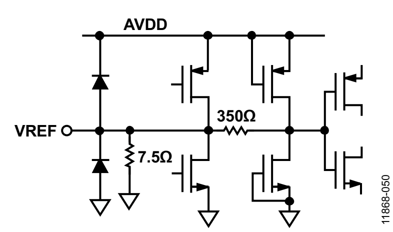

Figure 44. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9656 is a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 16-bit result in the digital correction logic. The serializer transmits this converted data in a 16-bit output. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter [MDAC]). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9656 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

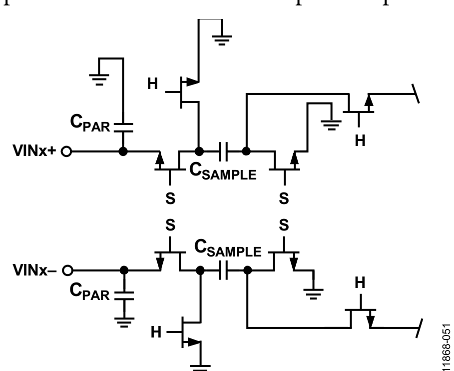

Figure 45. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 45). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and therefore achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a differential capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" for more information. In general, the precise values depend on the application.

Input Common-Mode Voltage

The analog inputs of the AD9656 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = AVDD/2 is recommended for optimum performance, but the device can function over a wider V_{CM} range with reasonable performance, as shown in Figure 46 and Figure 47.

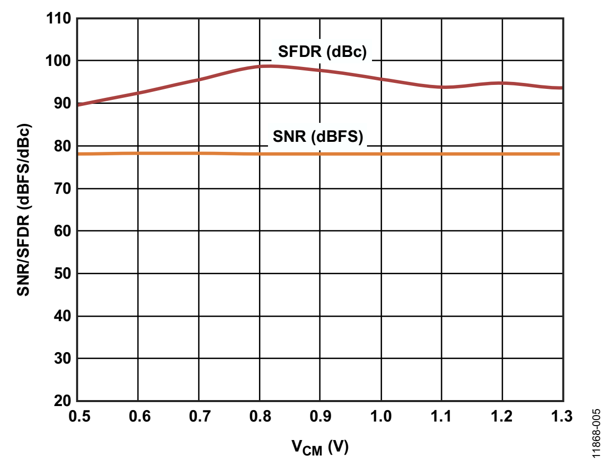

Figure 46. SNR/SFDR vs. Common-Mode Voltage (V_{CM}), f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.0 V

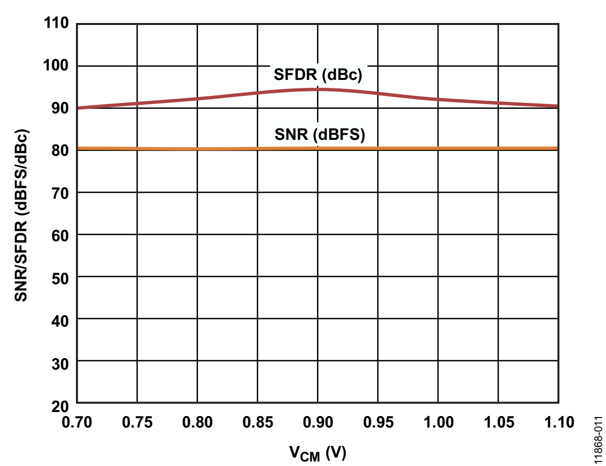

Figure 47. SNR/SFDR vs. Common-Mode Voltage (V_{CM}), f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS, V_{REF} = 1.4 V

An on-chip, common-mode voltage reference is included in the design and is available from the VCM pin. Bypass the VCM pin to ground with a 0.1 µF capacitor, as described in the Applications Information section.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9656, the input span is dependent on the reference voltage (see Table 11).

Differential Input Configurations

There are several ways to drive the AD9656 either actively or passively. However, optimum performance is achieved by driving the analog inputs differentially. Using a differential double balun configuration to drive the AD9656 provides excellent performance and a flexible interface to the ADC for baseband applications (see Figure 48).

For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration (see Figure 49) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9656.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

It is not recommended to drive the AD9656 inputs single-ended.

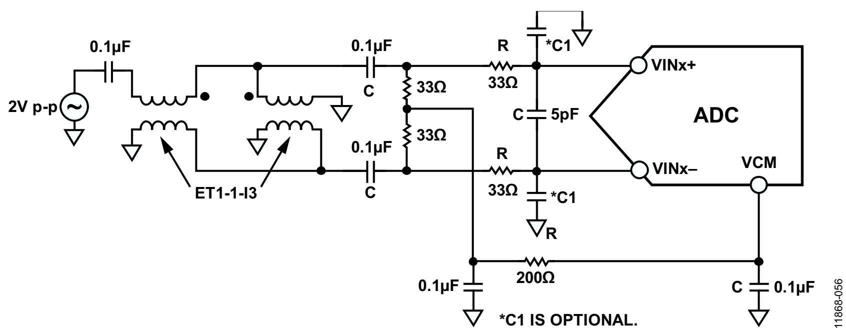

Figure 48. Differential Double Balun Input Configuration for Baseband Applications

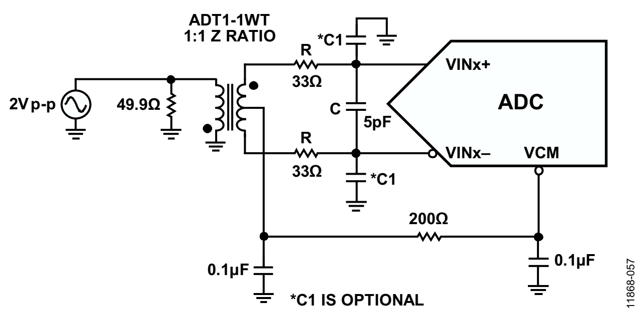

Figure 49. Differential Transformer-Coupled Configuration for Baseband Applications

Table 11. Reference Configuration Summary

Selected Mode	SENSE Voltage (V)	Resulting V_{REF} (V)	Resulting Differential Span (V p-p)
Fixed Internal Reference	AGND to 0.2 V	1.0 V to 1.4 V internal, SPI selectable with Register 0x18, Bits[7:6]	2.0 to 2.8
Programmable Internal Reference	Tie SENSE pin to external R divider (see Figure 51)	0.5 × (1 + R2/R1), for example: R1 = 3.2 kΩ, R2 = 5.8 kΩ for V_{REF} = 1.4 V	2 × V_{REF}
Fixed External Reference	AVDD	1.0 V to 1.4 V applied to external VREF pin	2.0 to 2.8

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD9656. VREF can be configured using the internal 1.0 V reference, using an externally applied 1.0 V to 1.4 V reference voltage, or using an external resistor divider applied to the internal reference to produce a user-selectable reference voltage. The reference modes are described in the Internal Reference Connection section and the External Reference Operation section. Externally bypass the VREF pin to ground with a low equivalent series resistance (ESR), 1.0 μF capacitor in parallel with a low ESR, 0.1 μF ceramic capacitor.

Internal Reference Connection

A comparator within the AD9656 detects the potential at the SENSE pin and configures the reference for one of three possible modes, which are summarized in Table 11. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 50), setting the voltage at the VREF pin, V_{REF}, to 1.0 V. If SENSE is connected to an external resistor divider (see Figure 51), V_{REF} is defined as

$$V_{REF} = 0.5 \times \left(1 + \frac{R2}{R1}\right)$$

where:

$7\ k\Omega \leq (R1 + R2) \leq 10\ k\Omega$

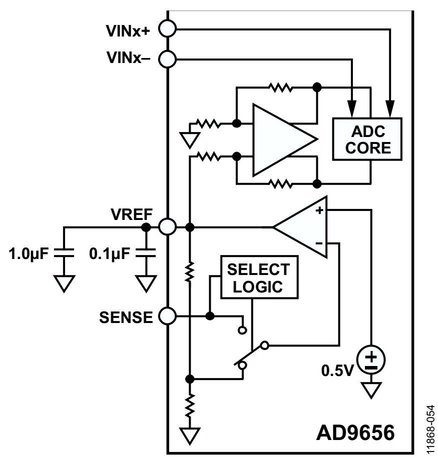

Figure 50. 1.0 V Internal Reference Configuration

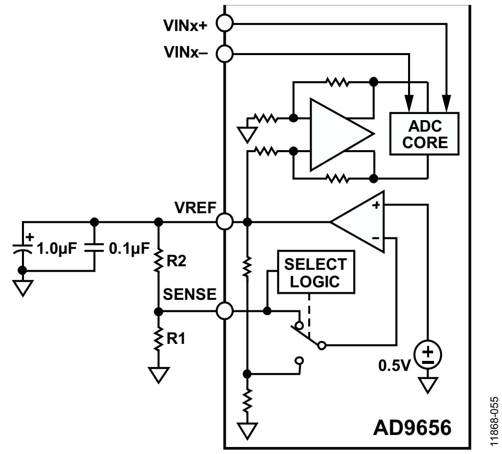

Figure 51. Programmable Internal Reference Configuration

If the internal reference of the AD9656 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 52 and Figure 53 show how the internal reference voltage is affected by loading.

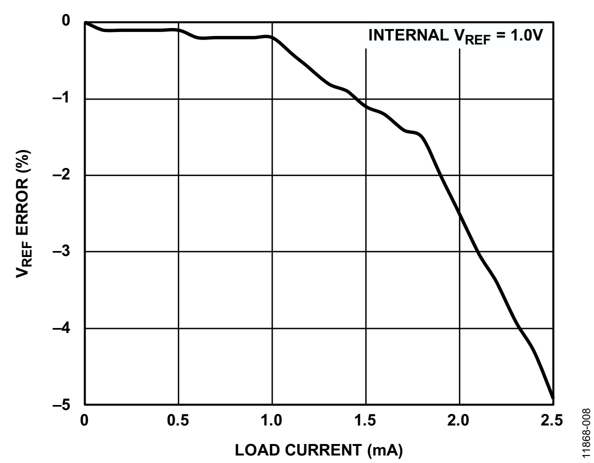

Figure 52. V_{REF} Error (Internal V_{REF} = 1.0 V) vs. Load Current

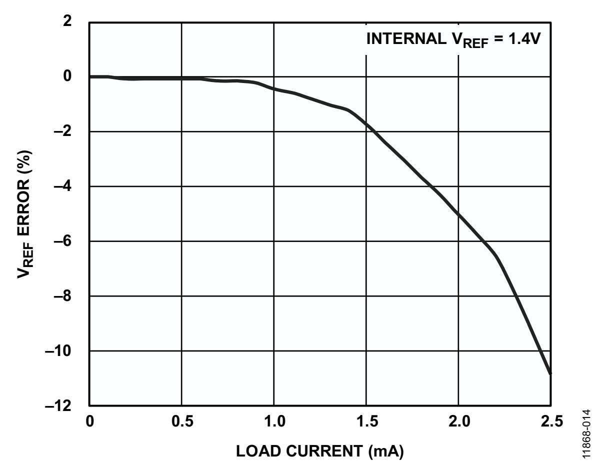

Figure 53. V_{REF} Error (Internal V_{REF} = 1.4 V) vs. Load Current

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or to improve thermal drift characteristics. Figure 54 and Figure 55 show the typical drift characteristics of the internal reference in 1.0 V mode and 1.4 V mode, respectively.

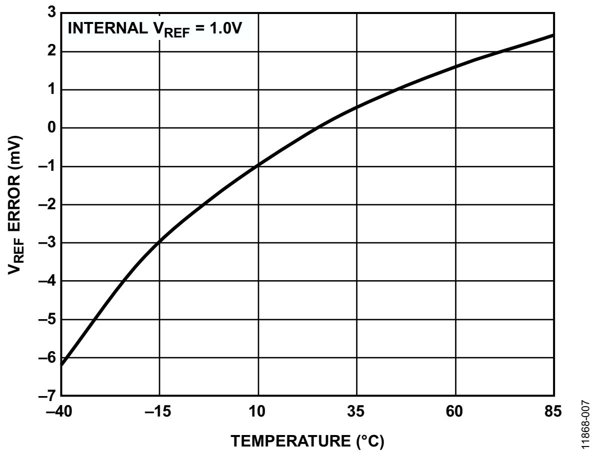

Figure 54. V_{REF} Error vs. Temperature, Typical V_{REF} = 1.0 V Drift

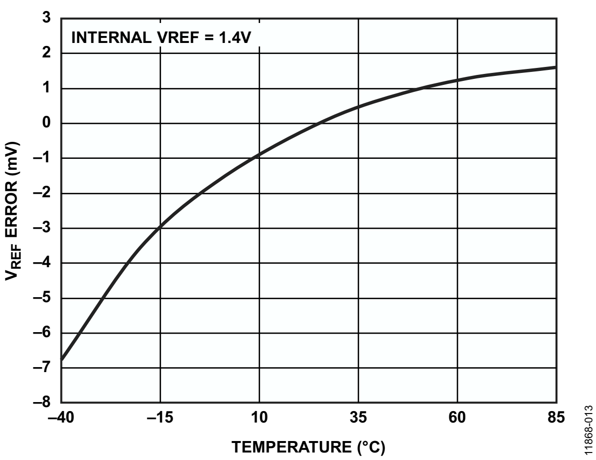

Figure 55. V_{REF} Error vs. Temperature, Typical V_{REF} = 1.4 V Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7.5 kΩ load. The internal buffer generates the positive and negative full-scale references for the ADC core.

It is not recommended to leave the SENSE pin floating.

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9656 sample clock inputs, CLK+ and CLK−, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally and require no external bias.

Clock Input Options

The AD9656 has a flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal used, clock source jitter is of the most concern, as described in the Jitter Considerations section.

Figure 56 and Figure 57 show two preferred methods for clocking the AD9656 (at clock rates up to 1 GHz prior to internal clock divider). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 1 GHz, and the RF transformer configuration is recommended for clock frequencies from 40 MHz to 200 MHz. The Schottky diodes, across the transformer/balun secondary winding limit clock excursions into the AD9656 to approximately 0.8 V p-p differential (see Figure 56 and Figure 57).

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9656 while preserving the fast rise and fall times of the signal that are critical to achieving low jitter performance. However, the diode capacitance has an effect on frequencies above 500 MHz. Care must be taken in choosing the appropriate signal limiting diode.

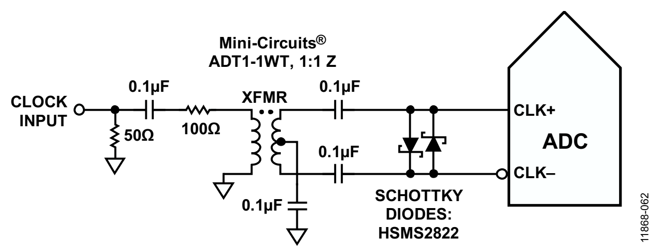

Figure 56. Transformer-Coupled Differential Clock (Up to 200 MHz)

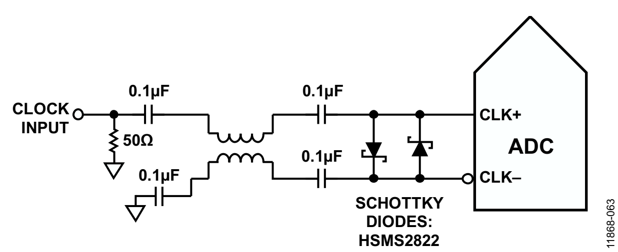

Figure 57. Balun-Coupled Differential Clock (Up to 1 GHz)

If a low jitter clock source is not available, another option is to ac-couple a differential PECL signal to the sample clock input pins, as shown in Figure 58. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers offer excellent jitter performance.

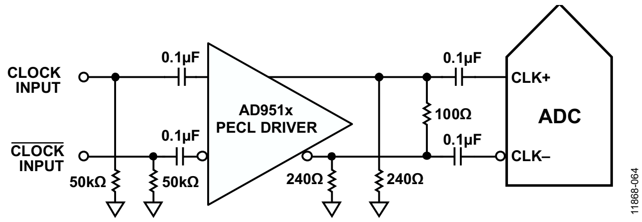

Figure 58. Differential PECL Sample Clock (Up to 1 GHz)

Another option is to ac-couple a differential LVDS signal to the sample clock input pins, as shown in Figure 59. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers offer excellent jitter performance.

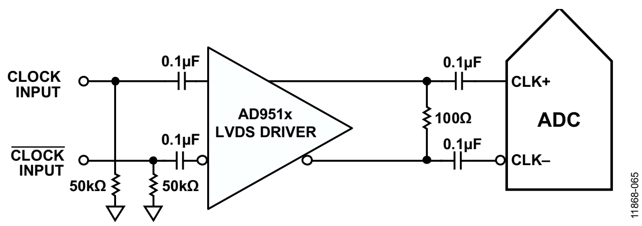

Figure 59. Differential LVDS Sample Clock (Up to 1 GHz)

In some applications, it is acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK− pin to ground with a 0.1 µF capacitor (see Figure 60).

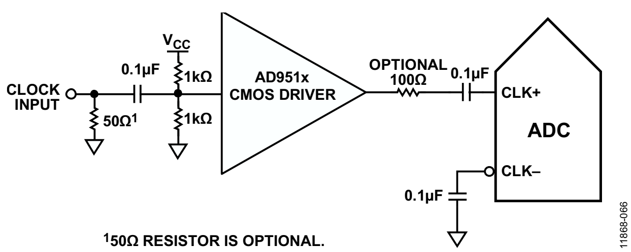

Figure 60. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD9656 contains an input clock divider with the ability to divide the input clock by integer values from 1 to 8.

The AD9656 clock divider can be synchronized using the external SYNC input. Bit 0 and Bit 1 of Register 0x109 allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, can be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9656 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This feature minimizes performance degradation in cases where the clock input duty cycle deviates more than the specified ±5% from the nominal 50% duty cycle. Enabling the DCS function can significantly improve noise and distortion performance for clock input duty cycles ranging from 30% to 45% and from 55% to 70%.

Jitter in the rising edge of the input is still of concern and is not easily reduced by the internal stabilization circuit. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR\ Degradation = 20 \log_{10}\left(\frac{1}{2\pi \times f_A \times t_J}\right)$$

In this equation, the rms aperture jitter represents the root sum square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 61).

Treat the clock input as an analog signal in cases where aperture jitter can affect the dynamic range of the AD9656. Separate power supplies for clock drivers from the supplies for the ADC output driver to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), retime it by the original clock at the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs.

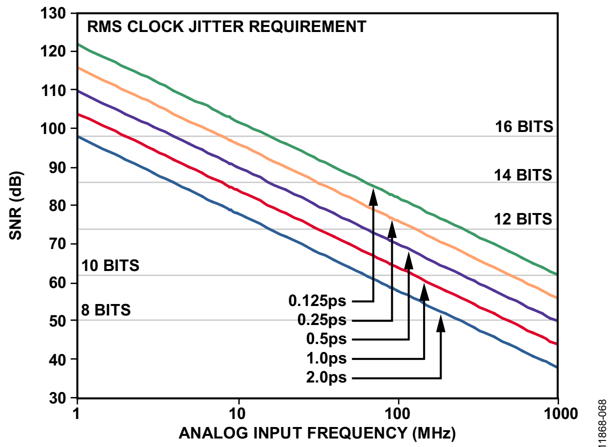

Figure 61. Ideal SNR vs. Analog Input Frequency and Jitter

POWER DISSIPATION AND POWER-DOWN MODE

As shown in Figure 62 and Figure 63, the power dissipated by the AD9656 is proportional to its sample rate.

The AD9656 is placed in power-down mode either by the SPI port or by asserting the PDWN pin high. In power-down mode, the ADC typically dissipates 14 mW. During power-down, the output drivers are placed in a high impedance state. When the PDWN pin is asserted low, the AD9656 returns to normal operating mode. Note that PDWN is referenced to the digital output driver supply (DRVDD) and must not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and must then be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode; shorter power-down cycles result in proportionally shorter wake-up times. When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map section for more information about using these features.

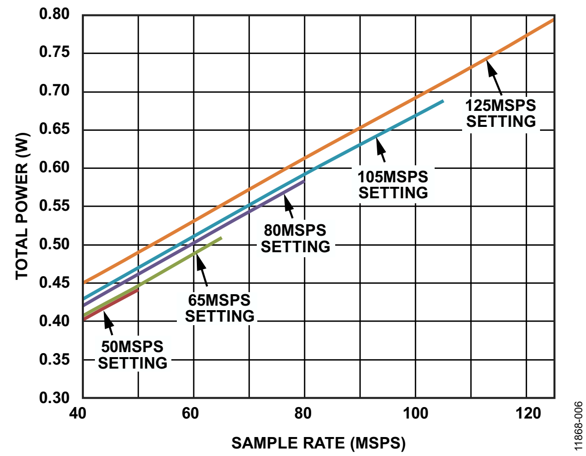

Figure 62. Total Power vs. f_{SAMPLE} for f_{IN} = 9.7 MHz, Four Channels (V_{REF} = 1.4 V)

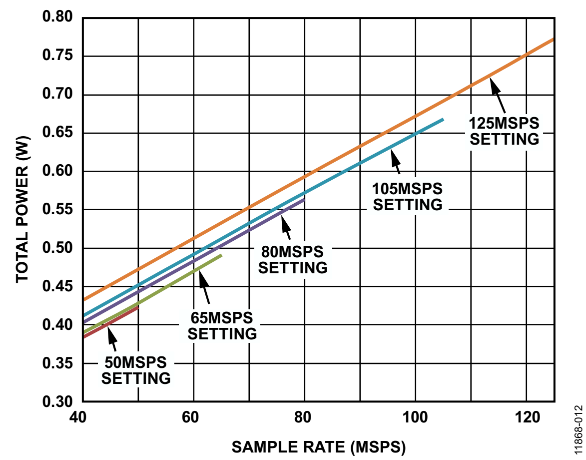

Figure 63. Total Power vs. f_{SAMPLE} for f_{IN} = 9.7 MHz, Four Channels (V_{REF} = 1.0 V)

DIGITAL OUTPUTS

JESD204B Transmit Top Level Description

The AD9656 digital output uses the JEDEC Standard No. JESD204B, *Serial Interface for Data Converters*. JESD204B is a protocol to link the AD9656 to a digital processing device over a serial interface with link speeds up to 6.4 Gbps. The benefits of the JESD204B interface include a reduction in the required board area for data interface routing and the enabling of smaller packages for converter and logic devices. The AD9656 supports single, dual, and four lane interfaces.

JESD204B Overview

The JESD204B data transmit block, JTX, assembles the parallel data from the ADC into frames and uses 8b/10b encoding, as well as optional scrambling, to form serial output data. Lane synchronization is supported using special characters during the initial establishment of the link, and additional synchronization is embedded in the data stream thereafter. A matching external receiver is required to lock onto the serial data stream and recover the data and clock. For additional information about the JESD204B interface, refer to the JESD204B standard.

The AD9656 JESD204B transmit block maps the output of the four ADCs over a link. A link can be configured to use either single, dual, or four serial differential outputs, which are called lanes. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (AD9656 output) and receiver.

The JESD204B link is described according to the following parameters:

- S = samples transmitted/single converter/frame cycle (AD9656 value = 1)
- M = number of converters/converter device (AD9656 value = 4)
- L = number of lanes/converter device (AD9656 value = 1, 2, or 4)
- N = converter resolution (AD9656 value = 16)
- N' = total number of bits per sample (AD9656 value = 16)
- CF = number of control words/frame clock cycle/converter device (AD9656 value = 0)
- CS = number of control bits/conversion sample (AD9656 value = 0)
- K = number of frames per multiframe (configurable on the AD9656)
- HD = high density mode (AD9656 value = 0)
- F = octets/frame (AD9656 value = 2, 4, or 8, dependent upon L = 4, 2, or 1)
- C = control bit (overrange, overflow, underflow; unavailable in the AD9656 default mode)
- T = tail bit (unavailable in the AD9656 default mode)
- SCR = scrambler enable/disable (configurable on the AD9656)
- FCHK = checksum for the JESD204B parameters (automatically calculated and stored in the register map)

Figure 64 shows a simplified block diagram of the AD9656 JESD204B link. By default, the AD9656 is configured to use four converters and one lane. The AD9656 allows for other configurations such as combining the outputs of two of the four converters onto a single lane resulting in the data from the four converters being output on two lanes. The mapping of the 0, 1, 2, and 3 digital output paths can be changed. These modes are set up through a quick configuration register in the SPI register map, along with additional customizable options.

By default in the AD9656, the 16-bit word from each converter is divided into two octets (8 bits of data each). Bit 0 (MSB) through Bit 7 are in the first octet, and Bit 8 through Bit 15 (LSB) are the second octet.

The two resulting octets can be scrambled. Scrambling is optional; however, it is available to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self synchronizing, polynomial-based algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver must be a self synchronizing version of the scrambler polynomial.

The two octets are then encoded with an 8b/10b encoder. The 8b/10b encoder works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol. Figure 65 shows how the 16-bit data is output from the ADC, the two octets are scrambled, and how the octets are encoded into two 10-bit symbols. Figure 65 illustrates the default data format.

At the data link layer, in addition to the 8b/10b encoding, character replacement is used to allow the receiver to monitor frame alignment. The character replacement process occurs on the frame and multiframe boundaries, and implementation depends on which boundary is occurring and if scrambling is enabled.

If scrambling is disabled, the following applies. If the last scrambled octet of the last frame of the multiframe equals the last octet of the previous frame, the transmitter replaces the last octet with the control character /A/ = /K28.3/. On other frames within the multiframe, if the last octet in the frame equals the last octet of the previous frame, the transmitter replaces the last octet with the control character /F/= /K28.7/.

If scrambling is enabled, the following applies. If the last octet of the last frame of the multiframe equals 0x7C, the transmitter replaces the last octet with the control character /A/ = /K28.3/. On other frames within the multiframe, if the last octet equals 0xFC, the transmitter replaces the last octet with the control character /F/ = /K28.7/.

Refer to JEDEC Standard No. JESD204B (July 2011) for additional information about the JESD204B interface. Section 5.1 covers the transport layer and data format details, and Section 5.2 covers scrambling and descrambling.

JESD204B Synchronization Details

The AD9656 is a JESD204B Subclass 1 device and establishes synchronization of the link through two control signals (DSYSREF and DSYNC). At the system level, multiple converter devices are aligned using a common DSYSREF and device clock (CLK).

The synchronization process is accomplished over three phases: code group synchronization (CGS), initial lane alignment sequence (ILAS), and data transmission. If scrambling is enabled, the bits are not actually scrambled until the data transmission phase, and the CGS phase and ILAS phase do not use scrambling.

CGS Phase

In the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver (external logic device) must find K28.5 characters in its input data stream using clock and data recovery (CDR) techniques.

When a certain number of consecutive K28.5 characters are detected on the link lanes, the receiver initiates a DSYSREF edge so that the AD9656 transmit data establishes a local multiframe clock (LMFC) internally.

The DSYSREF edge also resets any sampling edges within the ADC to align sampling instances to the LMFC. This is important to maintain synchronization across multiple devices.

The receiver or logic device deasserts the SYNC~ signal applied to DSYNC, and the transmitter block begins the ILAS phase.

ILAS Phase

In the ILAS phase, the transmitter sends out a known pattern, and the receiver aligns all lanes of the link and verifies the parameters of the link.

The ILAS phase begins after SYNC~ has been deasserted (goes high). The transmit block begins to transmit four multiframes. Dummy samples are inserted between the required characters so that full multiframes are transmitted. The four multiframes include the following:

- Multiframe 1: Begins with an /R/ character [K28.0] and ends with an /A/ character [K28.3].
- Multiframe 2: Begins with an /R/ character followed by a /Q/ [K28.4] character, followed by link configuration parameters over 14 configuration octets (see Table 12), and ends with an /A/ character.
- Multiframe 3: same as Multiframe 1.
- Multiframe 4: same as Multiframe 1.

Table 12. 14 Configuration Octets of the ILAS Phase

No.	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	DID[7:0]							
1					BID[3:0]			
2				LID[4:0]				
3	SCR			L[4:0]				
4	F[7:0]							
5				K[4:0]				
6	M[7:0]							
7	CS[1:0]			N[4:0]				
8	SUBCLASS[2:0]			N′[4:0]				
9	JESDV[2:0]			S[4:0]				
10				CF[4:0]				
11	Reserved, don't care (RES1)							
12	Reserved, don't care (RES2)							
13	FCHK[7:0]							

Data Transmission Phase

In the data transmission phase, frame alignment is monitored with control characters. Character replacement is used at the end of frames. Character replacement in the transmitter occurs in the following instances:

- If scrambling is disabled and the last octet of the frame or multiframe equals the octet value of the previous frame.
- If scrambling is enabled and the last octet of the multiframe is equal to 0x7C, or the last octet of a frame is equal to 0xFC.

Link Setup Parameters

The following demonstrates how to configure the AD9656 JESD204B interface. The steps to configure the output include the following:

1. Disable the lanes before changing configuration.
2. Select one quick configuration option.
3. Configure the detailed options.
4. Check FCHK, checksum of JESD204B interface parameters.
5. Set additional digital output configuration options.
6. Reenable the lane(s).

Disable Lanes Before Changing Configuration

Before modifying the JESD204B link parameters, disable the link and hold it in reset. This is accomplished by writing Logic 1 to Register 0x5F, Bit 0.

Select Quick Configuration Option

Write to Register 0x5E, the JESD204B quick configuration register to select the configuration options. See Table 15 for the configuration options and resulting JESD204B parameter values.

- 0x41 = four converters, one lane
- 0x42 = four converters, two lanes
- 0x44 = four converters, four lanes
- 0x21 = two converters, one lane
- 0x22 = two converters, two lanes
- 0x11 = one converter, one lane

Configure Detailed Options

Configure the tail bits and control bits.

- With N' = 16 and N = 14 (nondefault configuration), two bits are available per sample for transmitting additional information over the JESD204B link. The options are tail bits or control bits. By default, tail bits of 0b00 value are used.
- Tail bits are dummy bits sent over the link to complete the two octets and do not convey any information about the input signal. Tail bits can be fixed zeros (default) or pseudo-random numbers (Register 0x5F, Bit 6).
- One or two control bits can be selected to replace the tail bits using Register 0x72, Bits[7:6]. The meaning of the control bits can be set using Register 0x14, Bits[7:5].

Set lane identification values.

- JESD204B allows parameters to identify the device and lane. These parameters are transmitted during the ILAS phase, and they are accessible in the internal registers.
- The three identification values are device identification (DID), bank identification (BID), and lane identification (LID). DID and BID are device specific; therefore, they can be used for link identification.

Set the number of frames per multiframe, K.

- Per the JESD204B specification, a multiframe is defined as a group of K successive frames, where K is from 1 t0 32, and requires that the number of octets be from 17 to 1024. The K value is set to 32 by default in Register 0x70, Bits[4:0]. Note that the K value is the register value plus 1.
- The K value can be changed; however, it must comply with a few conditions. The AD9656 uses a fixed value for octets per frame [F] based on the JESD204B quick configuration setting. K must also be a multiple of 4 and conform to the following equation:

  $32 \geq K \geq Ceil\ (17/F)$

- The JESD204B specification also specifies that the number of octets per multiframe (K × F) be from 17 to 1024. The F value is fixed through the quick configuration setting to ensure that this relationship is true.

Table 13. JESD204B Configurable Identification Values

DID Value	Register, Bits	Value Range
LID (Lane 0)	0x66, [4:0]	0…31
LID (Lane 1)	0x67, [4:0]	0…31
DID	0x64, [7:0]	0…255
BID	0x65, [3:0]	0…15

Scramble, SCR.

- Scrambling can be enabled or disabled by setting Register 0x6E, Bit 7. By default, scrambling is enabled. Per the JESD204B protocol, scrambling is functional only after the lane synchronization has completed.

Select lane synchronization options.

Most of the synchronization features of the JESD204B interface are enabled by default for typical applications. In some cases, these features can be disabled or modified as follows:

- ILAS enabling is controlled in Register 0x5F, Bits[3:2] and is enabled by default. Optionally, to support some unique instances of the interfaces (such as NMCDA-SL), the JESD204B interface can be programmed to either disable the ILAS sequence or continually repeat the ILAS sequence.

The AD9656 has fixed values for some JESD204B interface parameters, and they are as follows:

- [N'] = 16: number of bits per sample is 16, in Register 0x73, Bits[4:0]
- [CF] = 0: number of control words/frame clock cycle/converter is 0, in Register 0x75, Bits[4:0]

Verify read only values: lanes per link (L), octets per frame (F), number of converters (M), and samples per converter per frame (S). The AD9656 calculates values for some JESD204B parameters based on other settings, particularly the quick configuration register selection. The following read only values are available in the register map for verification.

- [L] = lanes per link can be 1, 2 or 4; read the values from Register 0x6E, Bits [4:0]
- [F] = octets per frame can be 2, 4, or 8; read the value from Register 0x6F, Bits[7:0]
- [HD] = high density mode is 0; read the value from Register 0x75, Bit 7
- [M] = number of converters per link; default is 4, but can be 1, 2, or 4. Read the value from Register 0x71, Bits[7:0]
- [S] = samples per converter per frame is 1; read the value from Register 0x74, Bits[4:0]

Check FCHK, Checksum of JESD204B Interface Parameters

The JESD204B parameters can be verified through the checksum value [FCHK] of the JESD204B interface parameters. Each lane has a FCHK value associated with it. The FCHK value is transmitted during the ILAS second multiframe and can be read from the internal registers.

The checksum value is the modulo 256 sum of the parameters listed in the No. column of Table 14. The checksum is calculated by adding the parameter fields before they are packed into the octets shown in Table 14.

The FCHK for the lane configuration for data exiting Lane 0 can be read from Register 0x78. Similarly, the FCHK for the lane configuration for data exiting Lane 1 can be read from Register 0x79, FCHK for Lane 2 can be read from Register 0x7A, and FCHK for Lane 3 can be read from Register 0x7B.

Table 14. JESD204B Configuration Table Used in ILAS and CHKSUM Calculation

No.	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	DID[7:0]							
1					BID[3:0]			
2				LID[4:0]				
3	SCR			L[4:0]				
4	F[7:0]							
5				K[4:0]				
6	M[7:0]							
7	CS[1:0]			N[4:0]				
8	SUBCLASS[2:0]			N'[4:0]				
9	JESDV[2:0]			S[4:0]				
10				CF[4:0]				

Set Additional Digital Output Configuration Options

Other data format controls include the following:

- Invert polarity of serial output data: Register 0x60, Bit 1
- ADC data format (offset binary or twos complement): Register 0x14, Bits[1:0]
- Options for interpreting signal on DSYSREF and DSYNC: Register 0x3A, Bits[4:3]
- Option to remap converter (logical lane) and SERDOUTx± (physical lane) assignments: Register 0x82 and Register 0x83. See Figure 64 for a simplified block diagram.

Reenable Lanes After Configuration

After modifying the JESD204B link parameters, enable the link so that the synchronization process can begin. This is accomplished by writing Logic 0 to Register 0x5F, Bit 0.

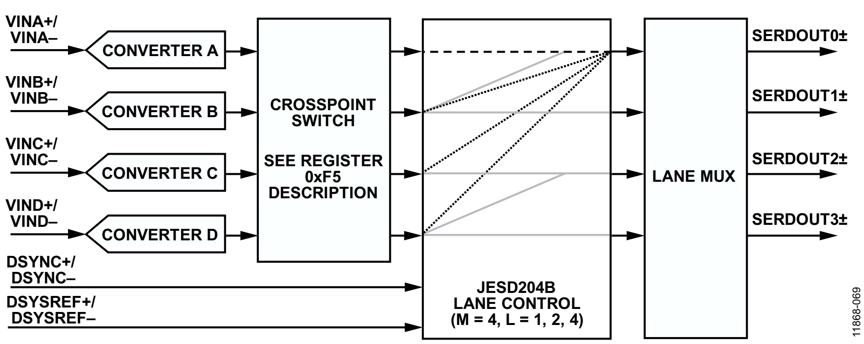

Figure 64. AD9656 Transmit Link Simplified Block Diagram

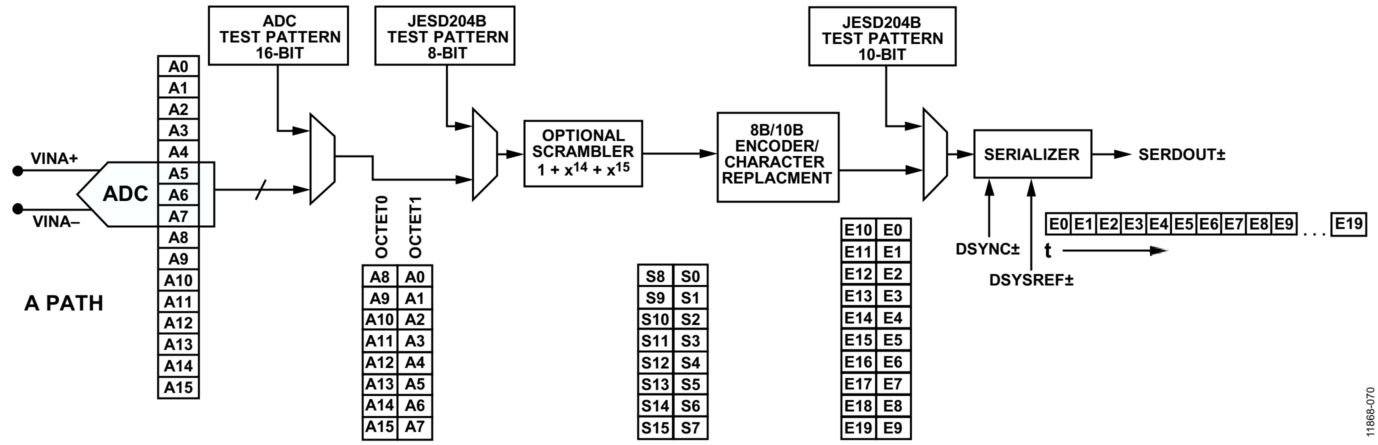

Figure 65. AD9656 Digital Processing of JESD204B Lanes

Table 15. AD9656 JESD204B Typical Configurations

JESD204B Quick Configuration Setting, Register 0x5E	M (No. of Converters), Register 0x71, Bits[7:0]	L (No. of Lanes), Register 0x6E, Bits[4:0]	F (Octets/Frame), Register 0x6F, Bits[7:0], Read Only	S (Samples/ADC/Frame), Register 0x74, Bits[4:0], Read Only	HD (High Density Mode), Register 0x75, Bit[7], Read Only
0x41	4	1	8	1	0
0x42	4	2	4	1	0
0x44	4	4	2	1	0
0x22	2	2	2	1	0
0x21	2	1	4	1	0
0x11	1	1	2	1	0

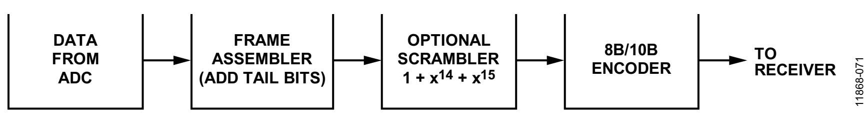

Figure 66. AD9656 ADC Output Data Path

Table 16. AD9656 JESD204B Frame Alignment Monitoring and Correction Replacement Characters

Scrambling	Lane Synchronization	Character to be Replaced	Last Octet in Multiframe	Replacement Character
Off	On	Last octet in frame repeated from previous frame	No	K28.7
Off	On	Last octet in frame repeated from previous frame	Yes	K28.3
Off	Off	Last octet in frame repeated from previous frame	Not applicable	K28.7
On	On	Last octet in frame equals D28.7	No	K28.7
On	On	Last octet in frame equals D28.3	Yes	K28.3
On	Off	Last octet in frame equals D28.7	Not applicable	K28.7

Frame and Lane Alignment Monitoring and Correction

Frame alignment monitoring and correction is part of the JESD204B specification. The 16-bit word requires two octets to transmit all the data. The two octets (MSB and LSB), where F = 2, make up a frame. During normal operating conditions, frame alignment is monitored via alignment characters, which are inserted under certain conditions at the end of a frame. Table 16 summarizes the conditions for character insertion, along with the expected characters under the various operation modes. If lane synchronization is enabled, the replacement character value depends on whether the octet is at the end of a frame or at the end of a multiframe.

Based on the operating mode, the receiver can ensure that it is still synchronized to the frame boundary by correctly receiving the replacement characters.

Digital Outputs and Timing

The AD9656 has differential digital outputs that power up by default. The driver current is derived on chip and sets the output current at each output equal to a nominal 4 mA. Each output presents a 100 Ω dynamic internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver input to result in a nominal 600 mV p-p differential swing at the receiver (see Figure 67). Alternatively, single-ended 50 Ω termination can be used. When single-ended termination is used, the termination voltage must be DRVDD/2; otherwise, ac coupling capacitors can be used to terminate to any single-ended voltage.

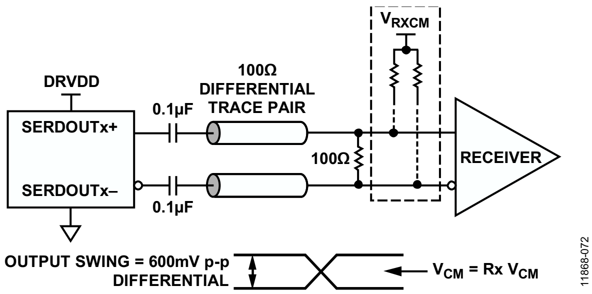

Figure 67. AC-Coupled Digital Output Termination Example

The AD9656 digital outputs can interface with custom ASICs and FPGA receivers, providing superior switching performance in noisy environments. Single point-to-point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver logic as possible. The common mode of the digital output automatically biases itself to half the supply of the receiver (that is, the common-mode voltage is 0.9 V for a receiver supply of 1.8 V) if a dc-coupled connection is used (see Figure 68). For receiver logic that is not within the bounds of the DRVDD supply, use an ac-coupled connection. Place a 0.1 µF capacitor on each output pin and derive a 100 Ω differential termination close to the receiver side.

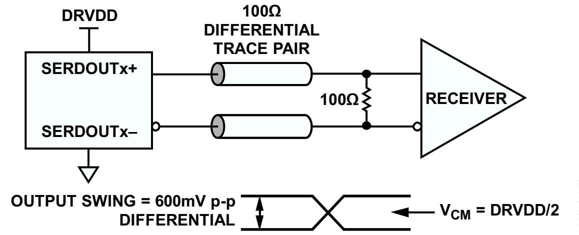

Figure 68. DC-Coupled Digital Output Termination Example

If there is no far-end receiver termination, or if there is poor differential trace routing, timing errors can result. To avoid such timing errors, it is recommended that the trace length be less than six inches, and that the differential output traces be close together and of equal lengths.

Figure 69 shows an example of the digital output data eye and time interval error (TIE) jitter histogram and bathtub curve for the AD9656 lane running at 6.4 Gbps.

Additional SPI options allow the user to further increase the output driver voltage swing of all four outputs to drive longer trace lengths (see Register 0x15 in Table 19). The power dissipation of the DRVDD supply increases when this option is used. See the Memory Map section for more information.

The format of the output data is twos complement by default. To change the output data format to offset binary, see the Memory Map section and Register 0x14 in Table 19.

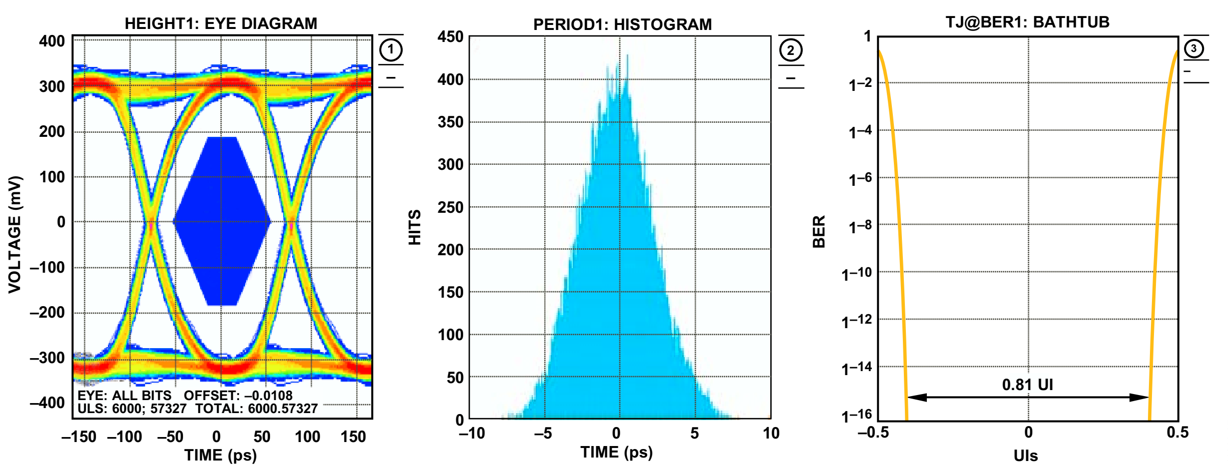

Figure 69. AD9656 Digital Outputs Data Eye, Histogram, and Bathtub, External 100 Ω Terminations at 6.4 Gbps

SERIAL PORT INTERFACE (SPI)

The AD9656 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For general operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 17). The SCLK (serial clock) pin is used to synchronize the read and write data presented from/to the ADC. The SDIO (serial data input/output) pin is a dual purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 17. Serial Port Interface Pins

Pin	Function
SCLK	Serial Clock. The serial shift clock input, which is used to synchronize serial interface reads and writes.
SDIO	Serial Data Input/Output. A dual purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip Select Bar. An active low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 70 and Table 7.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB pin can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and the W1 bits.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Input data is registed on the rising edge of SCLK, and output data is transmited on the falling edge. After the address information passes to the converter that is requesting a read, the SDIO line transitions from an input to an output within one-half of a clock cycle. This timing ensures that when the falling edge of the next clock cycle occurs, data can be safely placed on this serial line for the controller to read.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 17 make up the physical interface between the user programming device and the serial port of the AD9656. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

When the full dynamic performance of the converter is required, do not activate the SPI port. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9656 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 18 provides a brief description of the features that are accessible via the SPI. These features are described in general in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. The AD9656 part-specific features are described in the Memory Map Register Descriptions section. Information in the AD9656 data sheet takes precedence over information in AN-877 Application Note, where it relates to the AD9656.

Table 18. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the duty cycle stabilizer via the SPI
Offset	Allows the user to digitally adjust the converter offset
Test Input/Output	Allows the user to set test modes to place known data on the output bits
Output Mode	Allows the user to set up the outputs
VREF	Allows the user to set the reference voltage

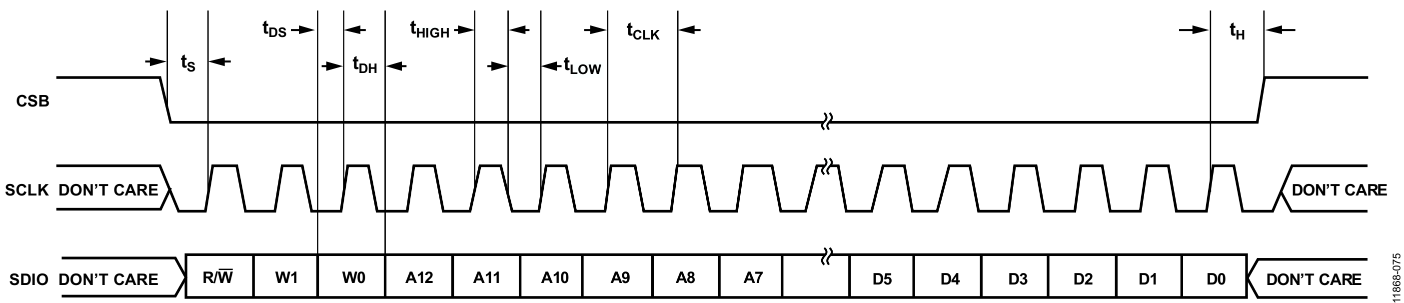

Figure 70. Serial Port Interface Timing Diagram

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into three sections: the chip configuration registers (Address 0x00 to Address 0x02); the channel index and transfer registers (Address 0x05 and Address 0xFF); and the ADC functions registers, including setup, control, and test (Address 0x08 to Address 0x10A).

The memory map register table (see Table 19) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x14, the output mode register, has a hexadecimal default value of 0x01. This means that Bit 0 = 1 and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For general information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. See Table 19 for SPI register information specific to the AD9656.

Open and Reserved Locations

All address and bit locations that are not included in Table 19 are not supported for this device. Write 0s to unused bits of a valid address location. Writing to these locations is required only when part of an address location is open (for example, Address 0x18). If the entire address location is open (for example, Address 0x13), do not write to this address location.

Default Values

After the AD9656 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table (see Table 19).

Logic Levels

An explanation of logic level terminology follows:

- “Bit is set” is synonymous with “bit is set to Logic 1” or “writing Logic 1 for the bit.”
- “Clear a bit” is synonymous with “bit is set to Logic 0” or “writing Logic 0 for the bit.”

Channel-Specific Registers

Some channel setup functions can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 19 as local. These local registers and bits can be accessed by setting the appropriate Channel 0, Channel 1, Channel 2, or Channel 3 bit in Register 0x05. If four bits are set, the subsequent write affects the registers of all four channels. In a read cycle, set only one of the channels to read one of the four registers. If all bits are set during an SPI read cycle, the device returns the value for Channel 0. Registers and bits designated as global in Table 19 affect the entire device and the channel features for which independent settings are not allowed between channels. The settings in Register 0x05 do not affect the global registers and bits.

MEMORY MAP REGISTER TABLE

The AD9656 uses a 3-wire interface and 16-bit addressing. Bit 0 and Bit 7 in Register 0x00 are set to 0, and Bit 3 and Bit 4 are set to 1. When Bit 5 in Register 0x00 is set high, the SPI enters a soft reset, where all of the user registers revert to their default values and Bit 2 is automatically cleared.

Table 19. Memory Map Registers (SPI Registers/Bits Not Labeled Local Are Global)

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Notes/ Comments
Chip Configuration Registers											
0x00	SPI port configuration	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	
0x01	Chip ID	8-bit chip ID[7:0]; AD9656 = 0xC0 (quad, 16-bit, 125 MSPS, JESD204B)								0xC0	Read only.
0x02	Chip grade	Open	Speed grade ID[6:4]; 110 = 125 MSPS			Open	Open	Open	Open	0x60	Read only.
Channel Index and Transfer Registers											
0x05	Device index	Open	Open	Open	Open	Data Channel 3	Data Channel 2	Data Channel 1	Data Channel 0	0x0F	
0xFF	Transfer	Open	Open	Open	Open	Open	Open	Open	Initiate Register 0x100 override (self-clearing)	0x00	
ADC Functions											
0x08	Power modes	Open	Open	PDWN pin function: 0 = full power-down, 1 = standby	JTX standby mode: 0 = ignore standby, 1 = do not ignore standby	Reserved		Power mode: 00 = normal operation, 01 = full power-down, 10 = standby, 11 = digital reset		0x00	
0x09	Clock	Open	0	Open	Open	Open	Open	Open	Duty cycle stabilizer: 0 = off, 1 = on	0x00	
0x0A	PLL_STATUS	PLL locked status bit: 0 = PLL is not locked, 1 = PLL is locked	Open	Open	Open	Open	Open	Open	JTX link status: 0 = not ready, 1 = ready		Read only.
0x0B	Clock divider	Open	Open	Open	Open	Open	Clock divider ratio[2:0]: 000 = divide by 1, 001 = divide by 2, 010 = divide by 3, 011 = divide by 4, 100 = divide by 5, 101 = divide by 6, 110 = divide by 7, 111 = divide by 8			0x00	
0x0C	Enhancement control	Open	Open	Open	Open	Open	Chop mode: 0 = off, 1 = on	Open	Open	0x00	
0x0D	Test mode (local except for pseudo-random number (PN) sequence resets)	User input test mode: 00 = single, 01 = alternate, 10 = single once, 11 = alternate once, (affects user input test mode only, Bits[3:0] = 1000)		Reset PN long generator	Reset PN short generator	Output test mode[3:0] (local): 0000 = off (default), 0001 = midscale short, 0010 = positive full scale (FS), 0011 = negative FS, 0100 = alternating checkerboard, 0101 = PN23 sequence, 0110 = PN9 sequence, 0111 = one/zero word toggle, 1000 = user input, 1001 = 1/0 bit toggle, 1010 = 1× sync, 1011 = one bit high, 1100 = mixed bit frequency				0x00	When set, the test data is placed on the output pins in place of normal data.
0x10	Offset adjust (local)	8-bit device offset adjustment [7:0] (local); offset adjusts in LSBs from +127 to −128 (twos complement format)								0x00	Device offset trim.

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Notes/ Comments
0x14	Output mode	JTX CS mode: 000 = {overrange||underrange, valid flag}, 001 = {overrange, underrange}, 010 = {overrange||underrange, blank}, 011 = {blank, valid flag}, 100 = {blank, blank}, Others = {overrange||underrange, valid flag}			ADC output valid flag: 0 = output valid, 1 = output invalid (local)	Open	Open	Output format: 0 = offset binary, 1 = twos complement		0x01	
0x15	Output adjust	Open	Open	Open	Open	Open	Typical CML differential output drive level: 000 = 473 mV p-p, 001 = 524 mV p-p, 010 = 574 mV p-p, 011 = 621 mV p-p (default), 100 = 667 mV p-p, 101 = 716 mV p-p, 110 = 763 mV p-p, 111 = 811 mV p-p			0x03	
0x16	Clock phase control	Open	Input clock phase adjust[2:0] (value is number of input clock cycles of phase delay)			Open	Open	Open	Open	0x00	
0x18	Input span select	Internal VREF adjustment[1:0]: 00 = 1.0 V, 01 = 1.2 V, 10 = 1.3 V, 11 = 1.4 V		Open	Open	Open	Differential span adjustment: 000 = 50% of normal, 001 = 57% of normal, 010 = 67% of normal, 011 = 80% of normal, 100 = normal			0x04	
0x19	User Test Pattern 1 LSB	User Test Pattern 1[7:0]								0x00	
0x1A	User Test Pattern 1 MSB	User Test Pattern 1[15:8]								0x00	
0x1B	User Test Pattern 2 LSB	User Test Pattern 2[7:0]								0x00	
0x1C	User Test Pattern 2 MSB	User Test Pattern 2[15:8]								0x00	
0x21	FLEX_SERIAL_ CONTROL	Open	Open	Open	Open	PLL low rate mode: 0 = lane rate ≥ 2 Gbps 1 = lane rate < 2 Gbps	Open	Open	Open	0x00	
0x22	FLEX_SERIAL_ CH_STAT	Open	Open	Open	Open	Open	Open	Open	Channel power-down (local)	0x00	
0x3A	SYSREF_CTRL	Open	Open	Open	0 = normal mode, 1 = realign the lanes on every active DSYNC±	0 = realign the lanes only when DSYSREF± causes a resync of the counters, 1 = realign the lanes on every DSYSREF±	Open	Open	Open	0x00	
0x3B	REALIGN_ PATTERN_CTRL	This pattern is written into the FIFO when a lane is being aligned: 00 = lane outputs constant zero, 55 = lane outputs toggling pattern								0x55	
0x5E	JESD204B quick configuration	0x41 = four converters, one lane; 0x42 = four converters, two lanes; 0x44 = four converters, four lanes; 0x22 = two converters, two lanes; 0x21 = two converters, one lane; 0x11 = one converter, one lane								0x00	Self clearing, always reads 0x00.

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Notes/ Comments
0x5F	JESD204B Link CTRL 1	Open	Tail bits mode: 0 = fill with 0s, 1 = fill with 9-bit PN sequence	JTX transport layer test: 0 = not enabled, 1 = long transport layer test enabled	Multiframe alignment character insertion: 0 = disabled, 1 = enabled	ILAS mode: 00 = ILAS disabled, 01 = ILAS enabled (normal mode), 11 = ILAS always on (test mode)		Frame alignment character insertion: 0 = enabled, 1 = disabled	0 = JTX link enabled, 1 = JTX link disabled	0x14	
0x60	JESD204B Link CTRL 2	Reserved		DSYNC± pin invert: 0 = not inverted, 1 = inverted	DSYNC± pin input bias: 0 = disabled, 1 = enabled	Open	Open	JTX output invert: 0 = normal, 1 = inverted	Reserved	0x10	
0x61	JESD204B Link CTRL 3	Reserved	Reserved	Test data injection point: 01 = 10-bit data injected at 8b/10b encoder output, 10 = 8-bit data at scrambler input		JTX test mode patterns: 0000 = normal operation (test mode disabled), 0001 = alternating checkerboard, 0010 = 1/0 word toggle, 0011 = PN sequence PN23, 0100 = PN sequence PN9, 0101= continuous/repeat user test mode, 0110 = single user test mode, 0111 = reserved, 1000 = modified RPAT test sequence (8-bit data only), 1100 = PN sequence PN7, 1101 = PN sequence PN15, other setting are unused				0x00	
0x62	JESD204B Link CTRL 4	Reserved								0x00	
0x64	JESD204B DID configuration	Device identification (DID) = C0								0xC0	Read only.
0x65	JESD204B BID configuration	Open	Open	Open	Open	JTX bank identification (BID) number				0x00	
0x66	JESD204B LID Configuration 0	Open	Open	Open	JTX lane identification (LID) number for Lane 0					0x00	
0x67	JESD204B LID Configuration 1	Open	Open	Open	JTX lane identification (LID) number for Lane 1					0x01	
0x68	JESD204B LID Configuration 2	Open	Open	Open	JTX lane identification (LID) number for Lane 2					0x02	
0x69	JESD204B LID Configuration 3	Open	Open	Open	JTX lane identification (LID) number for Lane 3					0x03	
0x6E	JESD204B parameters, SCR/L	JESD204B scrambling (SCR): 0 = disabled, 1 = enabled	Open	Open	JESD204B serial lane control: 0 = one lane per link (L = 1), 1 = two lanes per link (L = 2), 2 = unused, 3 = four lanes per link (L = 4), 4 to 31 = unused					0x80	
0x6F	JESD204B parameters, F	JESD204B number of octets per frame (F); calculated value, F = (2 × M)/L								0x00	Read only.
0x70	JESD204B parameters, K	Open	Open	Open	JESD204B number of frames per multiframe (K); K = register contents + 1, but also must be a multiple of four octets					0x1F	
0x71	JESD204B parameters, M	JESD204B number of converters (M): 0 = one converter (M = 1), 1 = two converters (M = 2), 3 = four converters (M = 4, default)								0x03	
0x72	JESD204B parameters, CS/N	00 = number of control bits sent per sample (CS = 0)		Open	JTX converter resolution (N): 0x0F = 16-bit, 0x0D = 14-bit, 0x0B = 12-bit, 0x09 = 10-bit					0x0F	
0x73	JESD204B parameters, subclass/Np	JESD204B subclass; 0x0 = Subclass 0; 0x1 = Subclass 1 (default)			JESD204B number of bits per sample (N'); N' = register contents + 1					0x2F	
0x74	JESD204B parameters, S	Reserved			JESD204B converter samples per frame (S); S = register contents + 1					0x20	Read only.
0x75	JESD204B parameters, HD and CF	JESD204B HD value = 0	Open	Open	JESD204B control words per frame clock cycle per link (CF = 0, fixed)					0x00	Read only.
0x76	JESD204B RESV1	JESD204B Serial Reserved Field No. 1 in link configuration, see Table 12 (RES1)								0x00	
0x77	JESD204B RESV2	JESD204B Serial Reserved Field No. 2 in link configuration, see Table 12 (RES2)								0x00	
0x78	JESD204B CHKSUM0	JESD204B serial checksum value in link configuration, see Table 12 for Lane 0 (FCHK)									Read only.

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Notes/ Comments
0x79	JESD204B CHKSUM1	JESD204B serial checksum value in link configuration, see Table 12 for Lane 1 (FCHK)									Read only.
0x7A	JESD204B CHKSUM2	JESD204B serial checksum value in link configuration, see Table 12 for Lane 2 (FCHK)									Read only.
0x7B	JESD204B CHKSUM3	JESD204B serial checksum value in link configuration, see Table 12 for Lane 3 (FCHK)									Read only.
0x80	JTX physical lane disable	Open	Open	Open	Open	Lane 3: 0 = enabled, 1 = disabled	Lane 2: 0 = enabled, 1 = disabled	Lane 1: 0 = enabled, 1 = disabled	Lane 0: 0 = enabled, 1 = disabled	0x00	Lane serialize and output driver powered down.
0x82	JESD204B Lane Assign 1	Open	Physical Lane 1 assignment: 000 = Logical Lane 0, 001 = Logical Lane 1, 010 = Logical Lane 2, 011 = Logical Lane 3			Open	Physical Lane 0 assignment: 000 = Logical Lane 0, 001 = Logical Lane 1, 010 = Logical Lane 2, 011 = Logical Lane 3			0x10	
0x83	JESD204B Lane Assign 2	Open	Physical Lane 3 assignment: 000 = Logical Lane 0, 001 = Logical Lane 1, 010 = Logical Lane 2, 011 = Logical Lane 3			Open	Physical Lane 2 assignment: 000 = Logical Lane 0, 001 = Logical Lane 1, 010 = Logical Lane 2, 011 = Logical Lane 3			0x32	
0x86	JESD204B lane inversion	Open	Open	Open	Open	Lane 3: 0 = no invert, 1 = invert	Lane 2: 0 = no invert, 1 = invert	Lane 1: 0 = no invert, 1 = invert	Lane 0: 0 = no invert, 1 = invert	0x00	
0x8B	JESD204B LMFC offset	Open	Open	Open	Local multiframe clock (LMFC) phase offset value; reset value for LMFC phase counter when DSYSREF± is asserted; used for deterministic delay applications					0x00	
0xA0	JTX User Pattern Octet 0, LSB	User test pattern least significant byte, Octet 0								0x00	
0xA1	JTX User Pattern Octet 0, MSB	User test pattern most significant byte, Octet 0								0x00	
0xA2	JTX User Pattern Octet 1, LSB	User test pattern least significant byte, Octet 1								0x00	
0xA3	JTX User Pattern Octet 1, MSB	User test pattern most significant byte, Octet 1								0x00	
0xA4	JTX User Pattern Octet 2, LSB	User test pattern least significant byte, Octet 2								0x00	
0xA5	JTX User Pattern Octet 2, MSB	User test pattern most significant byte, Octet 2								0x00	
0xA6	JTX User Pattern Octet 3, LSB	User test pattern least significant byte, Octet 3								0x00	
0xA7	JTX User Pattern Octet 3, MSB	User test pattern most significant byte, Octet 3								0x00	
0xF5	JTX converter mapping	JTX Converter 3: 0 = ADCA, 1 = ADCB, 2 = ADCC, 3 = ADCD		JTX Converter 2: 0 = ADCA, 1 = ADCB, 2 = ADCC, 3 = ADCD		JTX Converter 1: 0 = ADCA, 1 = ADCB, 2 = ADCC, 3 = ADCD		JTX Converter 0: 0 = ADCA, 1 = ADCB, 2 = ADCC, 3 = ADCD		0xE4	
0x100	Resolution/ sample rate override	Open	Override enable	Resolution: 0 = 16 bits, 1 = 14 bits, 2 = 12 bits, 3 = 10 bits		Open	Sample rate: 001 = 40 MSPS, 010 = 50 MSPS, 011 = 65 MSPS, 100 = 80 MSPS, 101 = 105 MSPS, 110 = 125 MSPS			0x00	Sample rate override (requires transfer register, 0xFF).
0x101	User I/O Control 2	Open	Open	Open	Open	Open	Open	Open	SDIO pull-down	0x00	Disables SDIO pull-down.
0x102	User I/O Control 3	Open	Open	Open	Open	VCM power-down	Open	Open	Open	0x00	VCM control.

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Notes/ Comments
0x109	Clock divider sync control	Clock divider sync mode: 0 = use SYNC pin, 1 = use DSYSREF± pins	Reserved					Reset clock divider sync received	Sync clock divider enable: 0 = disabled, 1 = enabled	0x00	
0x10A	Clock divider sync received	Open	Open	Open	Open	Open	Open	Open	Clock divider sync received	0x00	Read only.

MEMORY MAP REGISTER DESCRIPTIONS

For additional general information about functions controlled in Register 0x00 to Register 0xFF, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Device Index (Register 0x05)

Certain features in the map that are designated as local can be set independently for each channel, whereas other features apply globally to all channels (depending on context), regardless of the channel is selected. Bits[3:0] of Register 0x05 can be used to select which data channels are affected.

Transfer (Register 0xFF)

All registers except Register 0x100 are updated the moment they are written. Setting Bit 0 of the transfer register high initializes the settings in the resolution/sample rate override register (Address 0x100).

Power Modes (Register 0x08)

Bit 5—PDWN Pin Function

If set to 1, the PDWN pin initiates standby mode. If set to 0 (cleared), the PDWN pin initiates full power-down mode.

Bit 4—JTX Standby Mode

If set, the JTX block enters standby mode when chip standby is activated. Only the PLL is left running in standby mode. If cleared, the JTX block remains running when chip standby is activated.

Bits[1:0]—Power Mode

In normal operation (Bits[1:0] = 00), all ADC channels and the JTX block are active.

In full power-down mode (Bits[1:0] = 01), all ADC channels and the JTX block are powered down, and the digital datapath clocks are disabled, while the digital datapath is reset. The outputs are disabled.

In standby mode (Bits[1:0] = 10), all ADC channels are partially powered down, and the digital datapath clocks are disabled. If JTX standby mode is set, the outputs are also disabled.

During a digital reset (Bits[1:0] = 11), all the digital datapath clocks and the outputs (where applicable) on the chip are reset, except for the SPI port. Note that the SPI is always left under control of the user; that is, it is never automatically disabled or in reset (except by power-on reset). When the digital reset is deactivated, a foreground calibration sequence is initiated.

Enhancement Control (Register 0x0C)

Bit 2—Chop Mode

For applications that are sensitive to offset voltages and other low frequency noise, such as homodyne or direct conversion receivers, chopping in the first stage of the AD9656 is a feature that can be enabled by setting Bit 2. In the frequency domain, chopping translates offsets and other low frequency noise to $f_{CLK}/2$ where it can be filtered.

Output Mode (Register 0x14)

Bits[7:5]—JTX CS Mode

Defines the meaning of the JTX control bits.

Bits[1:0]—Output Format

By default, this field is set to 1 for data output in twos complement format. Setting this field to 0 changes the output mode to offset binary.

Clock Phase Control (Register 0x16)

Bits[6:4]—Input Clock Phase Adjust

When the clock divider (Register 0x0B) is used, the applied clock is at a higher frequency than the internal sampling clock. Bits[6:4] determine at which phase the external clock sampling occurs. This is only applicable when the clock divider is used. Setting Bits[6:4] greater than Register 0x0B, Bits[2:0] is prohibited.

Table 20. Input Clock Phase Adjust Options

Input Clock Phase Adjust, Bits[6:4]	Number of Input Clock Cycles of Phase Delay
000 (default)	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

JTX User Pattern (Register 0xA0 to Register 0xA7)

The pattern in these registers is output on all active lanes when Register 0x61, Bits[3:0] are set to 5 or 6. A 32-bit pattern, the concatenation of Register 0xA0, Register 0xA2, Register 0xA4, and Register 0xA6 is inserted before the scrambler if Register 0x61, Bits[5:4] are set to 2. If Register 0x61, Bits[5:4] are set to 1 (a 40-bit pattern), the concatenation of Register 0xA1, Bits[1:0] and Register 0xA0, Bits[7:0]; Register 0xA3, Bits[1:0] and Register 0xA2, Bits[7:0]; Register 0xA5, Bits[1:0] and Register 0xA4, Bits[7:0]; Register 0xA7, Bits[1:0] and Register 0xA6, Bits[7:0] is inserted after the 8b10b encoder.

Resolution/Sample Rate Override (Register 0x100)

This register allows the user to downgrade the resolution and/or the maximum sample rate (for lower power) in applications that do not require full resolution and/or sample rate. Settings in this register are not initialized until Bit 0 of the transfer register (Register 0xFF) is written high.

Bits[2:0] do not affect the sample rate; they affect the maximum sample rate capability of the ADC.

User I/O Control 2 (Register 0x101)

Bit 0—SDIO Pull-Down

Bit 0 can be set to disable the internal 30 kΩ pull-down resistor on the SDIO pin. This setting can be used to limit the loading when many devices are connected to the SPI bus.

User I/O Control 3 (Register 0x102)

Bit 3—VCM Power-Down

Bit 3 can be set high to power down the internal VCM generator. This feature is used when applying an external reference.

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting system level design and layout of the AD9656, it is recommended that the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements needed for certain pins.

POWER AND GROUND RECOMMENDATIONS

When connecting power to the AD9656, it is recommended that two separate 1.8 V supplies be used: one supply for analog (AVDD), and a separate supply for the digital outputs (DRVDD and DVDD). The designer can use several different decoupling capacitors to cover both high and low frequencies. Locate these capacitors close to the point of entry at the printed circuit board (PCB) level and close to the pins of the part with minimal trace length.

When using the AD9656, a single PCB ground plane is sufficient. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

CLOCK STABILITY CONSIDERATIONS

When powered on, the AD9656 enters an initialization phase during which an internal state machine sets up the biases and the registers for proper operation. During the initialization process, the AD9656 needs a stable clock. If the ADC clock source is not present or not stable during ADC power-up, it disrupts the state machine and causes the ADC to start up in an unknown state. To correct this, an initialization sequence Must be reinvoked after the ADC clock is stable. By issuing a digital reset via Register 0x08. In the default configuration (internal V_{REF}, ac-coupled input) where V_{REF} and V_{CM} are supplied by the ADC itself, a stable clock during power-up is sufficient. In the case where V_{REF} and/or V_{CM} are supplied by an external source, these, too, must be stable at power-up; otherwise, a subsequent digital reset via Register 0x08 is needed. The pseudo code sequence for a digital reset is as follows:

```
SPI_Write (0x08, 0x03);    # Digital Reset
SPI_Write (0x08, 0x00);    # Normal Operation
```

EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS

It is mandatory that the exposed pad on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance. A continuous, exposed (no solder mask) copper plane on the PCB must mate to the AD9656 exposed pad, Pin 0.

The copper plane must have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. Fill or plug these vias with nonconductive epoxy.

To maximize the coverage and adhesion between the ADC and the PCB, overlay a silkscreen to partition the continuous plane on the PCB into several uniform sections. This partitioning prevents the solder from pooling and provides several tie points between the ADC and the PCB during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and the PCB. See the evaluation board for a PCB layout example. For detailed information about the packaging and PCB layout of chip scale packages, refer to the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

VCM

Decouple the VCM pin to ground with a 0.1 µF capacitor.

REFERENCE DECOUPLING

Externally bypass the VREF pin to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

SPI PORT

When the full dynamic performance of the converter is required, do not activate the SPI port. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9656 to keep these signals from transitioning at the converter input pins during critical sampling periods.

OUTLINE DIMENSIONS

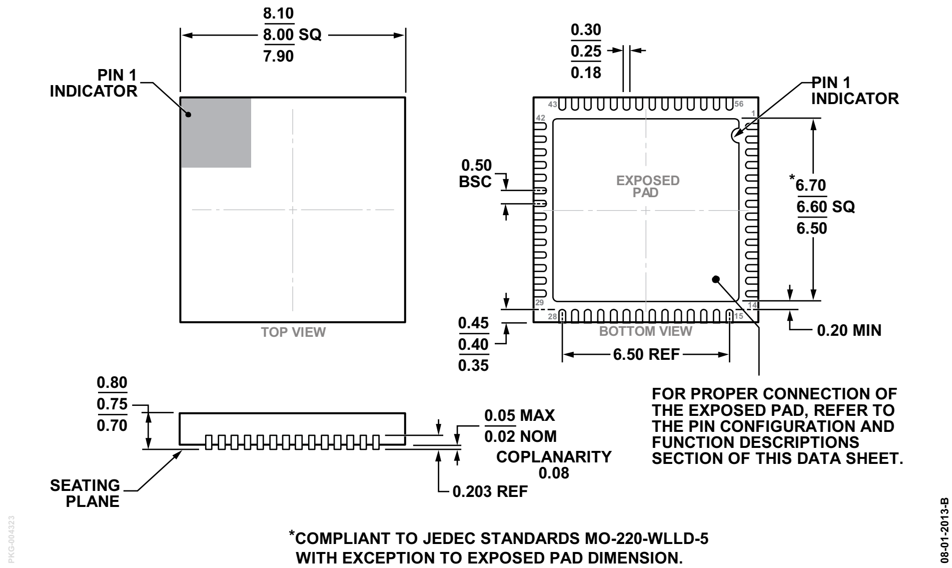

Figure 71. 56-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
8 mm × 8 mm Body, Very Very Thin Quad
(CP-56-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9656BCPZ-125	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-56-9
AD9656BCPZRL7-125	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-56-9
AD9656EBZ	−40°C to +85°C	Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES