N-Channel 20 V (D-S) MOSFET

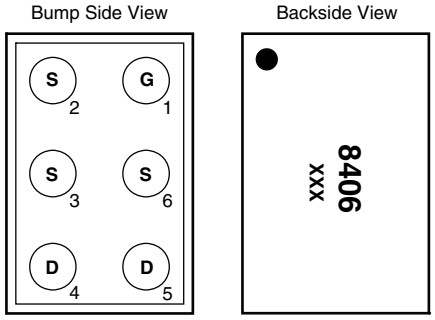
PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I_D (A)	Q_g (Typ.)
20	0.033 at V_{GS} = 4.5 V	16[e]	7.5 nC
	0.037 at V_{GS} = 2.5 V	16[e]	
	0.042 at V_{GS} = 1.8 V	15	

FEATURES

- TrenchFET® Power MOSFET
- Ultra-small 1.5 mm x 1 mm Maximum Outline
- Ultra-thin 0.59 mm Maximum Height
- Material categorization:
  For definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

MICRO FOOT

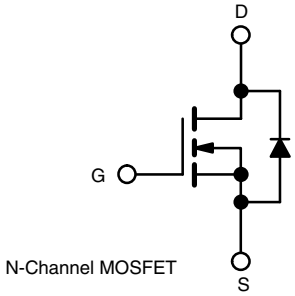


Device Marking: 8406
xxx = Date/Lot Traceability Code

Ordering Information:
Si8406DB-T2-E1 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- Load Switch
- Battery Management
- Boost Converter



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	16[e]	A
	T_C = 70 °C		13.5	
	T_A = 25 °C		7.8[a, b]	
	T_A = 70 °C		6.2[a, b]	
Pulsed Drain Current (t = 300 µs)		I_{DM}	30	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	11	
	T_A = 25 °C		2.3[a, b]	
Maximum Power Dissipation	T_C = 25 °C	P_D	13	W
	T_C = 70 °C		8.4	
	T_A = 25 °C		2.77[a, b]	
	T_A = 70 °C		1.77[a, b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Package Reflow Conditions[c]	IR/Convection		260	

Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. t = 10 s.
c. Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.
d. Case in defined as the top surface of the package.
e. T_C = 25 °C package limited.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a, b]		R_{thJA}	37	45	°C/W
Maximum Junction-to-Case (Drain)[c]	Steady State	R_{thJC}	7	9.5	

Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. Maximum under steady state conditions is 85 °C/W.
c. Case is defined as top surface of the package.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0, I_D = 250 µA	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		18		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.4		0.85	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 70 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 4.5 V	5			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 1 A		0.026	0.033	Ω
		V_{GS} = 2.5 V, I_D = 1 A		0.028	0.037	
		V_{GS} = 1.8 V, I_D = 1 A		0.030	0.042	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 1 A		20		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		830		pF
Output Capacitance	C_{oss}			146		
Reverse Transfer Capacitance	C_{rss}			61		
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 8 V, I_D = 1 A		13	20	nC
		V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 1 A		7.5	12	
Gate-Source Charge	Q_{gs}			1.1		
Gate-Drain Charge	Q_{gd}			0.8		
Gate Resistance	R_g	V_{GS} = 0.1 V, f = 1 MHz		3.6		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω $I_D \cong$ 1 A, V_{GEN} = 4.5 V, R_g = 1 Ω		7	15	ns
Rise Time	t_r			18	40	
Turn-Off Delay Time	$t_{d(off)}$			30	60	
Fall Time	t_f			10	20	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D = 1 A, V_{GEN} = 8 V, R_g = 1 Ω		5	10	ns
Rise Time	t_r			17	35	
Turn-Off Delay Time	$t_{d(off)}$			25	50	
Fall Time	t_f			10	20	

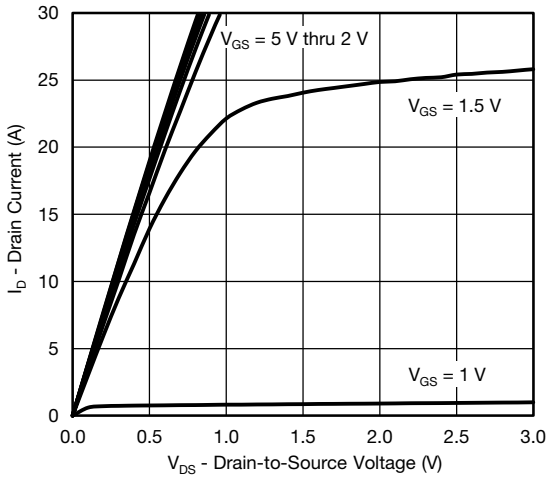
For technical questions, contact: pmostechsupport@vishay.com
Document Number: 62530
S12-0978-Rev. A, 30-Apr-12

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			20	A
Pulse Diode Forward Current	I_{SM}				30	
Body Diode Voltage	V_{SD}	I_S = 1 A, V_{GS} = 0		0.7	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 1 A, dI/dt = 100 A/µs, T_J = 25 °C		15	30	ns
Body Diode Reverse Recovery Charge	Q_{rr}			5	10	nC
Reverse Recovery Fall Time	t_a			8		ns
Reverse Recovery Rise Time	t_b			7		

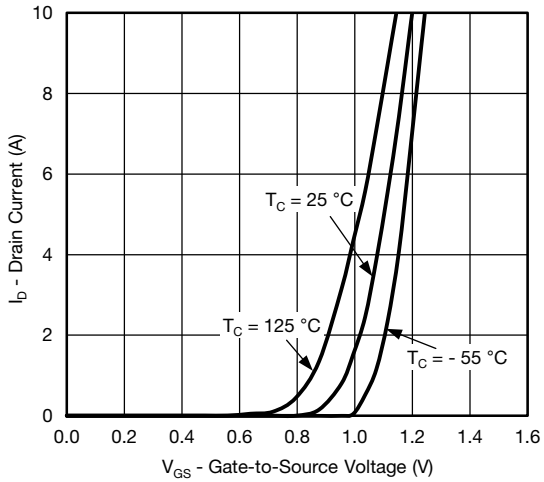
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

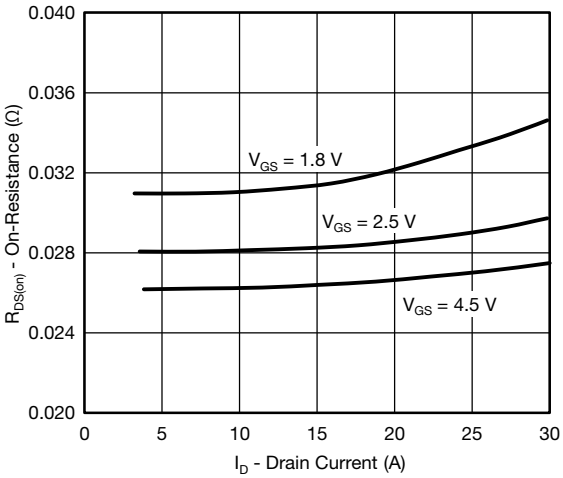
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



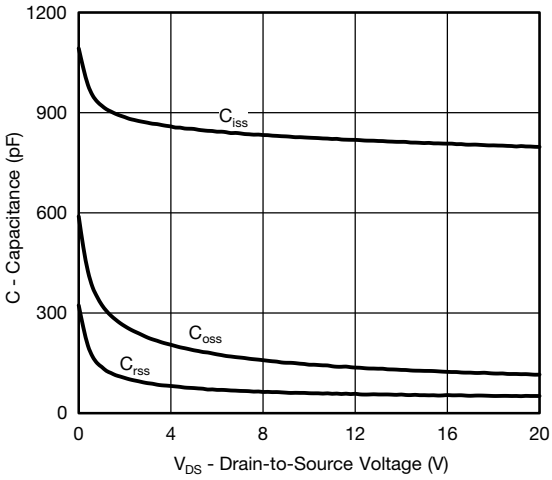
Output Characteristics



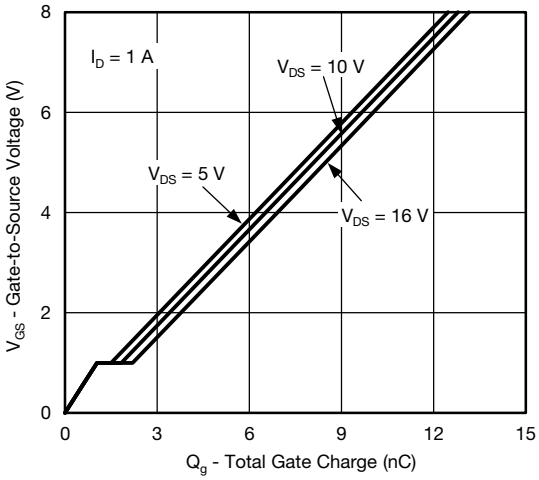
Transfer Characteristics



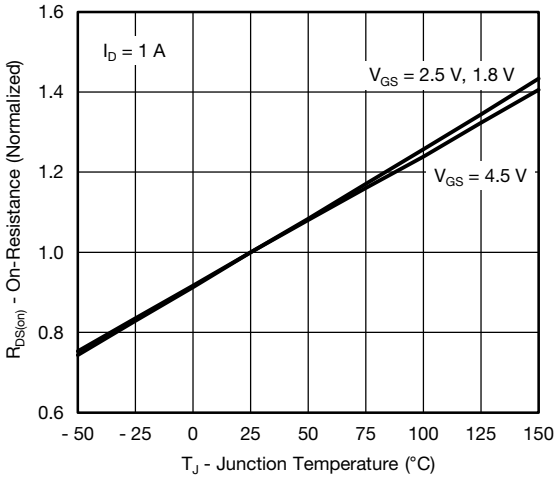
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

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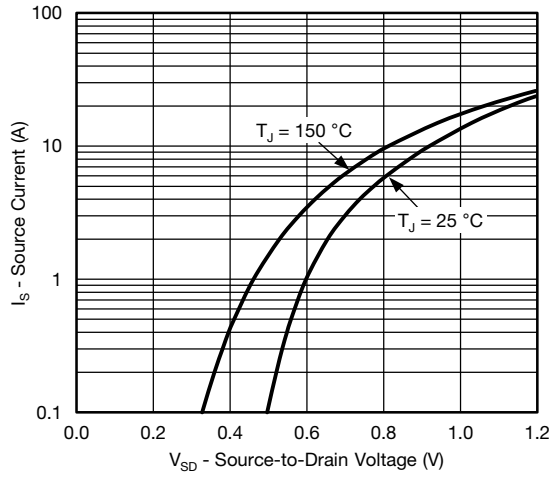
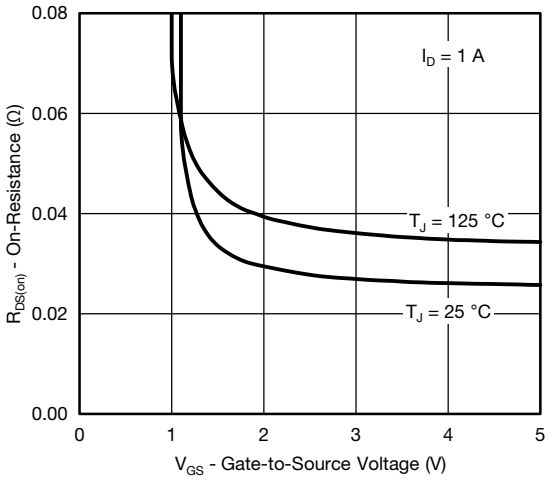
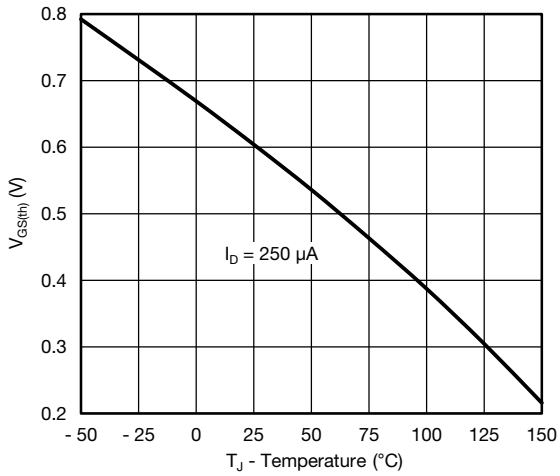
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



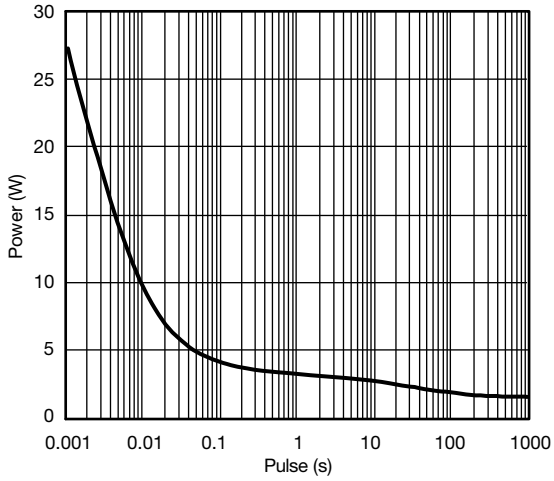
Source-Drain Diode Forward Voltage



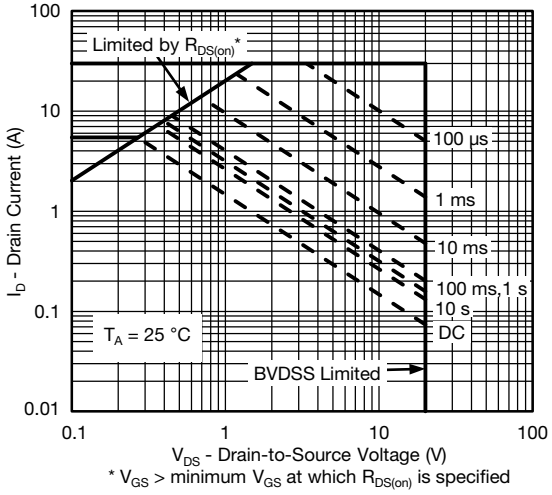
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



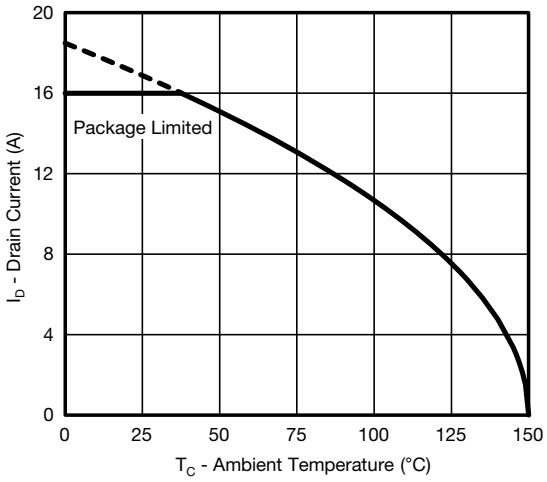
Single Pulse Power, Junction-to-Ambient



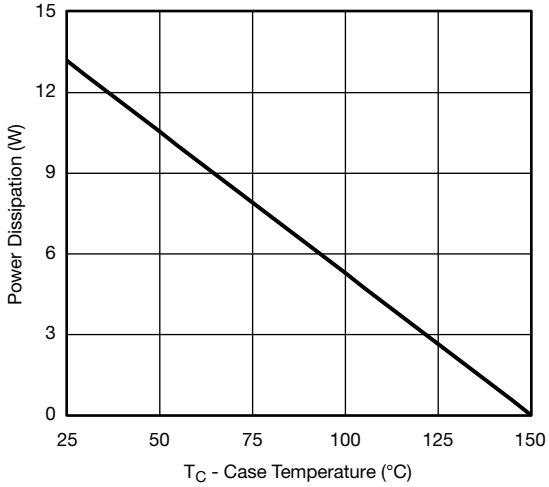
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



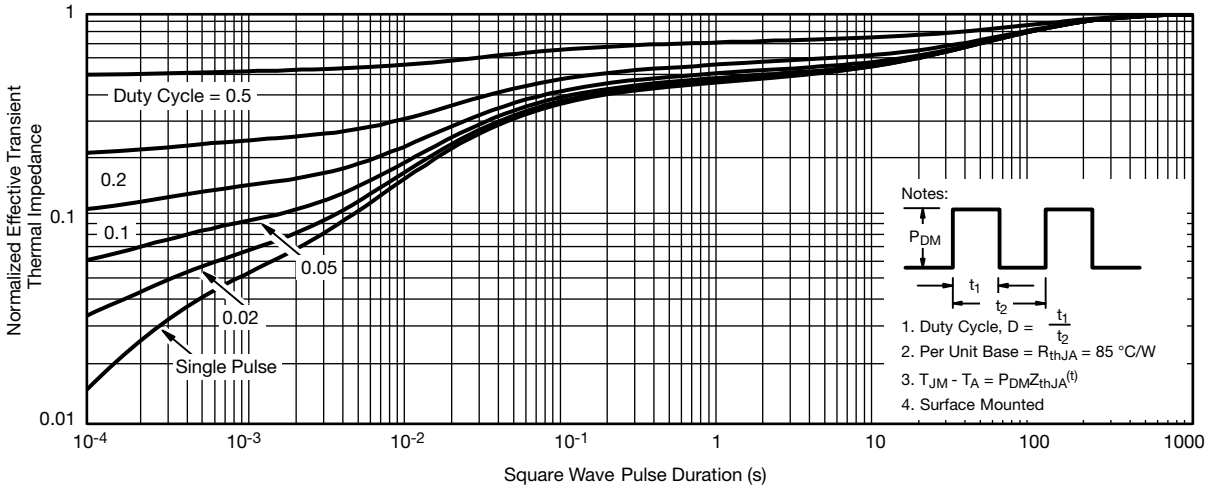
Current Derating*



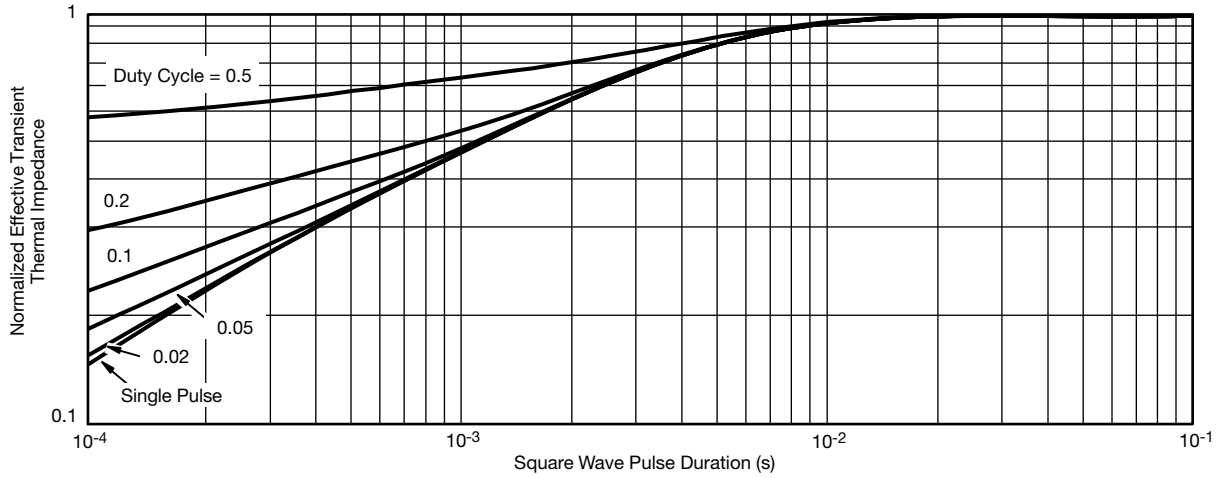
Power Derating

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



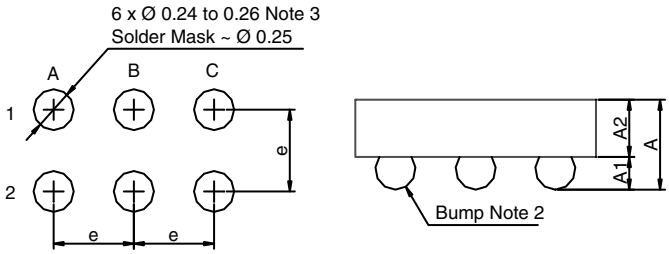
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

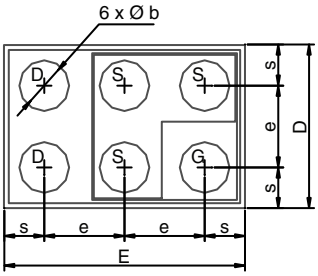
PACKAGE OUTLINE

MICRO FOOT: 6-BUMP (0.5 mm PITCH)



Recommended Land

Mark on Backside of Die



Notes (unless otherwise specified):
1. All dimensions are in millimeters.
2. Six (6) solder bumps are lead (Pb)-free 95.5Sn, 3.8Ag, 0.7Cu with diameter ∅ 0.30 mm to 0.32 mm.
3. Backside surface is coated with a Ti/Ni/Ag layer.
4. Non-solder mask defined copper landing pad.
5. • is location of pin 1.

Dim.	Millimeters[a]			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.510	0.575	0.590	0.0201	0.0224	0.0232
A_1	0.220	0.250	0.280	0.0087	0.0098	0.0110
A_2	0.290	0.300	0.310	0.0114	0.0118	0.0122
b	0.300	0.310	0.320	0.0118	0.0122	0.0126
e		0.500			0.0197	
s	0.230	0.250	0.270	0.0090	0.0098	0.0106
D	0.920	0.960	1.000	0.0362	0.0378	0.0394
E	1.420	1.460	1.500	0.0559	0.0575	0.0591

Note:
a. Use millimeters as the primary measurement.

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