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PicoEMI™ Programmable Spread Spectrum Clock

FEATURES

- Advanced programmable PLL with Spread Spectrum
- Accepts reference clock input: 10-200MHz
- Output frequency range: up to 166MHz @ 2.5V or up to 200MHz @ 3.3V operation.
- Programmable Spread Spectrum modulation magnitude:
  - Center Spread: ±0.125% to ±2.0% in ±0.125% steps
  - Down Spread: -0.25% to -4.0% in 0.25% steps
- Four pre-programmed configurations.
- Spread Spectrum On/Off selection.
- Programmable output drive (4mA, 8mA, 16mA)
- Low Cycle to Cycle jitter.
- Single 2.5V or 3.3V ± 10% power supply.
- Accepts ≥0.1V reference signal input voltage.
- Available in 6-pin SOT23 **GREEN**/RoHS compliant packages.

DESCRIPTION

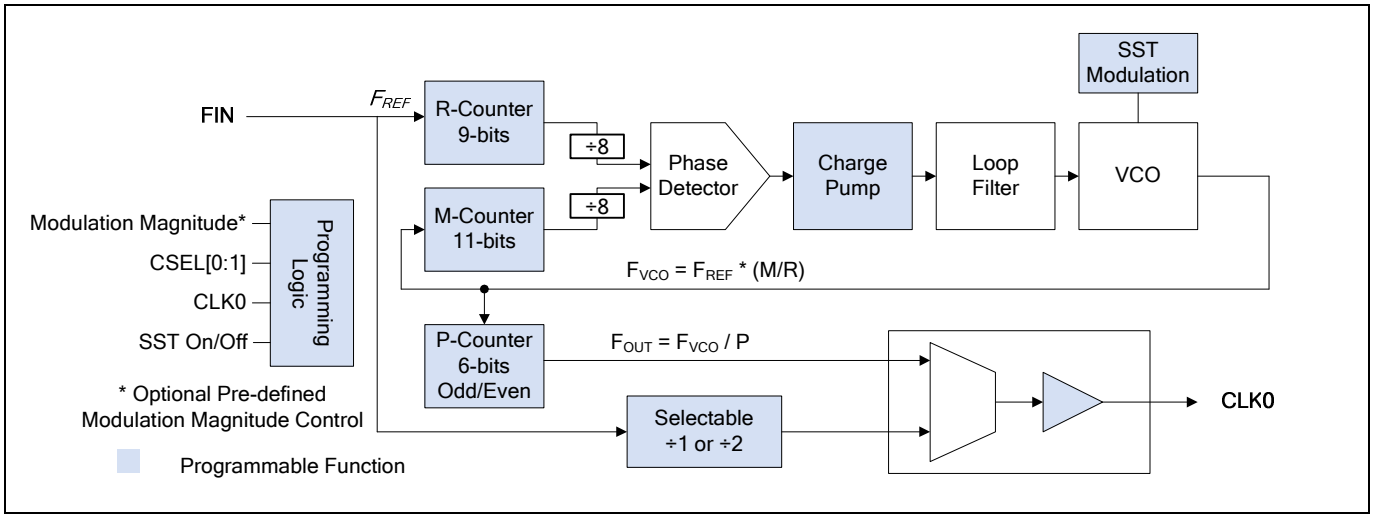
The PL671-05 and -06 are advanced programmable clock and Spread Spectrum clock generators (PSSCG), and members of PhaseLink's PicoPLL™ Programmable Clock family.

The PL671-05 and -06 offer up to 200MHz outputs, and allow for programming the modulation type (center or down Spread), as well as 16 modulation magnitudes (±0.125 to ±2.0% or -0.25 to -4.0%) to choose from. In addition, the CSEL[0:1] pins can be used to toggle the device thru 4 pre-programmed configurations. The Spread Spectrum modulation can be turned 'ON/OFF', allowing for completing a design with PL671-05/-06 and having the assurance of turning 'ON' the EMI modulation, if EMI becomes an issue. The frequency modulation of the PL671-05 and -06 greatly reduces the fundamental and harmonic frequencies' peak magnitude, therefore reducing the system level Electro Magnetic Interference (EMI), by as much as 20dB.

PIN CONFIGURATION

Note: ^ Denotes 60KΩ Pull-up resistor

BLOCK DIAGRAM



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PACKAGE PIN ASSIGNMENT

Name	PL671-05 SOT23-6L	PL671-06 SOT23-6L	Type	Description
CLK0	1	3	O	Programmable Clock Output with spread spectrum (SST can be turned off).
GND	2	2	P	GND connection.
FIN	3	1	I	Reference input pin.
VDD	4	4	P	VDD connection (2.25~3.63V)
CSEL0^, CSEL1^	5,6	5,6	I	Optional, pre-programmed configuration input control pins, to allow switching between '4' pre-defined configurations. Both pins incorporate a 60KΩ pull up resistor.

KEY PROGRAMMING PARAMETERS

Clock Output Frequency	SST Modulation Magnitude (Spread Percentage)	"On the Fly" Configuration	Output Drive Strength
FOUT = FREF * M / (R * P) where M =11 bit R = 9 bit P = 6 bit CLK0= FREF, FREF /2, FOUT * 'P' is a 6-bit Odd/Even divider	16 programmable modulation magnitudes to choose from: • Center Spread: ±0.125% to ±2.0% in ±0.125% steps • Down Spread: -0.25% to -4.0% in 0.25% steps	Up to 4 'On-The-Fly' switchabe pre-defined configurations.. • CSEL[0:1] Configuration Selection - input	Three optional drive strengths to choose from: • Low: 4mA • Std: 8mA (default) • High: 16mA

FUNCTIONAL DESCRIPTION

PL671-05/-06 are highly featured, very flexible, advanced programmable PLL designs for high performance, low-power Spread Spectrum modulation applications. The PL671-05/-06 accept a reference clock input of 10MHz to 200MHz and are capable of producing SST modulated outputs up to 200MHz. These flexible designs allow the PL671-05/-06 to deliver any PLL generated frequency, FREF (Ref Clk) frequency or FREF /2 to CLK0. The use of CSEL0 & CSEL1 allows the device to choose from up to 4 different modulation magnitude settings providing a range of spread settings to choose from. Some of the design features of the PL671-05 are mentioned below.

PLL Programming

The PLL in the PL671-05/-06 is fully programmable. The PLL is equipped with an 8-bit input frequency divider (R-Counter), and an 11-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 6-bit post VCO Odd/Even divider (P-Counter). The output frequency is determined by the following formula [FOUT = (FREF * M)/(R*P).

Modulation Magnitude and Type

The PL671-05/-06 provide the following programmable capabilities for Modulation Type and Modulation Magnitude (Spread Percentage):

Modulation Type	Modulation Magnitude	Programming Steps
Center Spread	±0.125% thru ±2.00%	±0.125%
Down Spread	-0.25% thru -4.00%	-0.25%

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Modulation Rate

The PL671-05/-06 modulation rate is defined as FREF (Ref Clk Frequency) divided by 8 times the R-counter, i.e. Modulation Rate = (F_{REF} / 8R). The rate can be changed by choosing alternate R-Counter settings.

Clock Output (CLK0)

The output of CLK0 can be configured as the PLL output (F_{VCO}/P), FREF (Ref Clk Frequency) output, or FREF/2 output. The output drive level can be programmed to Low Drive (4mA), Standard Drive (8mA) or High Drive (16mA). The output frequency can be programmed up to 200MHz at 3.3V (166MHz at 2.5V).

CSEL[0:1] Configuration Selectors

The PL671-05/-06 has the capability to be programmed with 4 distinct configurations and to toggle "On the Fly" between these configurations using the selector pads CSEL0 and CSEL1. An example would be a part that can run at ±0.25%, ±0.50%, ±1.0% or ±1.5% based on the CSEL0 and CSEL1 configuration. CSEL0 and CSEL1 both incorporate a 60kΩ pull up resistor giving a default condition of logic "1".

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

- Keep traces short!

- Trace = Inductor. With a capacitive load this equals ringing!

- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).

- Design long traces as "striplines" or "microstrips" with defined impedance.

- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply

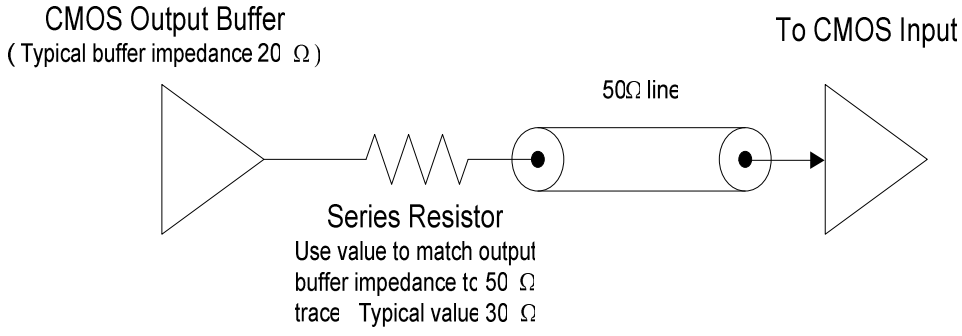
- Multiple VDD pins should be decoupled separately for best performance.

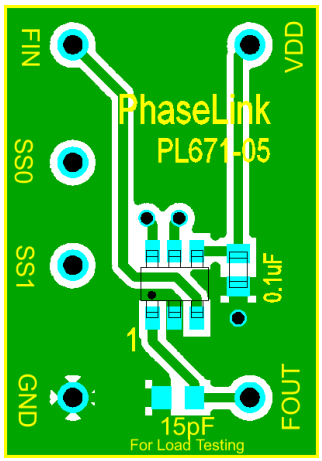
- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources

- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1µF for designs using crystals < 50MHz and 0.01µF for designs using crystals > 50MHz.

Typical CMOS termination

Place Series Resistor as close as possible to CMOS output





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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	4.6	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Soldering Temperature (Green package)			260	°C
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input (FIN) Frequency	@ V_{DD} =3.3V	10		200	MHz
	@ V_{DD} =2.5V			166	
Input (FIN) Signal Amplitude	Internally AC coupled (High Frequency)	0.9		V_{DD}	Vpp
Input (FIN) Signal Amplitude	Internally AC coupled (Low Frequency) 3.3V ≤50MHz, 2.5V ≤40MHz	0.1		V_{DD}	Vpp
Output Frequency	@ V_{DD} =3.3V			200	MHz
	@ V_{DD} =2.5V			166	MHz
Settling Time	At power-up (after V_{DD} increases over 2.25V)			2	ms
Output Enable Time	PDB Function; Ta=25° C, 15pF Load			2	ms
Output Rise Time	15pF Load, 10/90% V_{DD}, Standard Drive		2.5	3.5	ns
	15pF Load, 10/90% V_{DD}, High Drive		1.2	1.7	ns
Output Fall Time	15pF Load, 90/10% V_{DD}, Standard Drive		1.7	2.0	ns
	15pF Load, 90/10% V_{DD}, High Drive		1.2	1.7	ns
Duty Cycle	At V_{DD} / 2	45	50	55	%
Cycle to Cycle Jitter	$T_{cyc-cyc}$ (Over output frequency range @ 3.3V)			100	ps

* Note: Jitter performance depends on the programming parameters.

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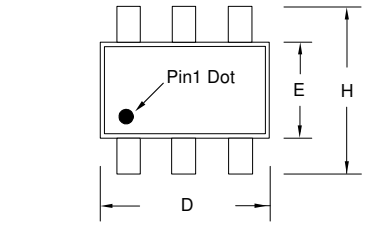
DC SPECIFICATIONS

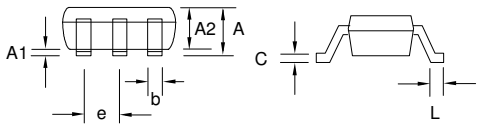
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	At 25MHz, 3.3V, load=15pF, (PDB=1)			15	mA
		PDB=0			10	µA
Operating Voltage	V_{DD}		2.25		3.63	V
Output Low Voltage	V_{OL}	I_{OL} = +4mA (Std. Drive)			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA (Std. Drive)	V_{DD} – 0.4			V
Output Current, Low Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	4			mA
Output Current, Standard Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	8			mA
Output Current, High Drive	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V	16			mA

PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

SOT23-6 L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.00
L	0.35	0.55
e	0.95 BSC	





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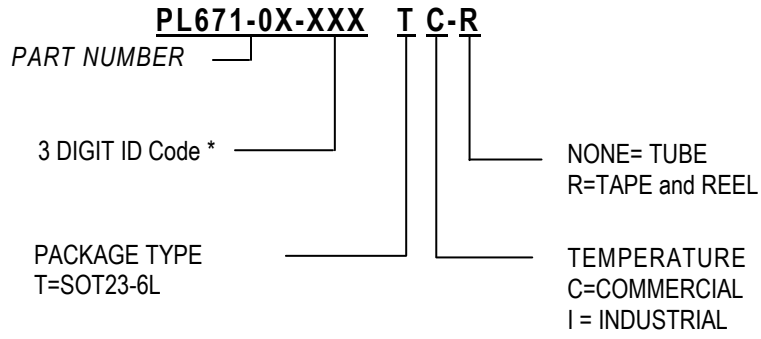
ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range



* PhaseLink will assign a unique 3-digit ID code for each approved programmed part number.

Part Number /Order Number	Marking†	Package Option
PL671-05-XXXTC-R	F4XXX	6-Pin SOT23 (Tape and Reel)
PL671-06-XXXTC-R	F5XXX	6-Pin SOT23 (Tape and Reel)

† Note: 'XXX' designates marking identifier that, at times, could be independent of the part number. Please consult your PhaseLink Sales Representative for marking information.

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Solder reflow profile available at www.phaselink.com/QA/solderingGreen.pdf

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