DDR3 SDRAM Specification

204pin Unbuffered SODIMM based on 1Gb D-die

64-bit Non-ECC

(RoHS compliant)

Table Contents

Revision History

Revision	Month	Year	History
0.5	November	2007	- First release

1.0 DDR3 Unbuffered SoDIMM Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank	Height
M471B6474DZ1-CF7/F8/G8/H9	512MB	64Mx64	64Mx16(K4B1G1646D-HC##)*4	1	30mm
M471B2874DZ1-CF7/F8/G8/H9	1GB	128Mx64	64Mx16(K4B1G1646D-HC##)*8	2	30mm
M471B5673DZ1-CF7/F8/G8/H9	2GB	256Mx64	128Mx8(K4B1G0846D-HC##)*16	2	30mm

* ## : F7 / F8 / G8 / H9

2.0 Key Features

Speed	DDR3-800	DDR3-1066		DDR3-1333	Unit
	6-6-6	7-7-7	8-8-8	9-9-9	
tCK(min)	2.5	1.875		1.5	ns
CAS Latency	6	7	8	9	tCK
tRCD(min)	15	13.125	15	13.5	ns
tRP(min)	15	13.125	15	13.5	ns
tRAS(min)	37.5	37.5	37.5	36	ns
tRC(min)	52.5	50.625	52.5	49.5	ns

- JEDEC standard 1.5V ± 0.075V Power Supply
- VDDQ = 1.5V ± 0.075V
- 400 MHz f_{CK} for 800Mb/sec/pin, 533MHz f_{CK} for 1066Mb/sec/pin, 667MHz f_{CK} for 1333Mb/sec/pin
- 8 independent internal bank
- Programmable $\overline{CAS}$ Latency: 6,7,8,9
- Programmable Additive Latency(Posted $\overline{CAS}$) : 0, CL - 2, or CL - 1 clock
- Programmable $\overline{CAS}$ Write Latency(CWL) = 5(DDR3-800), 6(DDR3-1066), 7(DDR3-1333)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < $T_{CASE} \leq$ 95°C
- Asynchronous Reset

3.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
64x16(1Gb) based Module	A0-A12	A0-A9	BA0-BA2	A10/AP
128x8(1Gb) based Module	A0-A13	A0-A9	BA0-BA2	A10/AP

4.0 x64 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REFDQ}	2	V_{SS}	71	V_{SS}	72	V_{SS}	139	V_{SS}	140	DQ38
3	V_{SS}	4	DQ4	KEY				141	DQ34	142	DQ39
5	DQ0	6	DQ5	73	CKE0	74	CKE1	143	DQ35	144	V_{SS}
7	DQ1	8	V_{SS}	75	V_{DD}	76	V_{DD}	145	V_{SS}	146	DQ44
9	V_{SS}	10	DQS0	77	NC	78	A15[3]	147	DQ40	148	DQ45
11	DM0	12	$\overline{DQS}$0	79	BA2	80	A14[3]	149	DQ41	150	V_{SS}
13	V_{SS}	14	V_{SS}	81	V_{DD}	82	V_{DD}	151	V_{SS}	152	$\overline{DQS}$5
15	DQ2	16	DQ6	83	A12/$\overline{BC}$	84	A11	153	DM5	154	DQS5
17	DQ3	18	DQ7	85	A9	86	A7	155	V_{SS}	156	V_{SS}
19	V_{SS}	20	V_{SS}	87	V_{DD}	88	V_{DD}	157	DQ42	158	DQ46
21	DQ8	22	DQ12	89	A8	90	A6	159	DQ43	160	DQ47
23	DQ9	24	DQ13	91	A5	92	A4	161	V_{SS}	162	V_{SS}
25	V_{SS}	26	V_{SS}	93	V_{DD}	94	V_{DD}	163	DQ48	164	DQ52
27	$\overline{DQS}$1	28	DM1	95	A3	96	A2	165	DQ49	166	DQ53
29	DQS1	30	$\overline{RESET}$	97	A1	98	A0	167	V_{SS}	168	V_{SS}
31	V_{SS}	32	V_{SS}	99	V_{DD}	100	V_{DD}	169	$\overline{DQS}$6	170	DM6
33	DQ10	34	DQ14	101	CK0	102	CK1	171	DQS6	172	V_{SS}
35	DQ11	36	DQ15	103	$\overline{CK}$0	104	$\overline{CK}$1	173	V_{SS}	174	DQ54
37	V_{SS}	38	V_{SS}	105	V_{DD}	106	V_{DD}	175	DQ50	176	DQ55
39	DQ16	40	DQ20	107	A10/AP	108	BA1	177	DQ51	178	V_{SS}
41	DQ17	42	DQ21	109	BA0	110	$\overline{RAS}$	179	V_{SS}	180	DQ60
43	V_{SS}	44	V_{SS}	111	V_{DD}	112	V_{DD}	181	DQ56	182	DQ61
45	$\overline{DQS}$2	46	DM2	113	$\overline{WE}$	114	$\overline{S}$0	183	DQ57	184	V_{SS}
47	DQS2	48	V_{SS}	115	$\overline{CAS}$	116	ODT0	185	V_{SS}	186	$\overline{DQS}$7
49	V_{SS}	50	DQ22	117	V_{DD}	118	V_{DD}	187	DM7	188	DQS7
50	DQ18	52	DQ23	119	A13[3]	120	ODT1	189	V_{SS}	190	V_{SS}
53	DQ19	54	V_{SS}	121	$\overline{S}$1	122	NC	191	DQ58	192	DQ62
55	V_{SS}	56	DQ28	123	V_{DD}	124	V_{DD}	193	DQ59	194	DQ63
57	DQ24	58	DQ29	125	TEST	126	V_{REF}CA	195	V_{SS}	196	V_{SS}
59	DQ25	60	V_{SS}	127	V_{SS}	128	V_{SS}	197	SA0	198	$\overline{EVENT}$
61	V_{SS}	62	$\overline{DQS}$3	129	DQ32	130	DQ36	199	V_{DDSPD}	200	SDA
63	DM3	64	DQS3	131	DQ33	132	DQ37	201	SA1	202	SCL
65	V_{SS}	66	V_{SS}	133	V_{SS}	134	V_{SS}	203	V_{tt}	204	V_{tt}
67	DQ26	68	DQ30	135	$\overline{DQS}$4	136	DM4				
69	DQ27	70	DQ31	137	DQS4	138	V_{SS}				

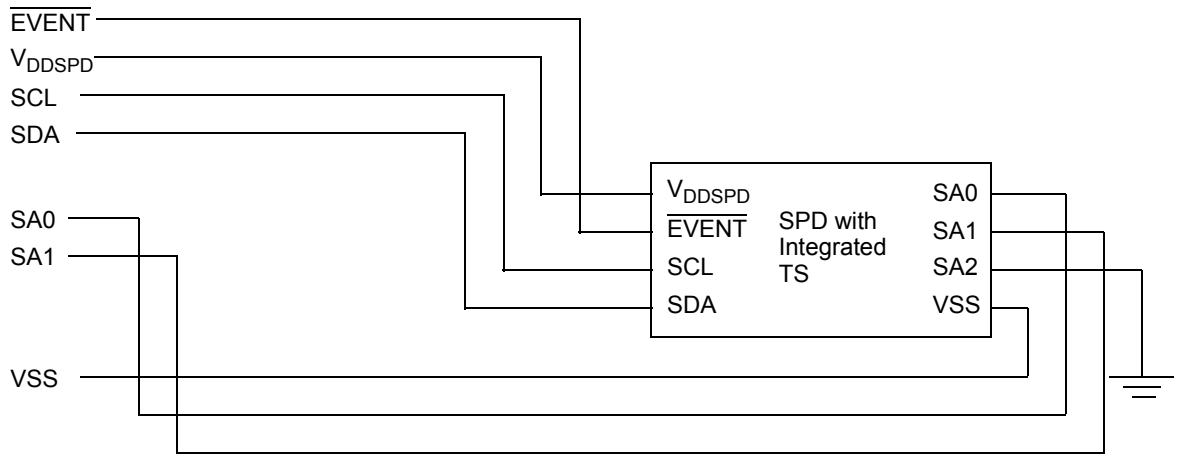
Note :
1. NC = No Connect, NU = Not Useable, RFU = Reserved Future Use
2. TEST(pin 125) is reserved for bus analysis probes and is NC on normal memory modules.
3. This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

5.0 Pin Description

Pin Name	Description	Number	Pin Name	Description	Number
CK0, CK1	Clock Inputs, positive line	2	DQ0-DQ63	Data Input/Output	64
$\overline{CK0}$, $\overline{CK1}$	Clock Inputs, negative line	2	DM0-DM7	Data Masks/ Data strobes, Termination data strobes	8
CKE0, CKE1	Clock Enables	2	DQS0-DQS7	Data strobes	8
$\overline{RAS}$	Row Address Strobe	1	$\overline{DQS0}$-$\overline{DQS7}$	Data strobes complement	8
$\overline{CAS}$	Column Address Strobe	1	$\overline{RESET}$	Reset Pin	1
$\overline{WE}$	Write Enable	1	TEST	Logic Analyzer specific test pin (No connect on SODIMM)	1
$\overline{S0}$, $\overline{S1}$	Chip Selects	2	$\overline{EVENT}$	Temperature event pin	1
A0-A9, A11, A13-A15	Address Inputs	14	V_{DD}	Core and I/O Power	18
A10/AP	Address Input/Autoprecharge	1	V_{SS}	Ground	52
A12/$\overline{BC}$	Address Input/Burst chop	1	V_{REFDQ} V_{REFCA}	Input/Output Reference	2
BA0-BA2	SDRAM Bank Addresses	3	V_{DDSPD}	SPD and Temp sensor Power	1
ODT0, ODT1	On-die termination control	2	V_{TT}	Termination Voltage	2
SCL	Serial Presence Detect (SPD) Clock Input	1	NC	Reserved for future use	2
SDA	SPD Data Input/Output	1		Total	204
SA0-SA1	SPD Address	2			

*The VDD and VDDQ pins are tied common to a single power-plane on these desigus.

6.0 ON DIMM Thermal Sensor



Temperature Sensor Characteristics

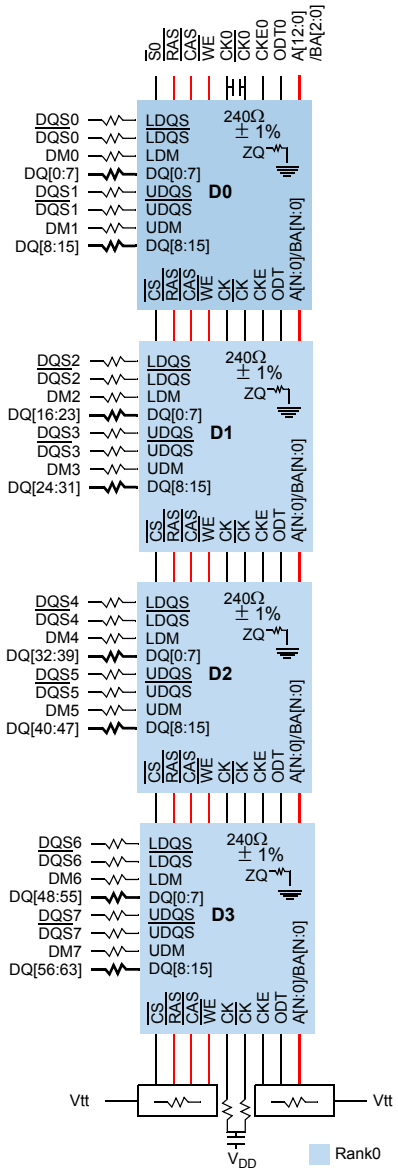
Grade	Range	Temperature Sensor Accuracy			Units	Notes
		Min.	Typ.	Max.		
C	75 < Ta < 95		+/- 1.0	+/- 2.0	°C	
	40 < Ta < 125		+/- 2.0	+/- 3.0		
	-20 < Ta < 125		+/- 3.0	+/- 4.0		
Resolution		0.25			°C /LSB	

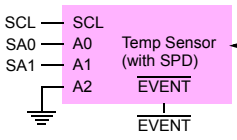
7.0 Input/Output Functional Description

Symbol	Type	Function
CK0-CK1 $\overline{CK0}$-$\overline{CK1}$	Input	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of CK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0-CKE1	Input	Activates the DDR3 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S}$0-$\overline{S}$1	Input	Enables the associated DDR3 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S}$0; Rank 1 is selected by $\overline{S}$1.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	When sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$, signals $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0-BA2	Input	Selects which DDR3 SDRAM internal bank of eight is activated.
ODT0-ODT1	Input	Asserts on-die termination for DQ, DM, DQS, and DQS signals if enabled via the DDR3 SDRAM mode register.
A0-A9, A10/AP, A11 A12/$\overline{BC}$ A13-A15	Input	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge. A12($\overline{BC}$) is sampled during READ and WRITE commands to determine if burst chop (on-thefly) will be performed (HIGH, no burst chop; LOW, burst chopped)
DQ0-DQ63	I/O	Data Input/Output pins.
DM0-DM7	Input	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS0-DQS7 $\overline{DQS0}$-$\overline{DQS7}$	I/O	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR3 SDRAMs and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$.
V_{DD},V_{DDSPD}, V_{SS}	Supply	Power supplies for core, I/O, Serial Presence Detect, Temp sensor, and ground for the module.
V_{REFDQ}, V_{REFCA}	Supply	Reference voltage for SSTL15 inputs.
SDA	I/O	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM and Temp sensor. A resistor must be connected from the SDA bus line to VDDSPD on the system planar to act as a pull up.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM and Temp sensor.
SA0-SA1	Input	Address pins used to select the Serial Presence Detect and Temp sensor base address.
TEST	I/O	The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules
$\overline{EVENT}$	Wire-OR Out	The $\overline{EVENT}$ pin is reserved for use to flag critical module temperature. A resistor may be connected from $\overline{EVENT}$ bus line to V_{DDSPD} on the system planar to act as a pullup.
$\overline{RESET}$	Input	$\overline{RESET}$ In Active Low This signal resets the DDR3 SDRAM

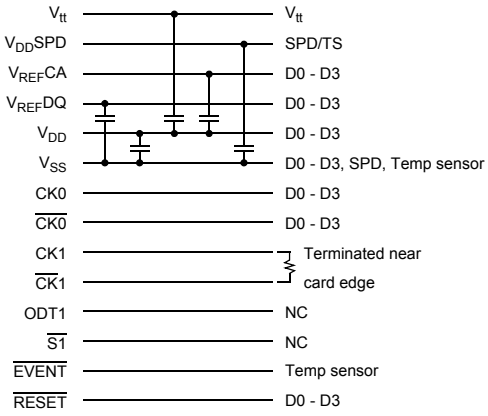
8.0 Functional Block Diagram:

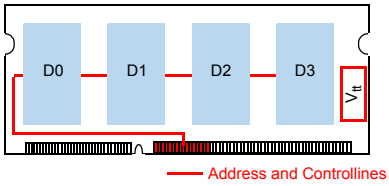
8.1 512MB, 64Mx64 Module(Populated as 1 rank of x16 DDR3 SDRAMs)





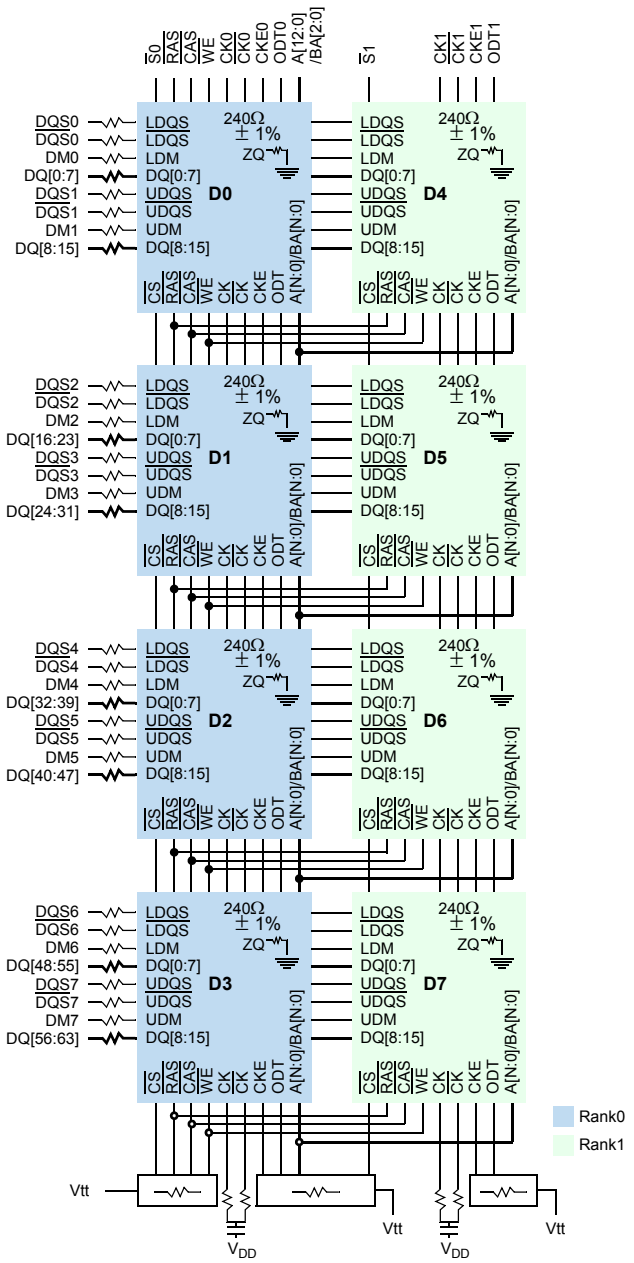
The SPD may be integrated with the Temp Sensor or may be a separate component.

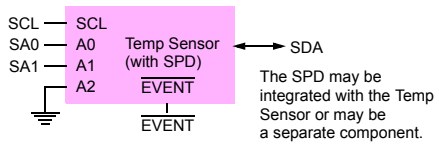


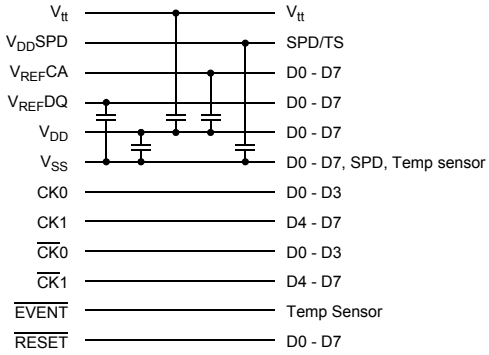


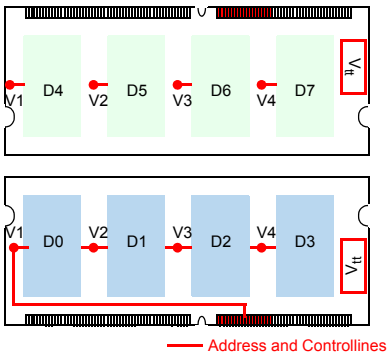
Note :
1. DQ wiring may differ from that shown however ,DQ, DM, DQS and $\overline{DQS}$ relationships are maintained as shown

8.2 1GB, 128Mx64 Module(Populated as 2 rank of x16 DDR3 SDRAMs)



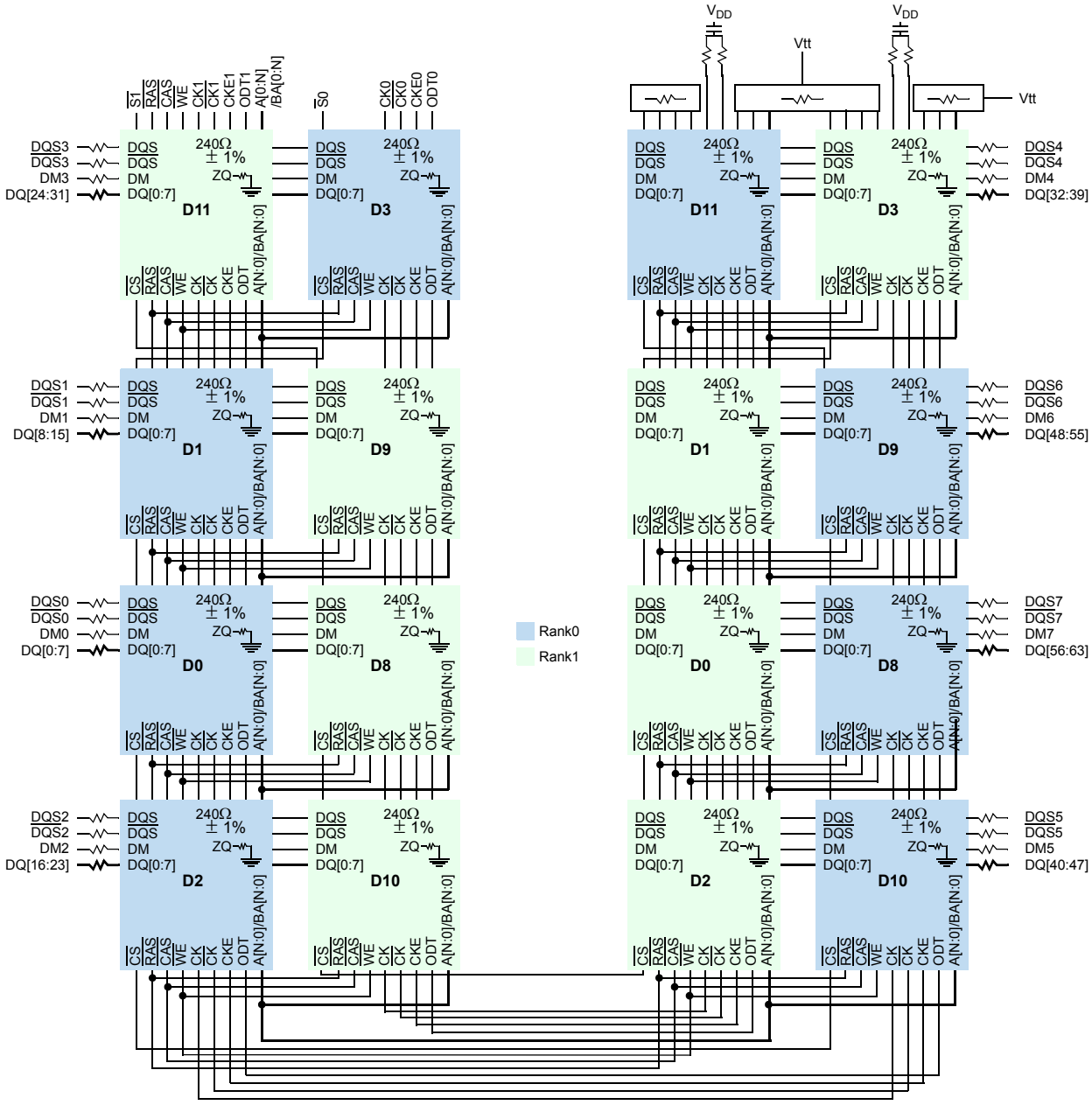


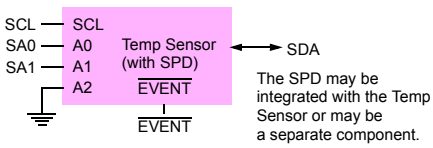




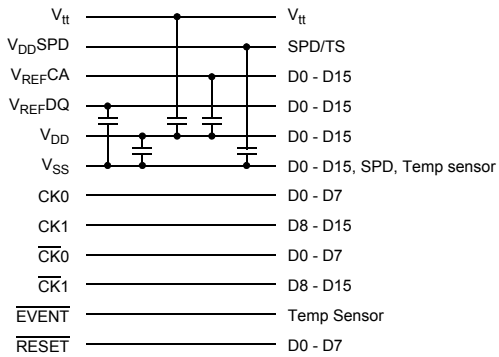
Note :
1. DQ wiring may differ from that shown however ,DQ, DM, DQS and DQS relationships are maintained as shown

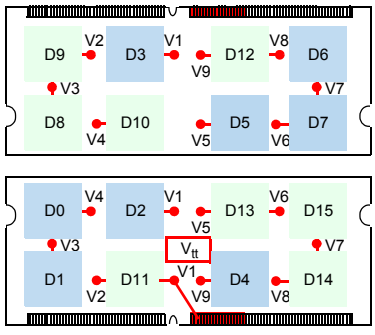
8.3 2GB, 256Mx64 Module(Populated as 2 rank of x8 DDR3 SDRAMs)





The SPD may be integrated with the Temp Sensor or may be a separate component.





Note :
1. DQ wiring may differ from that shown however ,DQ, DM, DQS and $\overline{DQS}$ relationships are maintained as shown

9.0 Absolute Maximum Ratings

9.1 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Note :

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times;and VREF must be not greater than 0.6XVDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

9.2 DRAM Component Operating Temperature Range

Symbol	Parameter	rating	Unit	Notes
TOPER	Normal Operating Temperature Range	0 to 85	°C	1,2
	Extended Temperature Range (Optional)	85 to 95	°C	1,3

Note :

1. Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions
3. Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9us. It is also possible to specify a component with 1X refresh (tREFI to 7.8us) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

10.0 AC & DC Operating Conditions

10.1 Recommended DC Operating Conditions (SSTL - 15)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.5	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.5	1.575	V	1,2

Note :

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

11.0 AC & DC Input Measurement Levels

11.1 AC and DC Logic input levels for single-ended signals

Symbol	Parameter	DDR3-800/1066/1333		Unit	Notes
		Min.	Max.		
V_{IH}(DC)	dc input logic high	VREF + 100	VDD	mV	1
V_{IL}(DC)	dc input logic low	VSS	VREF - 100	mV	1
V_{IH}(AC)	ac input logic high	VREF + 175	-	mV	1,2
V_{IL}(AC)	ac input logic low	-	VREF - 175	mV	1,2
V_{REFDQ}(DC)	I/O Reference Voltage(DQ)	0.49*VDDQ	0.51*VDDQ	V	3,4
V_{REFCA}(DC)	I/O Reference Voltage(CMD/ADD)	0.49*VDDQ	0.51*VDDQ	V	3,4

Single Ended AC and DC input levels

Note :
1. For DQ and DM, $V_{REF} = V_{REFDQ}$. For input only pins except RESET, or $V_{REF} = V_{REFCA}$
2. See "Overshoot and Undershoot specifications" on component datasheet
3. The ac peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REF(DC)}$ by more than ± 1% VDD (for reference : approx. ± 15mV)
4. For reference : approx. VDD/2 ± 15mV
5. Single ended swing requirement for DQS - $\overline{DQS}$ is 350 mV(peak to peak). Differential swing requirement for DQS - $\overline{DQS}$ is 700 mV(peak to peak).

The dc-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are illustrate in Figure 1. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA and VREFDQ likewise).

VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requiremts in above table. Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than ± 1% VDD.

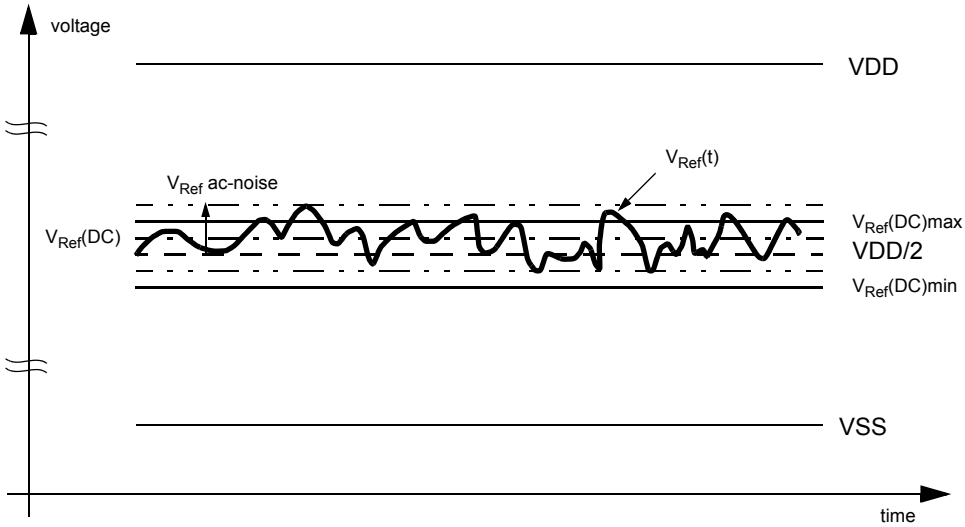


Illustration of VREF(DC) tolerance and VREF ac-noise limits

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VRef.

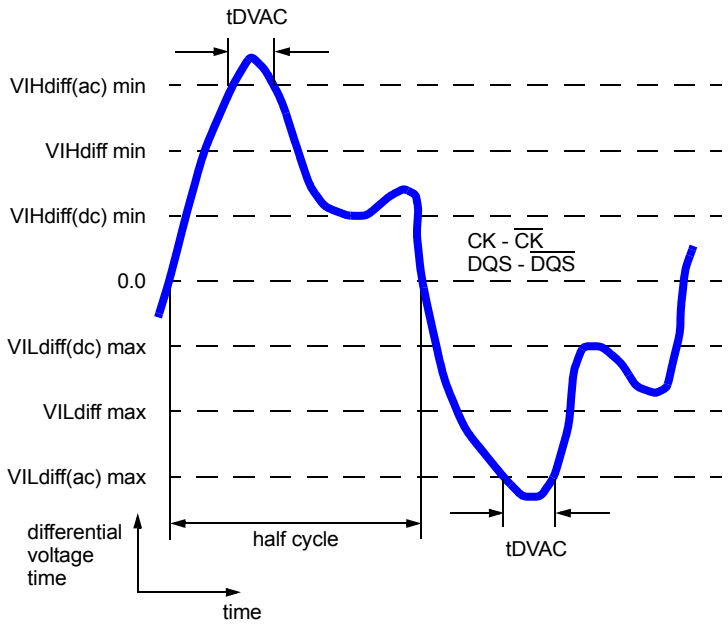
"VRef" shall be understood as VRef(DC), as defined in above Figure.

This clarifies, that dc-variations of VRef affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VRef(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VRef ac-noise. Timing and voltage effects due to ac-noise on VRef up to the specified limit (+/-1% of VDD) are included in DRAM timings and their associated deratings.

11.2 Differential swing requirement for differntial signals

Definition of differntial ac-swing and "time above ac level tDVAC



Differential swing requirement for clock (CK - $\overline{CK}$) and strobe (DQS - $\overline{DQS}$)

Symbol	Parameter	DDR3-800 / 1066 / 1333		unit	Note
		min	max		
VIHdiff	differential input high	+0.2	note 3	V	1
VILdiff	differential input low	note 3	-0.2	V	1
VIHdiff(ac)	differential input high ac	2 x (VIH(ac)-Vref)	note 3	V	2
VILdiff(ac)	differential input low ac	note 3	2 x (Vref - VIL(ac))	V	2

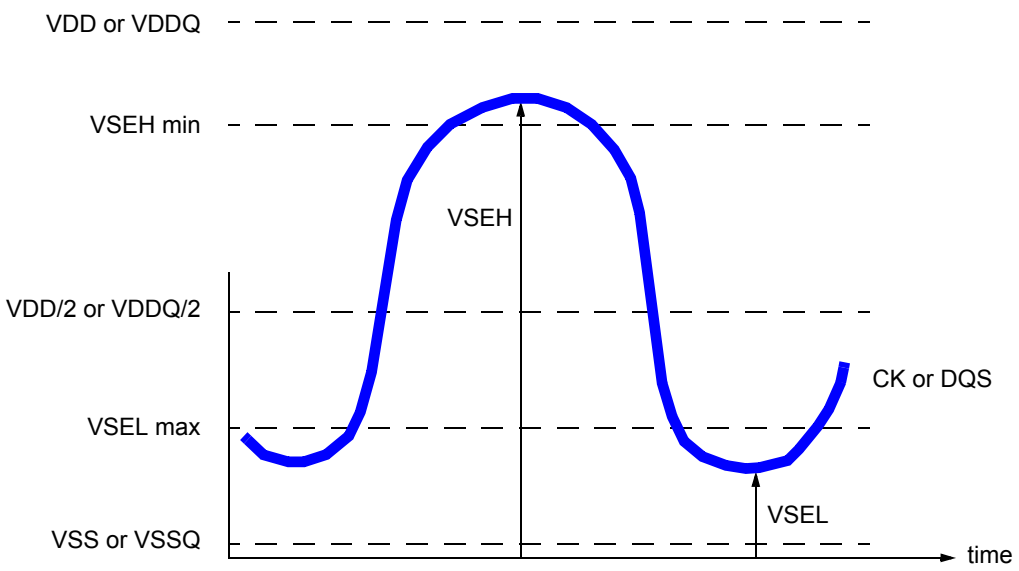
Notes:
1. used to define a differential signal slew-rate.
2. for CK - $\overline{CK}$ use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - $\overline{DQS}$, DQSL - $\overline{DQSL}$, DQSU - $\overline{DQSU}$ use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. these values are not defined, however they single-ended signals CK, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Allowed time before ringback (tDVAC) for CLK - $\overline{CLK}$ and DQS - $\overline{DQS}$.

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(ac)| = 350mV		tDVAC [ps] @ |VIH/Ldiff(ac)| = 300mV	
	min	max	min	max
> 4.0	75	-	175	-
4.0	57	-	170	-
3.0	50	-	167	-
2.0	38	-	163	-
1.8	34	-	162	-
1.6	29	-	161	-
1.4	22	-	159	-
1.2	13	-	155	-
1.0	0	-	150	-
< 1.0	0	-	150	-

11.2.1 Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$, or $\overline{DQSU}$) has also to comply with certain requirements for single-ended signals.
CK and $\overline{CK}$ have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH(ac) / VIL(ac)) for ADD/CMD signals) in every half-cycle.
DQS, DQSL, DQSU, $\overline{DQS}$, $\overline{DQSL}$ have to reach VSEHmin / VSELmax (approximately the ac-levels (VIH(ac) / VIL(ac)) for DQ signals) in every half-cycle preceeding and following a valid transition.
Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g. if VIH150(ac)/VIL150(ac) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and $\overline{CK}$



Single-ended requirement for differential signals.

Note that while ADD/CMD and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDD/2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode charateristics of these signals.

Each single ended levels for CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$ or $\overline{DQSU}$

Symbol	Parameter	DDR3-800/1066/1333		Unit	Notes
		Min	Max		
VSEH	Single-ended high-level for strobes	VIH(ac)-VREFDQ+VDDQ/2	Note3	V	1, 2
	Single-ended high-level for CK, $\overline{CK}$	VIH(ac)-VREFCA+VDDQ/2	Note3	V	1, 2
VSEL	Single-ended low-level for strobes	Note3	VIL(ac)+VREFDQ-VDDQ/2	V	1, 2
	Single-ended low-level for CK, $\overline{CK}$	Note3	VIL(ac)+VREFCA-VDDQ/2	V	1, 2

Notes:
1. for CK, $\overline{CK}$ use VIH/VIL(ac) of ADD/CMD; for strobes (DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$) use VIH/VIL(ac) of DQs.
2. VIH(ac)/VIL(ac) for DQs is based on VREFDQ; VIH(ac)/VIL(ac) for ADD/CMD is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here
3. these values are not defined, however they single-ended signals CK, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.

11.3 AC and DC logic input levels for Differential Signals

Differential DC and AC input levels

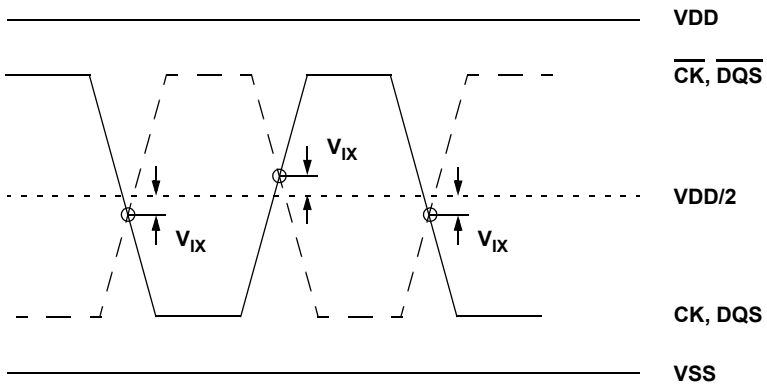
Symbol	Parameter	DDR3-800/1066/1333		Unit	Notes
		Min	Max		
VIHdiff	Differential input logic high	+ 200	-	mV	1
VILdiff	Differential input logic low	-	- 200		

Note :

1. Refer to "Overshoot and Undershoot specifications" on component datasheet

11.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in below table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signal to the midlevel between of VDD and VSS.



Vix Definition

Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	DDR3-800/1066/1333		Unit	Notes
		Min	Max		
VIX	Differential input Cross point voltage relative to VDD/2 for CK/$\overline{CK}$	-150	150	mV	
		-175	175	mV	1
VIX	Differential input Cross point voltage relative to VDD/2 for DQS/$\overline{DQS}$	-150	150	mV	

Note 1: Extended range for Vix is only allowed for clock and if single-ended clock input signals CK and $\overline{CK}$ are monotonic, have a single-ended swing VSEL/VSEH of at least VDD/2 +/-250 mV and if the differential slew rate of CK-$\overline{CK}$ is larger than 3 V/ns.

11.5 Slew rate definition for Single Ended Input Signals

11.5.1 Input Slew Rate for Input Setup Time (tIS) and Data Setup Time (tDS)

Setup (tIS and tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIH(AC)min. Setup (tIS and tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIL(AC)max.

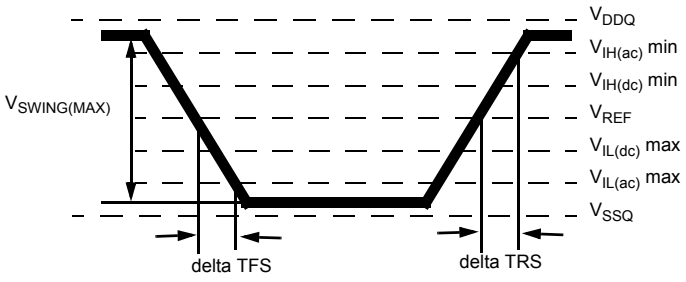
11.5.2 Input Slew Rate for Input Hold Time (tIH) and Data Hold Time (tDH)

Hold nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VRef. Hold (tIH & tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VRef

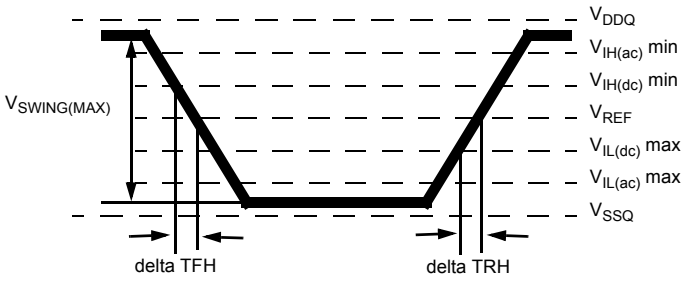
Description	Measured		Defined by	Applicable for
	From	To		
Input slew rate for rising edge	Vref	Vih(AC)min	Vih(AC)min-Vref / Delta TRS	Setup (tIS,tDS)
Input slew rate for falling edge	Vref	Vil(AC)max	Vref-Vil(AC)max / Delta TFS	
Input slew rate for rising edge	Vil(DC)max	Vref	Vref-Vil(DC)max / Delta TFH	Hold (tIH,tDH)
Input slew rate for falling edge	Vih(DC)min	Vref	Vih(DC)min-Vref / Delta TRH	

Single Ended Input Slew Rate definition

Notes: This nominal slew rate applies for linear signal waveforms.



< Figure : Input slew rate for setup>



< Figure : Input slew rate for Hold>

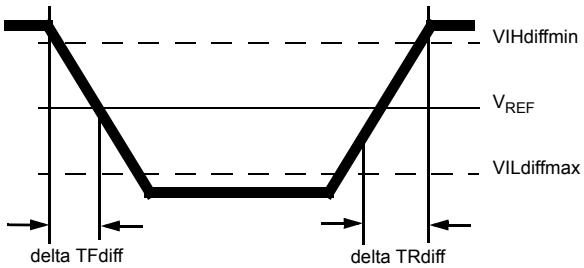
Input Nominal Slew Rate definition for Singel ended Signals

11.6 Slew rate definition for Differential Input Signals

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VILdiffmax	VIHdiffmin	VIHdiffmin - VILdiffmax / Delta TRdiff
Differential input slew rate for falling edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VIHdiffmin	VILdiffmax	VIHdiffmin - VILdiffmax / Delta TFdiff

Differential input slew rate definition

Note : The differential signal (i.e. CK - $\overline{CK}$ and DQS - $\overline{DQS}$) must be linear between these thresholds



Differential Input Slew Rate definition for DQS, $\overline{DQS}$ and CK, $\overline{CK}$

12.0 AC and DC Output Measurement Levels

12.1 Single Ended AC and DC Output Levels

Single Ended AC and DC output levels

Symbol	Parameter	DDR3-800/1066/1333	Units	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.8 x VDDQ	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.5 x VDDQ	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 x VDDQ	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	VTT + 0.1 x VDDQ	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	VTT - 0.1 x VDDQ	V	1

Note :

1. The swing of +/-0.1xVDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 34ohms and an effective test load of 25ohms to VTT=VDDQ/2.

12.2 Differential AC and DC Output Levels

Differential AC and DC output levels

Symbol	Parameter	DDR3-800/1066/1333	Units	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+0.2 x VDDQ	V	1
$V_{OLdiff(DC)}$	AC differential output low measurement level (for output SR)	-0.2 x VDDQ	V	1

Note :

1. The swing of +/-0.2xVDDQ is based on approximately 50% of the static singel ended output high or low swing with a driver impedance of 34ohms and an effective test load of 25ohms to VTT=VDDQ/2 at each of the differential outputs

12.3.Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in below Table and figure.

Single Ended Output slew rate definition

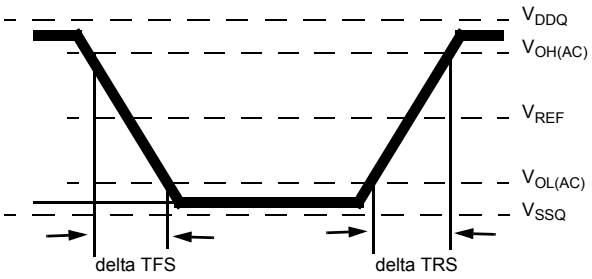
Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	VOH(AC)-VOL(AC) / Delta TRse
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	VOH(AC)-VOL(AC) / Delta TFse

Single Ended Output slew rate

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	2.5	5	2.5	5	2.5	5	V/ns

Note : Output slew rate is verified by design and characterization, and may not be subject to production test.

For Ron=RZQ/7 setting



Single Ended Output Slew Rate definition

12.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in below Table and figure.

Differential Output slew rate definition

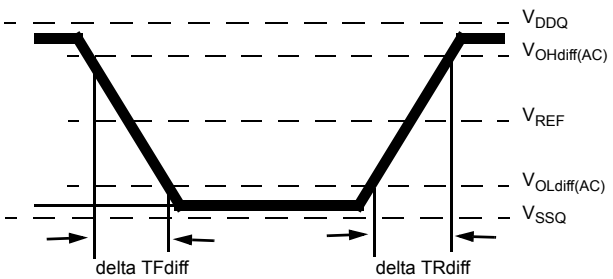
Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	VOHdiff(AC)-VOLdiff(AC) / Delta TRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	VOHdiff(AC)-VOLdiff(AC) / Delta TFdiff

Differential Output slew rate

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	5	10	5	10	5	10	V/ns

Note : Output slew rate is verified by design and characterization, and may not be subject to production test.

For Ron=RZQ/7 setting



Differential Output Slew Rate definition

13.0 IDD specification

(IDD values are for full operating range of Voltage and Temperature)

Symbol	Conditions	Max	Units	Notes
IDD0	**Operating one bank active-precharge current**; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	mA	
IDD1	**Operating one bank active-read-precharge current**; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC\ (IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	TBD	mA	
IDD2P	**Precharge power-down current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	mA	
IDD2Q	**Precharge quiet standby current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	mA	
IDD2N	**Precharge standby current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	mA	
IDD3P	**Active power-down current**; All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	mA	
IDD3N	**Active standby current**; All banks open; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	mA	
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RAS-max(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING;Data bus inputs are SWITCHING	TBD	mA	
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	TBD	mA	
IDD5B	**Burst refresh current**; $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	mA	
IDD6	**Self refresh current**; CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	TBD	mA	
IDD6ET	**Extended Temperature Range Self-Refresh Current**; CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled, Applicable for MR2 setting A6=0 and A7=1	TBD	mA	
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = $t_{RCD(IDD)}$-1*$t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RRD} = t_{RRD(IDD)}$, $t_{RCD} = 1*t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	TBD	mA	

13.1 IDD specification

M471B6474DZ1 : 512MB (64Mx64) Module

Symbol	F7 (DDR3 - 800 @ CL = 6)	F8 (DDR3 - 1066 @ CL = 7)	G8 (DDR3 - 1066 @ CL = 8)	H9 (DDR3 - 1333 @ CL = 9)	Units	Notes
IDD0	TBD	TBD	TBD	TBD	mA	
IDD1	TBD	TBD	TBD	TBD	mA	
IDD2P	TBD	TBD	TBD	TBD	mA	
IDD2Q	TBD	TBD	TBD	TBD	mA	
IDD2N	TBD	TBD	TBD	TBD	mA	
IDD3P	TBD	TBD	TBD	TBD	mA	
IDD3N	TBD	TBD	TBD	TBD	mA	
IDD4W	TBD	TBD	TBD	TBD	mA	
IDD4R	TBD	TBD	TBD	TBD	mA	
IDD5B	TBD	TBD	TBD	TBD	mA	
IDD6	TBD	TBD	TBD	TBD	mA	
IDD6ET	TBD	TBD	TBD	TBD	mA	
IDD6TC	TBD	TBD	TBD	TBD	mA	
IDD7	TBD	TBD	TBD	TBD	mA	

M471B2874DZ1 : 1GB (128Mx64) Module

Symbol	F7 (DDR3 - 800 @ CL = 6)	F8 (DDR3 - 1066 @ CL = 7)	G8 (DDR3 - 1066 @ CL = 8)	H9 (DDR3 - 1333 @ CL = 9)	Units	Notes
IDD0	TBD	TBD	TBD	TBD	mA	
IDD1	TBD	TBD	TBD	TBD	mA	
IDD2P	TBD	TBD	TBD	TBD	mA	
IDD2Q	TBD	TBD	TBD	TBD	mA	
IDD2N	TBD	TBD	TBD	TBD	mA	
IDD3P	TBD	TBD	TBD	TBD	mA	
IDD3N	TBD	TBD	TBD	TBD	mA	
IDD4W	TBD	TBD	TBD	TBD	mA	
IDD4R	TBD	TBD	TBD	TBD	mA	
IDD5B	TBD	TBD	TBD	TBD	mA	
IDD6	TBD	TBD	TBD	TBD	mA	
IDD6ET	TBD	TBD	TBD	TBD	mA	
IDD6TC	TBD	TBD	TBD	TBD	mA	
IDD7	TBD	TBD	TBD	TBD	mA	

M471B5673DZ1 : 2GB (256Mx64) Module

Symbol	F7 (DDR3 - 800 @ CL = 6)	F8 (DDR3 - 1066 @ CL = 7)	G8 (DDR3 - 1066 @ CL = 8)	H9 (DDR3 - 1333 @ CL = 9)	Units	Notes
IDD0	TBD	TBD	TBD	TBD	mA	
IDD1	TBD	TBD	TBD	TBD	mA	
IDD2P	TBD	TBD	TBD	TBD	mA	
IDD2Q	TBD	TBD	TBD	TBD	mA	
IDD2N	TBD	TBD	TBD	TBD	mA	
IDD3P	TBD	TBD	TBD	TBD	mA	
IDD3N	TBD	TBD	TBD	TBD	mA	
IDD4W	TBD	TBD	TBD	TBD	mA	
IDD4R	TBD	TBD	TBD	TBD	mA	
IDD5B	TBD	TBD	TBD	TBD	mA	
IDD6	TBD	TBD	TBD	TBD	mA	
IDD6ET	TBD	TBD	TBD	TBD	mA	
IDD6TC	TBD	TBD	TBD	TBD	mA	
IDD7	TBD	TBD	TBD	TBD	mA	

14.0 Input/Output Capacitance

14.1. 1Rx16 512MB SoDIMM

Parameter	Symbol	M471B6474DZ1				Units	Notes
		DDR3-800		DDR3-1066			
		Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	CIO	-	TBD	-	TBD	pF	
Input capacitance (CK and $\overline{CK}$)	CCK	-	TBD	-	TBD	pF	
Input capacitance (All other input-only pins)	CI	-	TBD	-	TBD	pF	
Input/output capacitance of ZQ pin	CZQ	-	TBD	-	TBD	pF	

14.2. 2Rx16 1GB SoDIMM

Parameter	Symbol	M471B2874DZ1				Units	Notes
		DDR3-800		DDR3-1066			
		Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	CIO	-	TBD	-	TBD	pF	
Input capacitance (CK and $\overline{CK}$)	CCK	-	TBD	-	TBD	pF	
Input capacitance (All other input-only pins)	CI	-	TBD	-	TBD	pF	
Input/output capacitance of ZQ pin	CZQ	-	TBD	-	TBD	pF	

14.3. 2Rx8 2GB SoDIMM

Parameter	Symbol	M471B5673DZ1				Units	Notes
		DDR3-800		DDR3-1066			
		Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	CIO	-	TBD	-	TBD	pF	
Input capacitance (CK and $\overline{CK}$)	CCK	-	TBD	-	TBD	pF	
Input capacitance (All other input-only pins)	CI	-	TBD	-	TBD	pF	
Input/output capacitance of ZQ pin	CZQ	-	TBD	-	TBD	pF	

15.0 Electrical Characteristics and AC timing

(0 °C<T_{CASE} ≤95 °C, V_{DDQ} = 1.5V ± 0.075V; V_{DD} = 1.5V ± 0.075V)

15.1 Refresh Parameters by Device Density

Parameter	Symbol		512Mb	1Gb	2Gb	4Gb	8Gb	Units
All Bank Refresh to active/refresh cmd time	tRFC		90	110	160	300	350	ns
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85°C	7.8	7.8	7.8	7.8	7.8	µs
		85 °C < T_{CASE} ≤ 95°C	3.9	3.9	3.9	3.9	3.9	µs

15.2 DDR3 SDRAM tRCD, tRP and tRC

Speed	DDR3-800	DDR3-1066		DDR3-1333	Units	Note
Bin (CL - tRCD - tRP)	6-6-6	7-7-7	8-8-8	9-9-9		
Parameter	min	min	min	min		
CL	6	7	8	9	tCK	
tRCD	15	13.13	15	13.5	ns	
tRP	15	13.13	15	13.5	ns	
tRAS	37.5	37.5	37.5	36	ns	
tRC	52.5	50.63	52.5	49.5	ns	
tRRD [1KB]	10	7.5	7.5	6	ns	
tRRD [2KB]	10	10	10	7.5	ns	
tFAW [1KB]	40	37.5	37.5	30	ns	
tFAW [2KB]	50	50	50	45	ns	

DDR3-800 Speed Bins

Speed		DDR3-800		Units	Note
CL-nRCD-nRP		6 - 6 - 6			
Parameter	Symbol	min	max		
Internal read command to first data	t_{AA}	15	20	ns	
ACT to internal read or write delay time	t_{RCD}	15	-	ns	
PRE command period	t_{RP}	15	-	ns	
ACT to ACT or REF command period	t_{RC}	52.5	-	ns	
ACT to PRE command period	t_{RAS}	37.5	9*tREFI	ns	9)
CL = 5 / CWL = 5	$t_{CK(AVG)}$	Reserved		ns	1)2)3)4)
CL = 6 / CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1)2)3)
Supported CL Settings		6		n_{CK}	
Supported CWL Settings		5		n_{CK}	

DDR3-1066 Speed Bins

Speed			DDR3-1066		DDR3-1066		Units	Note
CL-nRCD-nRP			7 - 7 - 7		8 - 8 - 8			
Parameter		Symbol	min	max	min	max		
Internal read command to first data		t_{AA}	13.125	20	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.125	-	15	-	ns	
PRE command period		t_{RP}	13.125	-	15	-	ns	
ACT to ACT or REF command period		t_{RC}	50.625	-	52.5	-	ns	
ACT to PRE command period		t_{RAS}	37.5	9*tREFI	37.5	9*tREFI	ns	8
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	ns	1,2,3,6
	CWL = 6	$t_{CK(AVG)}$	Reserved		Reserved		ns	1,2,3,4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	<2.5	Reserved		ns	1,2,3,4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	<2.5	1.875	<2.5	ns	1,2,3
Supported CL Settings			6,7,8		6,8		n_{CK}	
Supported CWL Settings			5,6		5,6		n_{CK}	

DDR3-1333 Speed Bins

Speed			DDR3-1333		Units	Note
CL-nRCD-nRP			9 -9 - 9			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.5	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.5	-	ns	
PRE command period		t_{RP}	13.5	-	ns	
ACT to ACT or REF command period		t_{RC}	49.5	-	ns	
ACT to PRE command period		t_{RAS}	36	9*tREFI	ns	8
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,7
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	<2.5	ns	1,2,3,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,
CL = 9	CWL = 5,6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,4
CL = 10	CWL = 5,6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3
			(Optional)		ns	5
Supported CL Settings			6,8,9		n_{CK}	
Supported CWL Settings			5,6,7		n_{CK}	

NOTES:

Absolute Specification (TOPER;VDDQ=VDD=1.5V +/- 0.075V);

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfiled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL'.
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CLSELECTED and round the resulting tCK(AVG) down to the next valid speed bin limit (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CLSELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. tREFI depends on TOPER

15.3 Timing parameters for DDR3-800, DDR3-1066 and DDR3-1333

Timing Parameters by Speed Bin

Speed		DDR3-800		DDR3-1066		DDR3-1333		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	$t_{CK(DLL\_OFF)}$	8	-	8	-	8	-	ns	6
Average Clock Period	$t_{CK(avg)}$	See Speed Bins Table						ps	f
Clock Period	$t_{CK(abs)}$	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Average high pulse width	$t_{CH(avg)}$	0.47	0.53	0.47	0.53	0.47	0.53	$t_{CK(avg)}$	f
Average low pulse width	$t_{CL(avg)}$	0.47	0.53	0.47	0.53	0.47	0.53	$t_{CK(avg)}$	f
Clock Period Jitter	$tJIT_{(per)}$	-100	100	-90	90	-80	80	ps	
Clock Period Jitter during DLL locking period	$tJIT_{(per,\ lck)}$	-90	90	-80	80	-70	70	ps	
Cycle to Cycle Period Jitter	$tJIT_{(cc)}$	200		180		160		ps	
Cycle to Cycle Period Jitter during DLL locking period	$tJIT_{(cc,\ lck)}$	180		160		140		ps	
Cumulative error across 2 cycles	$t_{ERR(2per)}$	- 147	147	- 132	132	- 118	118	ps	
Cumulative error across 3 cycles	$t_{ERR(3per)}$	- 175	175	- 157	157	- 140	140	ps	
Cumulative error across 4 cycles	$t_{ERR(4per)}$	- 194	194	- 175	175	- 155	155	ps	
Cumulative error across 5 cycles	$t_{ERR(5per)}$	- 209	209	- 188	188	- 168	168	ps	
Cumulative error across 6 cycles	$t_{ERR(6per)}$	- 222	222	- 200	200	- 177	177	ps	
Cumulative error across 7 cycles	$t_{ERR(7per)}$	- 232	232	- 209	209	- 186	186	ps	
Cumulative error across 8 cycles	$t_{ERR(8per)}$	- 241	241	- 217	217	- 193	193	ps	
Cumulative error across 9 cycles	$t_{ERR(9per)}$	- 249	249	- 224	224	- 200	200	ps	
Cumulative error across 10 cycles	$t_{ERR(10per)}$	- 257	257	- 231	231	- 205	205	ps	
Cumulative error across 11 cycles	$t_{ERR(11per)}$	- 263	263	- 237	237	- 210	210	ps	
Cumulative error across 12 cycles	$t_{ERR(12per)}$	- 269	269	- 242	242	- 215	215	PS	
Cumulative error across n = 13, 14 ... 49, 50 cycles	$t_{ERR(nper)}$	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 = 0.68ln(n))*tJIT(per)max						PS	24
Absolute clock HIGH pulse width	$t_{CH(abs)}$	0.43		0.43		0.43		$t_{CK(avg)}$	25
Absolute clock Low pulse width	$t_{CL(abs)}$	0.43		0.43		0.43		$t_{CK(avg)}$	26
Data Timing									
DQS,$\overline{DQS}$ to DQ skew, per group, per access	t_{DQSQ}	-	200	-	150	-	125	-	100
DQ output hold time from DQS, $\overline{DQS}$	t_{QH}	0.38	-	0.38	-	0.38	-	0.38	-
DQ low-impedance time from CK, $\overline{CK}$	$t_{LZ(DQ)}$	-800	400	-600	300	-500	250	-450	225
DQ high-impedance time from CK, $\overline{CK}$	$t_{HZ(DQ)}$	-	400	-	300	-	250	-	225
Data setup time to DQS, $\overline{DQS}$ referenced to Vih(ac)Vil(ac) levels	$t_{DS(base)}$	75	-	25	-	TBD	-	TBD	
Data hold time to DQS, $\overline{DQS}$ referenced to Vih(ac)Vil(ac) levels	$t_{DH(base)}$	150	-	100	-	TBD	-	TBD	
DQ and DM Input pulse width for each input	t_{DIPW}	600	-	490	-	400	-		
Data Strobe Timing									
DQS, $\overline{DQS}$ READ Preamble	t_{RPRE}	0.9	-	0.9	-	0.9	-	t_{CK}	13, 19, g
DQS, $\overline{DQS}$ differential READ Postamble	t_{RPST}	0.3	NOTE1	0.3	NOTE1	0.3	NOTE1	t_{CK}	11, 13, b
DQS, $\overline{DQS}$ output high time	t_{QSH}	0.38	-	0.38	-	0.4	-	$t_{CK(avg)}$	13, g
DQS, $\overline{DQS}$ output low time	t_{QSL}	0.38	-	0.38	-	0.4	-	$t_{CK(avg)}$	13, g
DQS, $\overline{DQS}$ WRITE Preamble	t_{WPRE}	0.9	-	0.9	-	0.9	-	t_{CK}	
DQS, $\overline{DQS}$ WRITE Postamble	t_{WPST}	0.3	-	0.3	-	0.3	-	t_{CK}	
DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$	t_{DQSCK}	-400	400	-300	300	-255	255	ps	13,f
DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1)	$t_{LZ(DQS)}$	-800	400	-600	300	-500	250	ps	13,14,f
DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	$t_{HZ(DQS)}$	-	400	-	300	-	250	ps	12,13,14
DQS, $\overline{DQS}$ differential input low pulse width	t_{DQSL}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
DQS, $\overline{DQS}$ differential input high pulse width	t_{DQSH}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	t_{DQSS}	-0.25	0.25	-0.25	0.25	-0.25	0.25	$t_{CK(avg)}$	c
DQS,$\overline{DQS}$ faling edge setup time to CK, $\overline{CK}$ rising edge	t_{DSS}	0.2	-	0.2	-	0.2	-	$t_{CK(avg)}$	c
DQS,$\overline{DQS}$ faling edge hold time to CK, $\overline{CK}$ rising edge	t_{DSH}	0.2	-	0.2	-	0.2	-	$t_{CK(avg)}$	c

Timing Parameters by Speed Bin (Cont.)

Speed		DDR3-800		DDR3-1066		DDR3-1333		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Command and Address Timing									
DLL locking time	t_{DLLK}	512	-	512	-	512	-	nCK	
internal READ Command to PRECHARGE Command delay	t_{RTP}	max ($4t_{CK}$,7.5ns)	-	max ($4t_{CK}$,7.5ns)	-	max ($4t_{CK}$,7.5ns)	-		e
Delay from start of internal write transaction to internal read command	t_{WTR}	max ($4t_{CK}$,7.5ns)	-	max ($4t_{CK}$,7.5ns)	-	max ($4t_{CK}$,7.5ns)	-		e,18
WRITE recovery time	t_{WR}	15	-	15	-	15	-	ns	e
Mode Register Set command cycle time	t_{MRD}	4	-	4	-	4	-	$t_{CK(avg)}$	
Mode Register Set command update delay	t_{MOD}	max ($12t_{CK}$,15ns)	-	max ($12t_{CK}$,15ns)	-	max ($12t_{CK}$,15ns)	-		
CAS# to CAS# command delay	t_{CCD}	4	-	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	$t_{DAL(min)}$	WR + roundup (t_{RP} / $t_{CK(AVG)}$)						nCK	
Multi-Purpose Register Recovery Time	t_{MPRR}	1	-	1	-	1	-	nCK	
ACTIVE to PRECHARGE command period	t_{RAS}	37.5	70,000	37.5	70,000	36	70,000	ns	e
ACTIVE to ACTIVE command period for 1KB page size	t_{RRD}	max ($4t_{CK}$,10ns)	-	max ($4t_{CK}$,7.5ns)	-	max ($4t_{CK}$,6ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	t_{RRD}	max ($4t_{CK}$,10ns)	-	max ($4t_{CK}$,10ns)	-	max ($4t_{CK}$,7.5ns)	-		e
Four activate window for 1KB page size	t_{FAW}	40	-	37.5	-	30	-	ns	e
Four activate window for 2KB page size	t_{FAW}	50	-	50	-	45	-	ns	e
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	$t_{IS(base)}$	200	-	125	-	65	-	ps	b,16
Command and Address hold time from CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	$t_{IH(base)}$	275	-	200	-	140	-		b,16
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	$t_{IS(base)}$ AC150	-	-	-	-	65+125	-	ps	b,16,27
Refresh Timing									
1Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	t_{RFC}	110	-	110	-	110	-	ns	
Average periodic refresh interval (0°C ≤ TCASE ≤ 85 °C)	t_{REFI}	7.8		7.8		7.8		us	
Average periodic refresh interval (85°C ≤ TCASE ≤ 95 °C)	t_{REFI}	3.9		3.9		3.9		us	
Calibration Timing									
Power-up and RESET calibration time	$t_{ZQinitI}$	512	-	512	-	512	-	t_{CK}	
Normal operation Full calibration time	t_{ZQoper}	256	-	256	-	256	-	t_{CK}	
Normal operation short calibration time	t_{ZQCS}	64	-	64	-	64	-	t_{CK}	23
Reset Timing									
Exit Reset from CKE HIGH to a valid command	t_{XPR}	max($5t_{CK}$, t_{RFC} + 10ns)	-	max($5t_{CK}$, t_{RFC} + 10ns)	-	max($5t_{CK}$, t_{RFC} + 10ns)	-		
Self Refresh Timing									
Exit Self Refresh to commands not requiring a locked DLL	t_{XS}	max($5t_{CK}$,t_{RFC} + 10ns)	-	max($5t_{CK}$,t_{RFC} + 10ns)	-	max($5t_{CK}$,t_{RFC} + 10ns)	-		
Exit Self Refresh to commands requiring a locked DLL	t_{XSDLL}	t_{DLLK}(min)	-	t_{DLLK}(min)	-	t_{DLLK}(min)	-	t_{CK}	
Minimum CKE low width for Self refresh entry to exit timing	t_{CKESR}	t_{CKE}(min) + $1t_{CK}$	-	t_{CKE}(min) + $1t_{CK}$	-	t_{CKE}(min) + $1t_{CK}$	-		
Valid Clock Requirement after Self Refresh Entry (SRE)	t_{CKSRE}	max($5t_{CK}$,10ns)	-	max($5t_{CK}$,10ns)	-	max($5t_{CK}$,10ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX)	t_{CKSRX}	max($5t_{CK}$,10ns)	-	max($5t_{CK}$,10ns)	-	max($5t_{CK}$,10ns)	-		

Timing Parameters by Speed Bin (Cont.)

Speed		DDR3-800		DDR3-1066		DDR3-1333		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Power Down Timing									
Exit Power Down with DLL on to any valid command;Exit Percharge Power Down with DLL frozen to commands not requiring a locked DLL	t_{XP}	max ($3t_{CK}$,7.5ns)	-	max ($3t_{CK}$,7.5ns)	-	max ($3t_{CK}$,6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	max ($10t_{CK}$,24ns)	-	max ($10t_{CK}$,24ns)	-	max ($10t_{CK}$,24ns)	-		2
CKE minimum pulse width	t_{CKE}	max ($3t_{CK}$,7.5ns)	-	max ($3t_{CK}$,5.625ns)	-	max ($3t_{CK}$,5.625ns)	-		
Command pass disable delay	t_{CPDED}	1	-	1	-	1	-	nCK	
Power Down Entry to Exit Timing	t_{PD}	t_{CKE}(min)	$9*t_{REFI}$	t_{CKE}(min)	$9*t_{REFI}$	t_{CKE}(min)	$9*t_{REFI}$	t_{CK}	15
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	1	-	1	-	1	-	nCK	20
Timing of PRE command to Power Down entry	t_{PRPDEN}	1	-	1	-	1	-	nCK	20
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	RL + 4 +1	-	RL + 4 +1	-	RL + 4 +1	-		
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	t_{WRPDEN}	WL + 4 +(t_{WR}/ t_{CK})	-	WL + 4 +(t_{WR}/ t_{CK})	-	WL + 4 +(t_{WR}/ t_{CK})	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	$t_{WRAPDEN}$	WL + 4 +WR +1	-	WL + 4 +WR +1	-	WL + 4 +WR +1	-	nCK	10
Timing of WR command to Power Down entry (BL4MRS)	t_{WRPDEN}	WL + 2 +(t_{WR}/ t_{CK})	-	WL + 2 +(t_{WR}/ t_{CK})	-	WL + 2 +(t_{WR}/ t_{CK})	-	nCK	9
Timing of WRA command to Power Down entry (BL4MRS)	$t_{WRAPDEN}$	WL +2 +WR +1	-	WL +2 +WR +1	-	WL +2 +WR +1	-	nCK	10
Timing of REF command to Power Down entry	$t_{REFPDEN}$	1	-	1	-	1	-		20,21
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	$t_{MOD(min)}$	-	$t_{MOD(min)}$	-	$t_{MOD(min)}$	-	t_{CK}	
ODT Timing									
ODT high time without write command or with wirte command and BC4	ODTH4	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK	
Asynchronous RTT tum-on delay (Power-Down with DLL frozen)	t_{AONPD}	1	9	1	9	1	9	ns	
Asynchronous RTT tum-off delay (Power-Down with DLL frozen)	t_{AOFPD}	1	9	1	9	1	9	ns	
ODT turn-on	t_{AON}	-400	400	-300	30	-250	250	ps	7,f
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	t_{AOF}	0.3	0.7	0.3	0.7	0.3	0.7	$t_{CK(avg)}$	8,f
RTT dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	0.3	0.7	$t_{CK(avg)}$	f
Write Leveling Timing									
First DQS pulse rising edge after tDQSS margining mode is programmed	t_{WLMRD}	40	-	40	-	40	-	t_{CK}	3
DQS/DQS delay after tDQS margining mode is programmed	$t_{WLDQSEN}$	25	-	25	-	25	-	t_{CK}	3
Setup time for tDQSS latch	t_{WLS}	325	-	245	-	195	-	ps	
Hold time of tDQSS latch	t_{WLH}	325	-	245	-	195	-	ps	
Write leveling output delay	t_{WLO}	0	9	0	9	0	9	ns	
Write leveling output error	t_{WLOE}	0	2	0	2	0	2	ns	

Jitter Notes

Specific Note a
Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. ex) tMRD =4 [nCK] means; if one Mode Register Set command is registered at Tm, anothe Mode Register Set commdn may be registered at Tm+4, even if (Tm+4-Tm) is 4 x tCK(avg) +tERR(4per) min.

Specific Note b
These parameters are measured from a command/address signal (CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

Specific Note c
These parameters are measured from a data strobe signal (DQS(L/U), $\overline{DQS}$(L/U)) crossing to its respective clock signal (CK, $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing.
That is, these parameters should be met whether clock jitter is present or not.

Specific Note d
These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), $\overline{DQS}$(L/U)) crossing.

Specific Note e
For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU{ tPARAM [ns] / tCK(avg) [ns] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied.
For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU{tRP / tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.

Specific Note f
When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper),act of the input clock, where 2 <= m <= 12. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR3-800 SDRAM has tERR(mper),act,min = - 172 ps and tERR(mper),act,max = + 193 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = - 400 ps - 193 ps = - 593 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400 ps + 172 ps = + 572 ps. Similarly, tLZ(DQ) for DDR3-800 derates to tLZ(DQ),min(derated) = - 800 ps - 193 ps = - 993 ps and tLZ(DQ),max(derated) = 400 ps + 172 ps = + 572 ps. (Caution on the min/max usage!)
Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 <= n <= 12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 <= n <= 12

Specific Note g
When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act = 2500 ps, tJIT(per),act,min = - 72 ps and tJIT(per),act,max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500 ps - 72 ps = + 2178 ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)

Timing Parameter Notes

1. Actual value dependant upon measurement level definitions which are TBD.

2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.

3. The max values are system dependent.

4. WR as programmed in mode register

5. Value must be rounded-up to next higher integer value

6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.

7. For definition of RTT turn-on time tAON see "Device Operation"

8. For definition of RTT turn-off time tAOF see "Device Operation".

9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.

10. WR in clock cycles as programmed in MR0

11. The maximum postamble is bound by tHZDQS(max)

12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD

13. Value is only valid for RON34

14. Single ended signal parameter. Refer to chapter <8, 9> for definition and measurement method.

15. tREFI depends on TOPER

16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, $\overline{CK}$ differential slew rate, Note for DQ and DM signals, VREF(DC) = VrefDQ(DC). FOr input only pins except RESET, VRef(DC)=VRefCA(DC).
See "Address/ Command Setup, Hold and Derating" on page 52.

17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, $\overline{DQS}$ differential slew rate. Note for DQ and DM signals, VREF(DC)= VRefDQ(DC). For input only pins except $\overline{RESET}$, VRef(DC)=VRefCA(DC).
See "Data Setup, Hold and Slew Rate Derating" on page 58.

18. Start of internal write transaction is definited as follows ;
For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL
For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL

19. The maximum preamble is bound by tLZDQS(max)

20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

21. Altough CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See "Device Operation".

22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) For example, if TSens = 1.5% /°C, VSens = 0.15% / mV, Tdriftrate = 1°C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \simeq 128\text{ms}$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.

25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

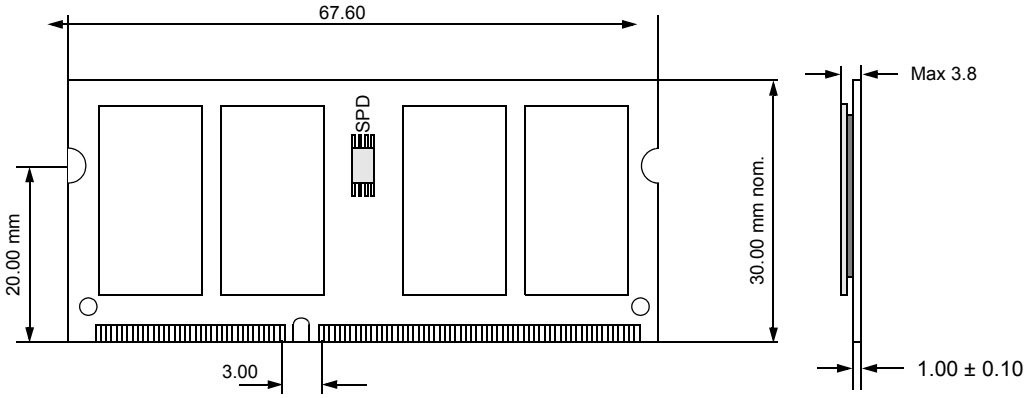
26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

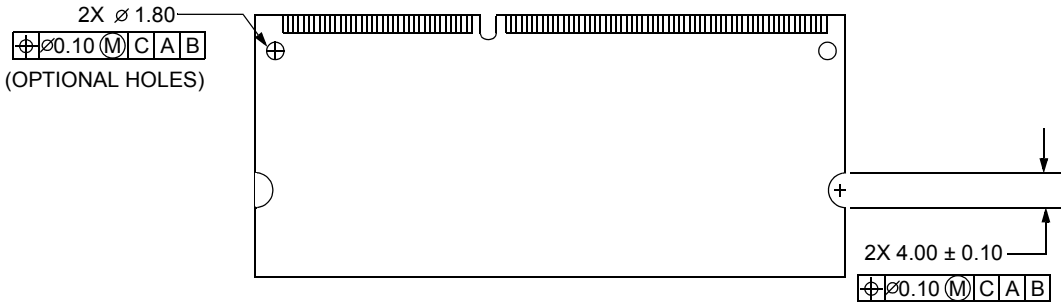
27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].

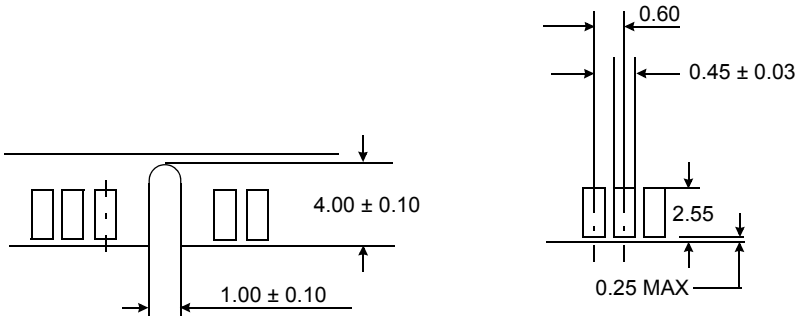
16.0 Physical Dimensions :

16.1 64Mbx16 based 64Mx64 Module(1 Rank)

Units : Millimeters





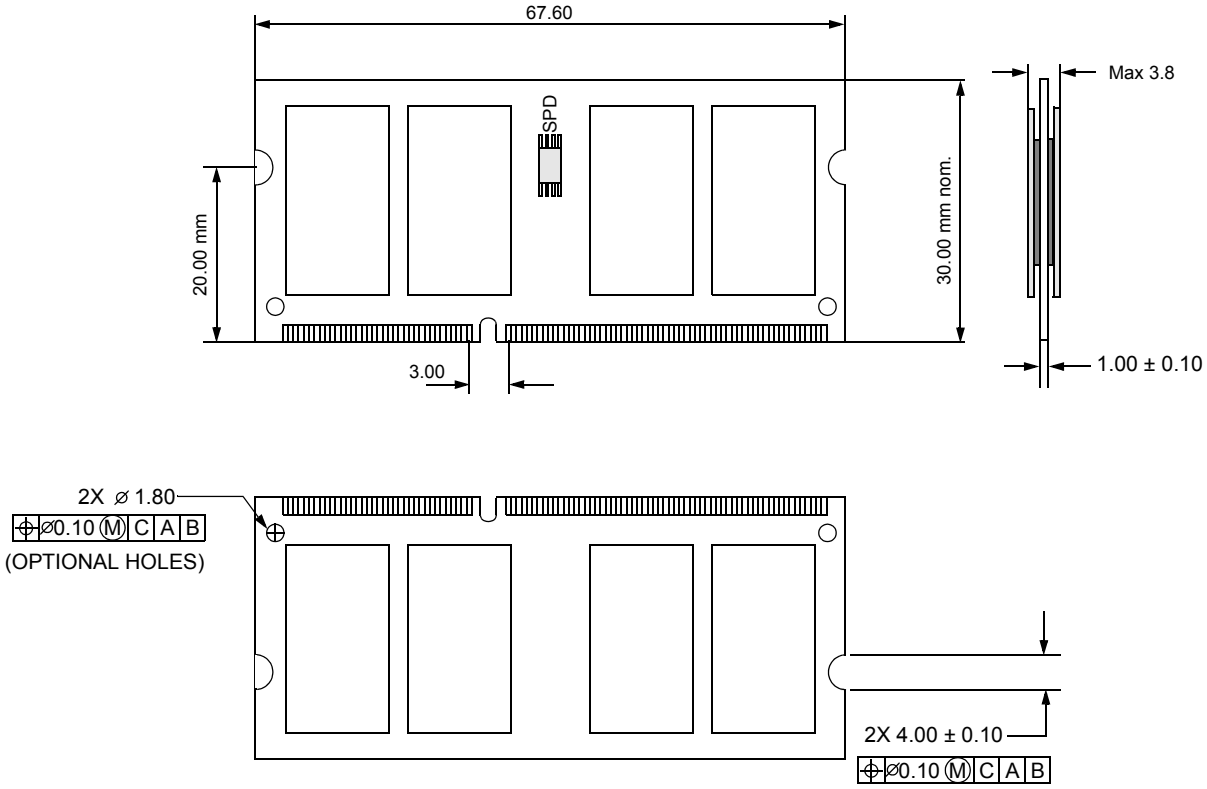


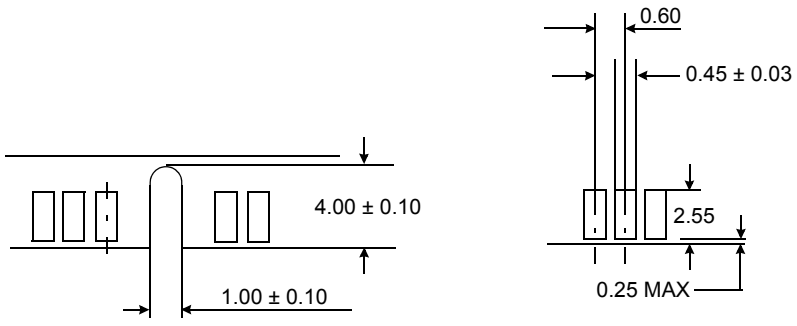
Detail A **Detail B**

The used device is 64M x16 DDR3 SDRAM, FBGA.
DDR3 SDRAM Part NO : K4B1G1646D - HC**

16.2 64Mbx16 based 128Mx64 Module(2 Ranks)

Units : Millimeters



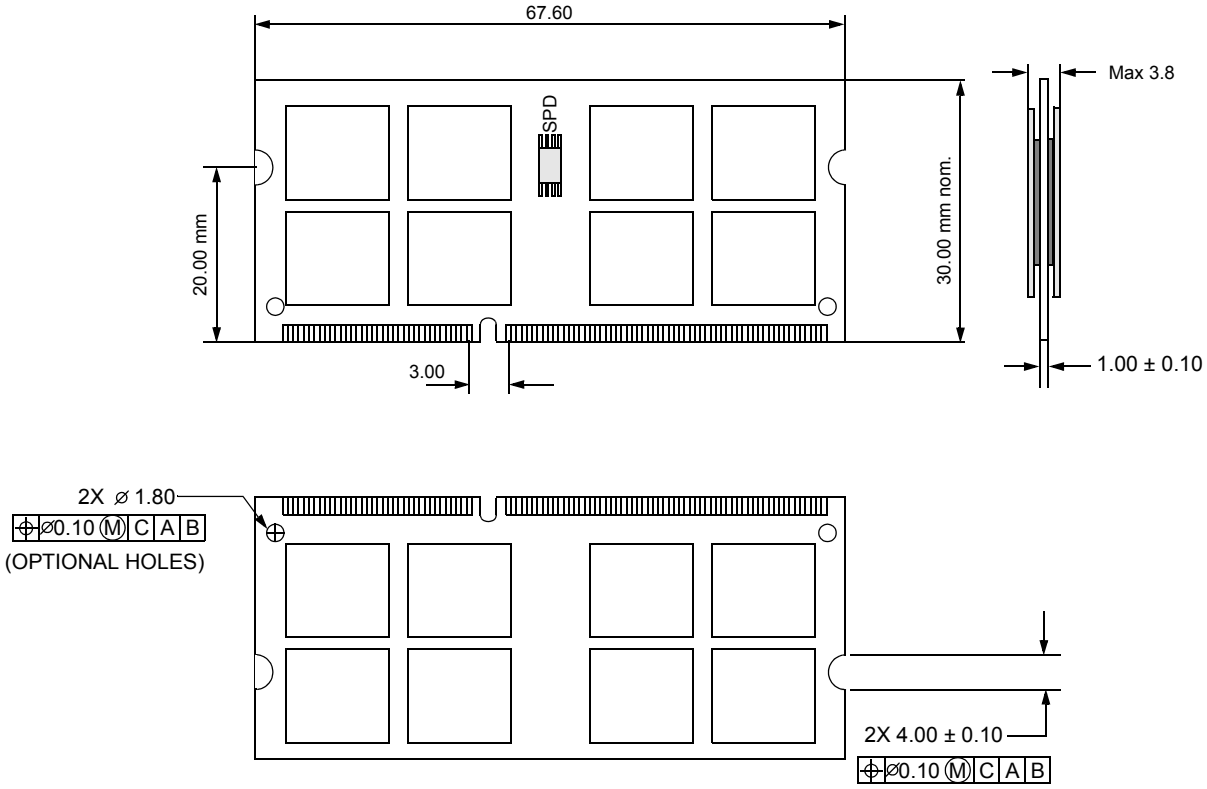


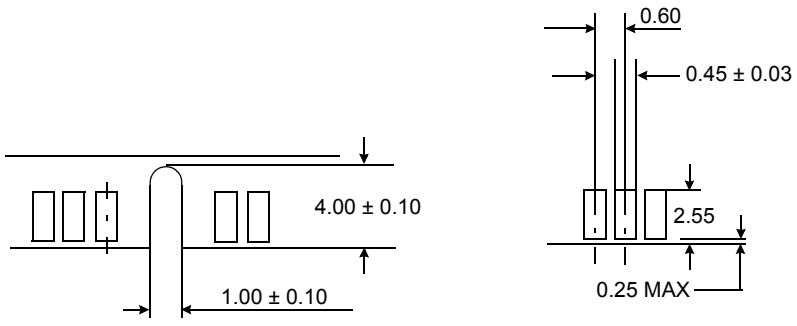
Detail A **Detail B**

The used device is 64M x16 DDR3 SDRAM, FBGA.
DDR3 SDRAM Part NO : K4B1G1646D - HC**

16.3 128Mbx8 based 256Mx64 Module(2 Ranks)

Units : Millimeters





Detail A **Detail B**

The used device is 128M x8 DDR3 SDRAM, FBGA.
DDR3 SDRAM Part NO : K4B1G0846D - HC**