

4M × 32 -Bit Dynamic RAM Module SMALL OUTLINE MEMORY MODULE

HYM 32V4020GD(L)-50/-60

Advanced Information

- 72-Pin Small Outline Dual-in-Line Memory Module
- 4 194 034 words by 32-bit organization
- Performance:

		-50	-60	
t _{RC}	Read / Write Cycle Time	90	110	ns
t _{RAC}	RAS Access Time	50	60	ns
t _{CAC}	CAS Access Time	13	15	ns
t _{AA}	Access Time From Address	25	30	ns
t _{PC}	Fast Page Mode Cycle Time	35	40	ns

- Single + 3.3 V (± 0.3 V) supply
- Low power dissipation
max. 2880 mW active (-50 version)
max. 2592 mW active (-60 version)

LVTLL - 57.6 mw standby
LVCMOS- 28.8 mW standby
LVCMOS- 5.76 mW standby (L-version)
- Fast Page Mode
- Low Power Versions with Self Refresh
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only-refresh
- 8 decoupling capacitors mounted on substrate
- All inputs, outputs and clock fully TTL compatible
- Utilizes eight 4M × 4 -DRAMs in TSOPII-packages
- Card size 59.69mm x 25.40mm x 3.80 mm
- 12 / 10 Addressing (Row/Column)
- 4096 refresh cycles / 64 ms, 128 ms for L-versions
- Gold contact pad

The HYM 32V4020GD(L) -50/-60 are 16 MByte DRAM 72pin small outline dual-in-line memory modules organized as 4M x 32, comprising eight HYB3116400BT(L) 4M x 4 DRAMs in 300 mil wide TSOPII-26/24 - packages mounted together with eight 0.2 µF ceramic decoupling capacitors on a PC board. These modules are optimized for use in byte-write non-parity applications. Each HYB 3116400BT(L) is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The density and speed of the module can be detected by the use of presence detect pins.

These modules are ideal for portable systems applications where high memory capacity is needed.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 32V4020GD -50		L-DIM-72-3	50 ns DRAM module
HYM 32V4020GD -60		L-DIM-72-3	60 ns DRAM module
HYM 32V4020GDL -50		L-DIM-72-3	50 ns Low Power DRAM module
HYM 32V4020GDL -60		L-DIM-72-3	60 ns Low Power DRAM module

Pin Names

A0-A11	Row Address Input
A0-A9	Column Address Inputs
DQ0 - DQ31	Data Input/Output
RAS0, RAS2	Row Address Strobe
CAS0 - CAS3	Column Address Strobe
WE	Read / Write Input
Vcc	Power (+3.3 Volt)
Vss	Ground
PD1 - PD7	Presence Detect Pins
N.C.	No Connection

Presence-Detect Truth Table *):

Module	PD1	PD2	PD3	PD4	PD5	PD6	PD7
HYM 32V4020GD -50	NC	NC	VSS	NC	VSS	VSS	NC
HYM 32V4020GD -60	NC	NC	VSS	NC	NC	NC	NC
HYM 32V4020GDL -50	NC	NC	VSS	NC	VSS	VSS	VSS
HYM 32V4020GDL -60	NC	NC	VSS	NC	NC	NC	VSS

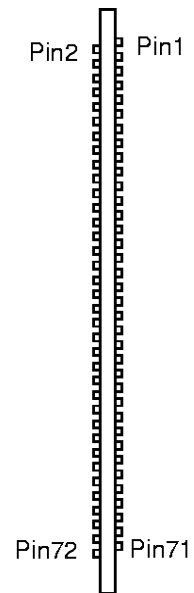
*) note: PD1...PD4 : configuration
 PD5..PD6 : speed
 PD7 : refresh mode

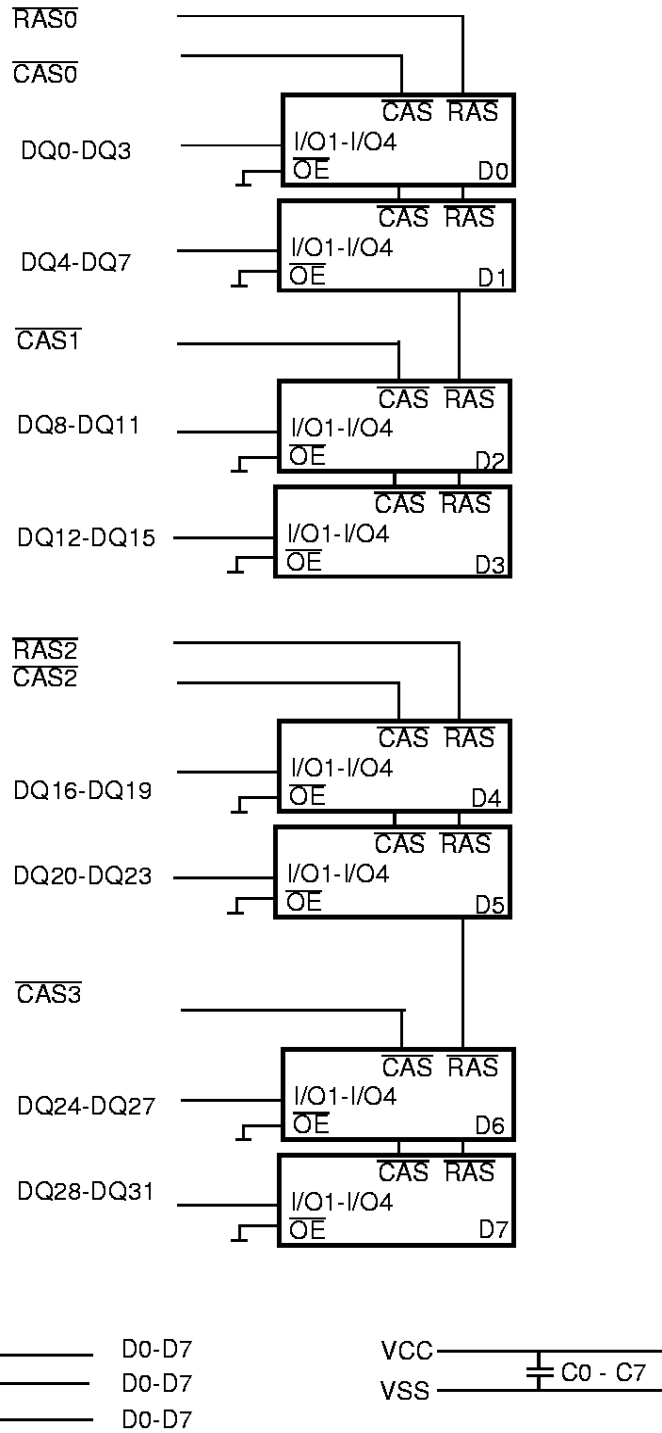
Pin Configuration

PIN	Name	PIN	NAME	PIN	NAME	PIN	NAME
1	VSS	37	DQ16	2	DQ0	38	DQ17
3	DQ1	39	VSS	4	DQ2	40	CAS0
5	DQ3	41	CAS2	6	DQ4	42	CAS3
7	DQ5	43	CAS1	8	DQ6	44	RAS0
9	DQ7	45	NC	10	VCC	46	NC
11	PD1	47	WRITE	12	A0	48	NC
13	A1	49	DQ18	14	A2	50	DQ19
15	A3	51	DQ20	16	A4	52	DQ21
17	A5	53	DQ22	18	A6	54	DQ23
19	A10	55	NC	20	NC	56	DQ24
21	DQ8	57	DQ25	22	DQ9	58	DQ26
23	DQ10	59	DQ28	24	DQ11	60	DQ27
25	DQ12	61	VCC	26	DQ13	62	DQ29
27	DQ14	63	DQ30	28	A7	64	DQ31
29	A11	65	NC	30	VCC	66	PD2
31	A8	67	PD3	32	A9	68	PD4
33	NC	69	PD5	34	RAS2	70	PD6
35	DQ15	71	PD7	36	NC	72	VSS

Front Side

Back Side





Block Diagram

Absolute Maximum Ratings

Operating temperature range.....	0 to 70 °C
Storage temperature range.....	- 55 to 150 °C
Input/output voltage.....	-0.5 to min (V _{CC} +0.5,4.6) V
Power supply voltage.....	-0.5V to 4.6 V
Power dissipation.....	1.0 W
Data out current (short circuit).....	50 mA

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Input high voltage	V _{IH}	2.0	V _{CC} +0.3	V	1)
Input low voltage	V _{IL}	- 0.3	0.8	V	1)
Output high voltage (LVTTL) Output „H“ level voltage (I _{out} = -2mA)	V _{OH}	2.4	-	V	1)
Output low voltage (LVTTL) Output „L“ level voltage (I _{out} = +2mA)	V _{OL}	-	0.4	V	1)
Output high voltage (LVCMOS) Output „H“ level voltage (I _{out} = -100uA)	V _{OH}	V _{CC} -0.2	-	V	1)
Output low voltage (LVCMOS) Output „L“ level voltage (I _{out} = +100uA)	V _{OL}	-	0.2	V	1)
Input leakage current, any input (0 V < V _{in} < V _{CC} , all other pins = 0 V)	I _{I(L)}	- 10	10	μA	
Output leakage current (DO is disabled, 0 V < V _{out} < V _{CC})	I _{O(L)}	- 10	10	μA	
Average V _{CC} supply current: -50 ns version -60 ns version (\overline{RAS} , \overline{CAS} , address cycling: t _{RC} = t _{RC} min.)	I _{CC1}	-	800 720	mA mA	2) 3) 4)
Standby V _{CC} supply current ($\overline{RAS}=\overline{CAS}=V_{IH}$)	I _{CC2}	-	16	mA	-
Average V _{CC} supply current, during RAS-only refresh cycles: -50 ns version -60 ns version (RAS cycling: CAS = V _{IH} ; t _{RC} = t _{RC} min.)	I _{CC3}	-	800 720	mA mA	2) 3)

DC Characteristics (cont'd)

$T_A = 0$ to 70 °C, $V_{SS} = 0$ V, $V_{CC} = 3.3$ V \pm 0.3 V

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Average V_{CC} supply current, during fast page mode: -50 ns version -60 ns version ($\overline{RAS} = V_{IL}$, \overline{CAS} , address cycling: $t_{PC} = t_{PC}$ min.)	I_{CC4}	–	320 280	mA mA	2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V)	I_{CC5}	–	8	mA	–
Standby V_{CC} supply current (L-version) ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V)	I_{CC5}	–	1.6	mA	–
Average V_{CC} supply current, during \overline{CAS} -before- \overline{RAS} refresh mode: -50 ns version -60 ns version (\overline{RAS} , \overline{CAS} cycling: $t_{RC} = t_{RC}$ min.)	I_{CC6}	–	800 720	mA mA	2) 4)
Self Refresh Current (L-version only) CBR cycle with $\overline{RAS} > t_{RASS(min.)}$; \overline{CAS} held low; $\overline{WE} = V_{CC} - 0.2$ V; Addresses and $D_i = V_{CC} - 0.2$ V or 0.2 V	I_{CC7}	–	2	mA	

Capacitance

$T_A = 0$ to 70 °C, $V_{CC} = 3.3$ V \pm 0.3 V, $f = 1$ MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A_0 to A_{11} , \overline{WE})	C_{I1}	–	55	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	40	pF
Input capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{I3}	–	25	pF
I/O capacitance (DQ_0 - DQ_{31})	C_{I0}	–	15	pF

AC Characteristics ⁵⁾⁶⁾

$T_A = 0$ to 70 °C, $V_{CC} = 5$ V \pm 10 %, $t_T = 5$ ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

common parameters

Random read or write cycle time	t_{RC}	90	–	110	–	ns	
\overline{RAS} precharge time	t_{RP}	30	–	40	–	ns	
\overline{RAS} pulse width	t_{RAS}	50	10k	60	10k	ns	
\overline{CAS} pulse width	t_{CAS}	13	10k	15	10k	ns	
\overline{CAS} precharge time	t_{CP}	10	–	10	–	ns	
Row address setup time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	15	–	ns	
\overline{RAS} to \overline{CAS} delay time	t_{RCD}	18	37	20	45		
\overline{RAS} to column address delay time	t_{RAD}	13	25	15	30	ns	
\overline{RAS} hold time	t_{RSH}	13		15	–	ns	
\overline{CAS} hold time	t_{CSH}	50		60	–	ns	
\overline{CAS} to \overline{RAS} precharge time	t_{CRP}	5	–	5	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	7
Refresh period	t_{REF}	–	64	–	64	ms	
Refresh period (L-version)	t_{REF}	–	128	–	128	ms	

Read Cycle

Access time from \overline{RAS}	t_{RAC}	–	50	–	60	ns	8, 9
Access time from \overline{CAS}	t_{CAC}	–	13	–	15	ns	8, 9
Access time from column address	t_{AA}	–	25	–	30	ns	8,10
Column address to \overline{RAS} lead time	t_{RAL}	25	–	30	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	11
Read command hold time referenced to \overline{RAS}	t_{RRH}	0	–	0	–	ns	11
\overline{CAS} to output in low-Z	t_{CLZ}	0	–	0	–	ns	8
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	12

AC Characteristics (cont'd) ⁵⁾⁶⁾

$T_A = 0$ to 70 °C, $V_{CC} = 5$ V \pm 10 %, $t_T = 5$ ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

Early Write Cycle

Write command hold time	t_{WCH}	8	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	ns	13
Write command to \overline{RAS} lead time	t_{RWL}	13	–	15	–	ns	
Write command to \overline{CAS} lead time	t_{CWL}	13	–	15	–	ns	
Data setup time	t_{DS}	0	–	0	–	ns	14
Data hold time	t_{DH}	10	–	10	–	ns	14

Fast Page Mode Cycle

Fast page mode cycle time	t_{PC}	35	–	40	–	ns	
Access time from \overline{CAS} precharge	t_{CPA}	–	30	–	35	ns	7
\overline{RAS} pulse width	t_{RAS}	50	200k	60	200k	ns	
\overline{CAS} precharge to \overline{RAS} Delay	t_{RHCP}	30	–	35	–	ns	

\overline{CAS} -before- \overline{RAS} refresh cycle

\overline{CAS} setup time	t_{CSR}	10	–	10	–	ns	
\overline{CAS} hold time	t_{CHR}	10	–	10	–	ns	
\overline{RAS} to \overline{CAS} precharge time	t_{RPC}	5	–	5	–	ns	
Write to \overline{RAS} precharge time	t_{WRP}	10	–	10	–	ns	
Write hold time referenced to \overline{RAS}	t_{WRH}	10	–	10	–	ns	

Self Refresh Cycle (L-version only)

\overline{RAS} pulse width	t_{RASS}	100k	–	100k	–	ns	
\overline{RAS} precharge time	t_{RPS}	95	–	110	–	ns	
\overline{CAS} hold time	t_{CHS}	-50	–	-50	–	ns	

Notes:

- 1) All voltages are referenced to VSS.
- 2) ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.
- 3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.
- 4) Address can be changed once or less while $\overline{\text{RAS}} = \text{VIL}$. In the case of ICC4 it can be changed once or less during a fast page mode cycle (tPC).
- 5) An initial pause of 200 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
- 6) AC measurements assume $t_T = 5 \text{ ns}$.
- 7) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL} .
- 8) Measured with a load equivalent to 2 TTL loads and 100 pF.
- 9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.
- 10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.
- 11) Either tRCH or tRRH must be satisfied for a read cycle.
- 12) tOFF (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels
- 13) tWCS is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If $tWCS > tWCS(\text{min.})$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle.
- 14) These parameters are referenced to the $\overline{\text{CAS}}$ leading edge.

SO-DIMM PACKAGE OUTLINES

