

Asymmetric Dual N-Channel Enhancement Mode MOSFET

MTNN8451KQ8

	FET1	FET 2
BV_{DSS}	30V	30V
I_D	6.8A	10.2A
$R_{DS(ON)(TYP.)}@V_{GS}=10V$	15m Ω	11m Ω
$R_{DS(ON)(TYP.)}@V_{GS}=4.5V$	23m Ω	18m Ω

Description

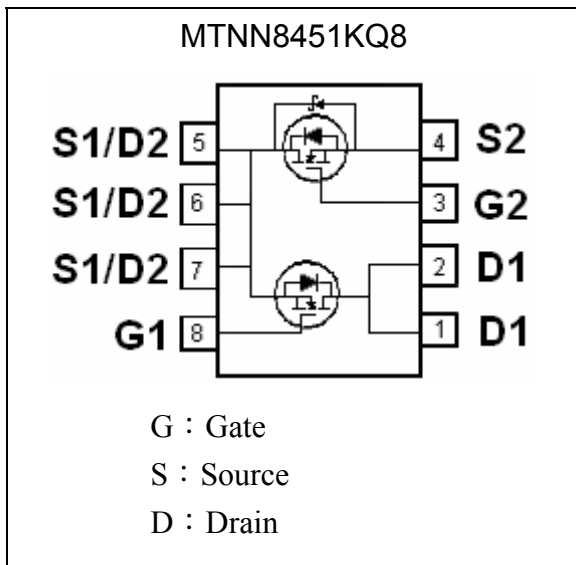
The MTNN8451KQ8 uses advanced trench technology to provide excellent $R_{DS(on)}$ and low gate charge. The two MOSFETs make a compact and efficient switch and synchronous rectifier combination for use in DC-DC converters. A Schottky diode in parallel with the synchronous MOSFET to boost efficiency further.

The SOP-8 package is universally preferred for all commercial-industrial surface mount applications.

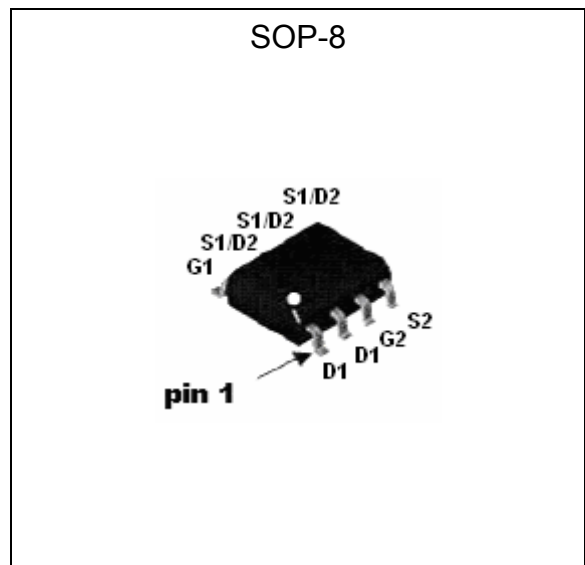
Features

- Simple drive requirement
- Low on-resistance
- Fast switching speed
- Pb-free lead plating and halogen-free package

Equivalent Circuit



Outline





Absolute Maximum Ratings (T_C=25°C, unless otherwise noted)

Parameter	Symbol	Limits		Unit	
		FET 1	FET 2		
Drain-Source Breakdown Voltage	BV _{DSS}	30	30	V	
Gate-Source Voltage	V _{GS}	±20	±20		
Continuous Drain Current (Note 2)	I _D	TA=25 °C, V _{GS} =10V	6.8	10.2	A
		TA=70 °C, V _{GS} =10V	5.4	8.1	
Pulsed Drain Current (Note 1)	I _{DM}	30	40		
Power Dissipation	P _D	1.2 (Note 2)	2 (Note 2)	W	
		0.7 (Note 3)	1.1 (Note 3)		
Operating Junction and Storage Temperature Range	T _j ; T _{stg}	-55~+150		°C	

Thermal Data

Parameter	Symbol	Value		Unit
Thermal Resistance, Junction-to-case, max	R _{th,j-c}	40		°C/W
Thermal Resistance, Junction-to-ambient, max	R _{th,j-a}	104 (Note 2)	62.5 (Note 2)	°C/W
		178 (Note 3)	114 (Note 3)	°C/W

- Note : 1.Pulse width limited by maximum junction temperature.
 2.Surface mounted on 1 in² copper pad of FR-4 board, pulse width≤10s.
 3.Surface mounted on minimum copper pad, pulse width≤10s.

FET 1 Electrical Characteristics (T_J=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	30	-	-	V	V _{GS} =0, I _D =250μA
V _{GS(th)}	1.0	1.7	2.5	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0
I _{DSS}	-	-	1	μA	V _{DS} =30V, V _{GS} =0
	-	-	10		V _{DS} =24V, V _{GS} =0, T _J =125°C
*R _{DSON}	-	15	20	mΩ	V _{GS} =10V, I _D =6A
	-	23	28		V _{GS} =4.5V, I _D =4A
*G _{FS}	-	7.6	-	S	V _{DS} =5V, I _D =5A
Dynamic					
C _{iss}	-	727	-	pF	V _{DS} =15V, V _{GS} =0, f=1MHz
C _{oss}	-	79	-		
C _{rss}	-	70	-		
*t _{d(ON)}	-	3.7	-	ns	V _{DS} =15V, I _D =1A, V _{GS} =10V, R _G =3 Ω
*t _r	-	3.2	-		
*t _{d(OFF)}	-	10	-		
*t _f	-	3.6	-		
*Q _g	-	9.3	-	nC	V _{DS} =15V, I _D =6A, V _{GS} =10V
*Q _{gs}	-	2.6	-		
*Q _{gd}	-	3.2	-		
R _g	-	2.2	-	Ω	V _{GS} =15mV, V _{DS} =0V, f=1MHz



Body Diode					
*Is	-	-	3	A	
*ISM	-	-	12		
*VSD	-	0.73	1	V	VGS=0V, Is=1A
*trr	-	15	-	ns	Is=6A, VGS=0V, dI/dt=100A/μs
*Qrr	-	9	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

FET 2 Electrical Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BVDSS	30	-	-	V	VGS=0, ID=250μA
VGS(th)	1.0	1.8	2.5		VDS=VGS, ID=250μA
IGSS	-	-	±100	nA	VGS=±20V, VDS=0
IDSS	-	-	50	μA	VDS=24V, VGS=0
	-	-	25	mA	VDS=24V, VGS=0, Tj=125°C
*RDS(ON)	-	11	15	mΩ	VGS=10V, ID=9A
	-	18	23		VGS=4.5V, ID=7A
*GFS	-	9	-	S	VDS=5V, ID=5A
Dynamic					
Ciss	-	1090	-	pF	VDS=15V, VGS=0, f=1MHz
Coss	-	149	-		
Crss	-	105	-		
*td(ON)	-	5.8	-	ns	VDS=15V, ID=1A, VGS=10V, RG=3Ω
*tr	-	4.7	-		
*td(OFF)	-	16	-		
*tf	-	5.4	-		
*Qg	-	12.7	-	nC	VDS=15V, ID=9A, VGS=10V
*Qgs	-	4.5	-		
*Qgd	-	4.6	-		
Rg	-	2	-	Ω	VGS=15mV, VDS=0V, f=1MHz
Body Diode					
*Is	-	-	4.5	A	
*ISM	-	-	18		
*VSD	-	0.5	0.6	V	VGS=0V, Is=1A
*trr	-	20	-	ns	Is=9A, VGS=0V, dI/dt=100A/μs
*Qrr	-	12	-	nC	

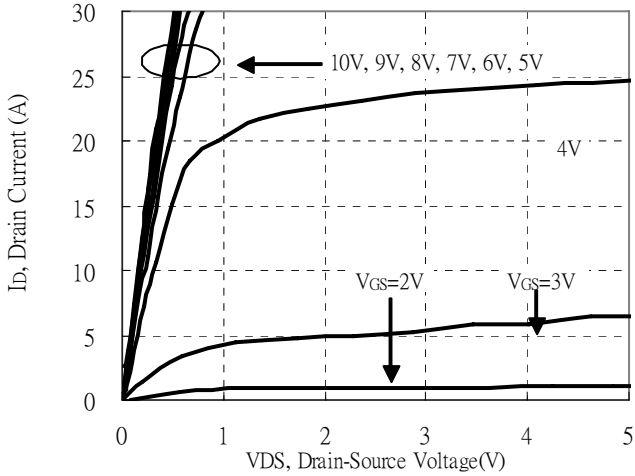
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Ordering Information

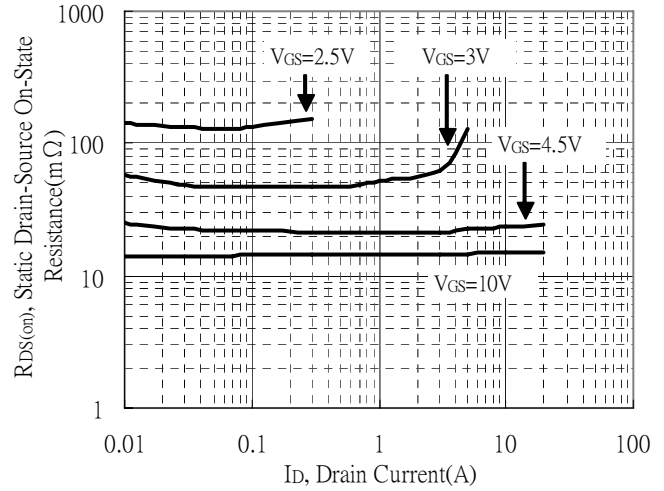
Device	Package	Shipping	Marking
MTNN8451KQ8	SOP-8 (Pb-free lead plating & halogen-free package)	2500 pcs / Tape & Reel	8451

Typical Characteristics : FET 1

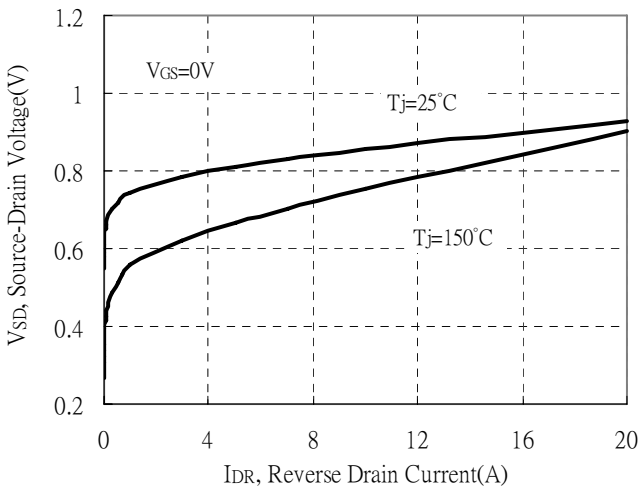
Typical Output Characteristics



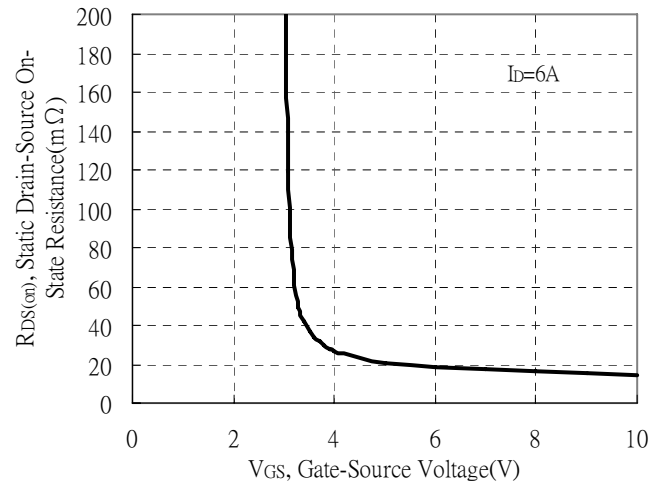
Static Drain-Source On-State resistance vs Drain Current



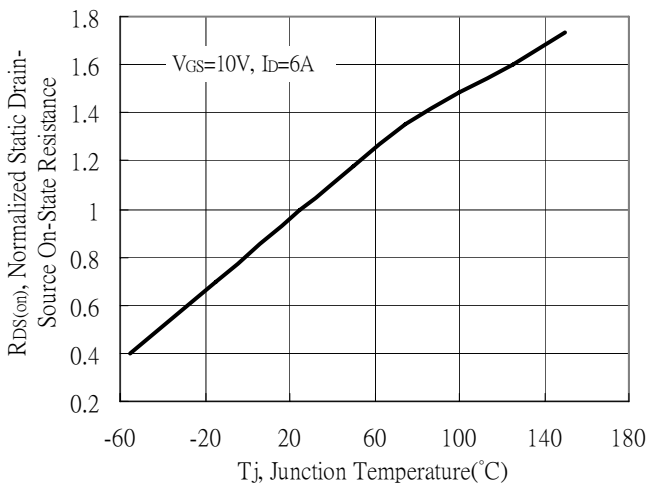
Reverse Drain Current vs Source-Drain Voltage



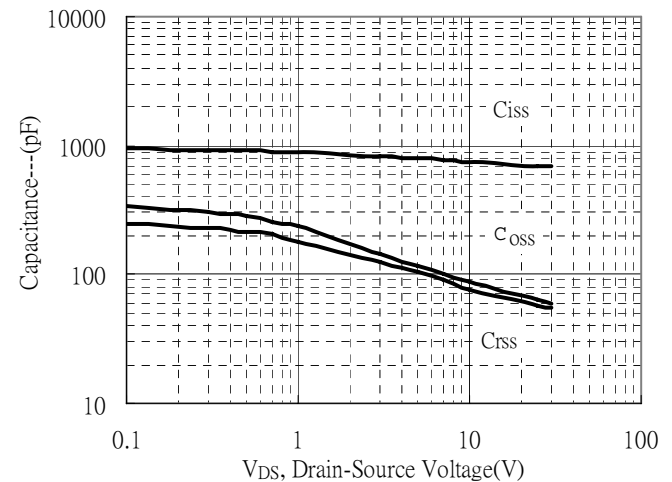
Static Drain-Source On-State Resistance vs Gate-Source Voltage



Drain-Source On-State Resistance vs Junction Temperature

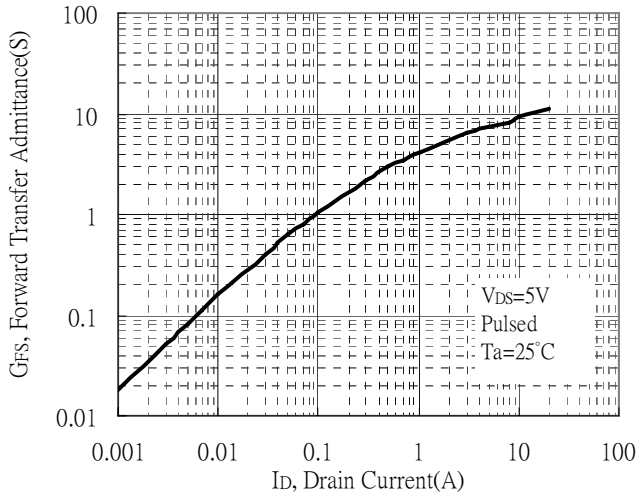


Capacitance vs Drain-to-Source Voltage

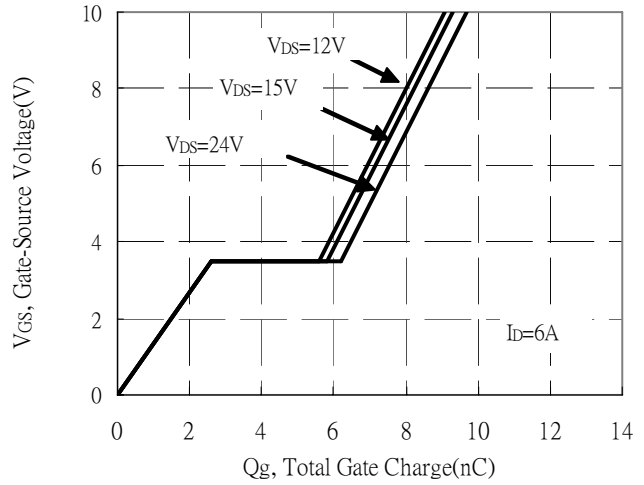


Typical Characteristics(Cont.) : FET 1

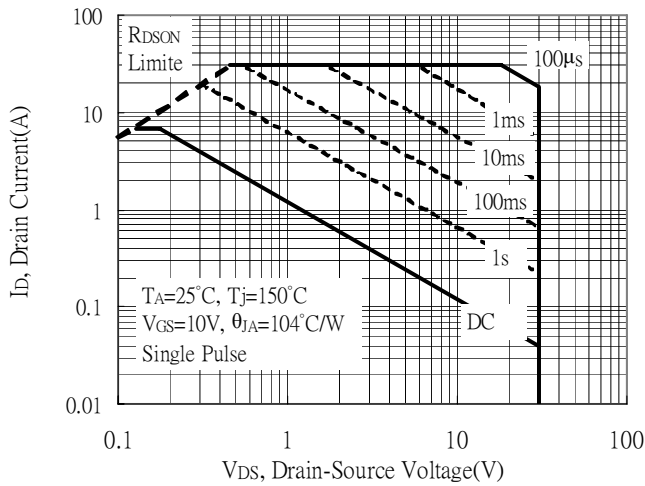
Forward Transfer Admittance vs Drain Current



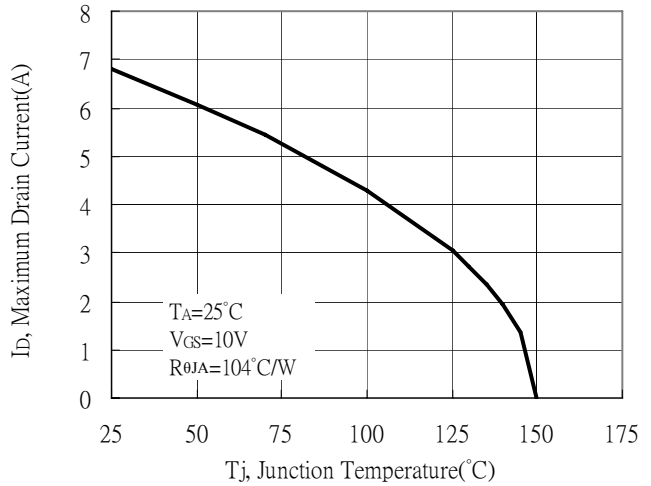
Gate Charge Characteristics



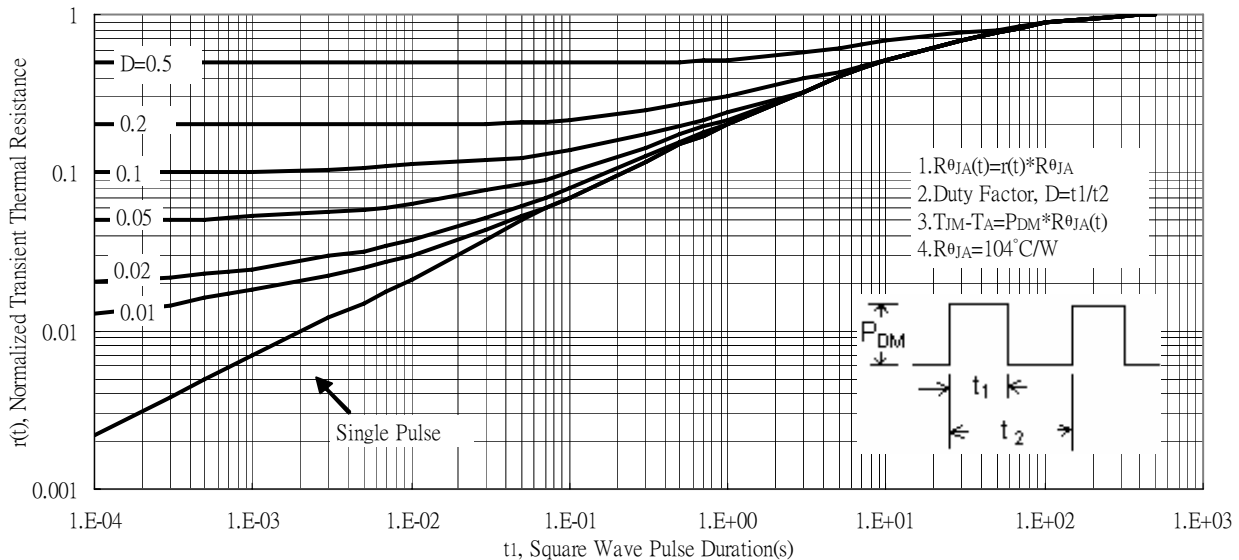
Maximum Safe Operating Area



Maximum Drain Current vs Case Temperature

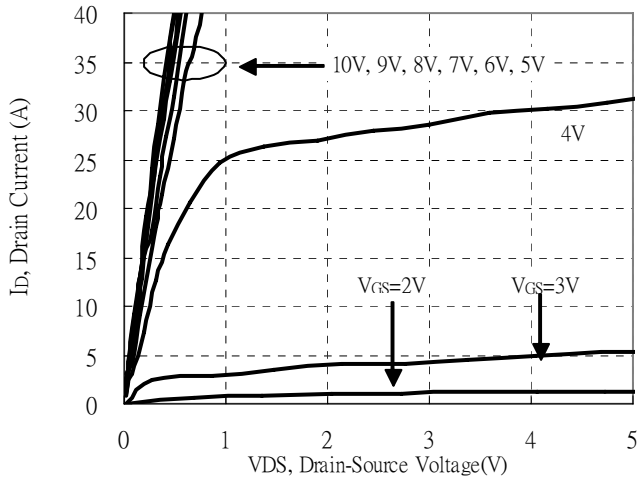


Transient Thermal Response Curves

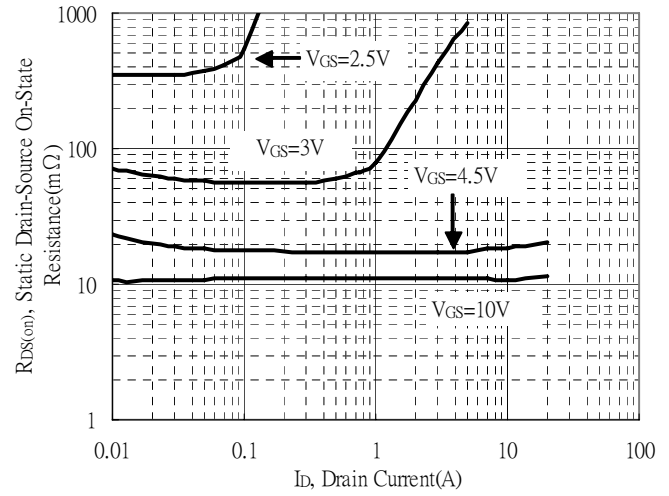


Typical Characteristics : FET 2

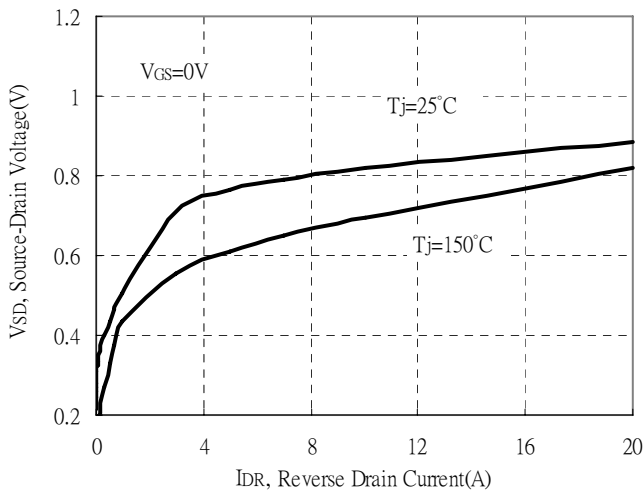
Typical Output Characteristics



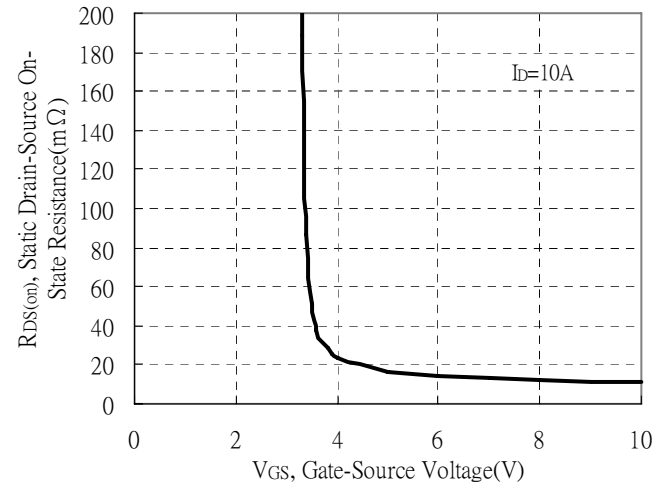
Static Drain-Source On-State resistance vs Drain Current



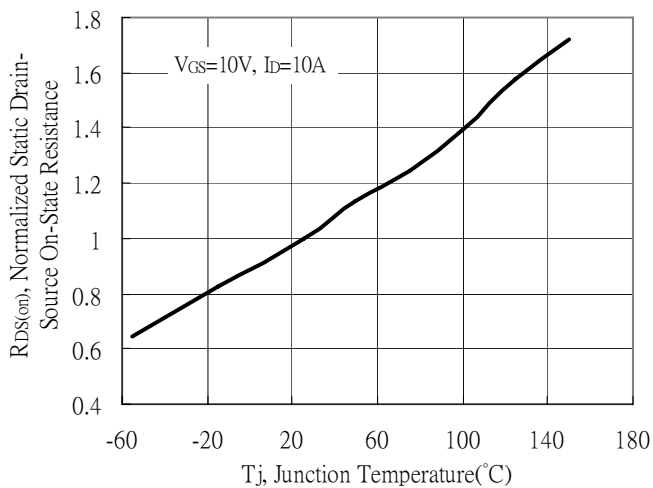
Reverse Drain Current vs Source-Drain Voltage



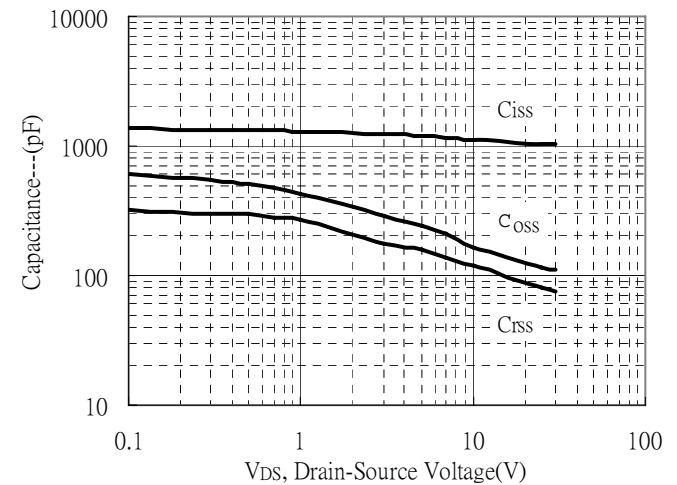
Static Drain-Source On-State Resistance vs Gate-Source Voltage



Drain-Source On-State Resistance vs Junction Temperature

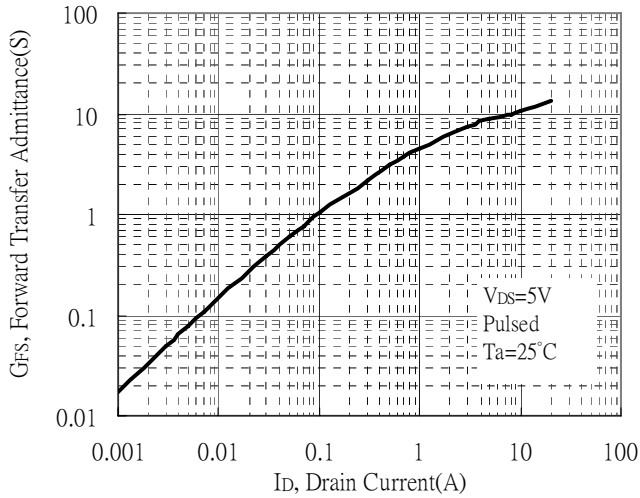


Capacitance vs Drain-to-Source Voltage

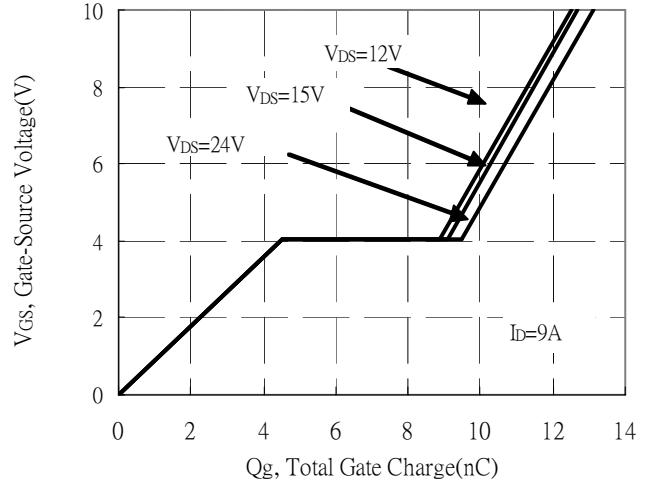


Typical Characteristics(Cont.) : FET 2

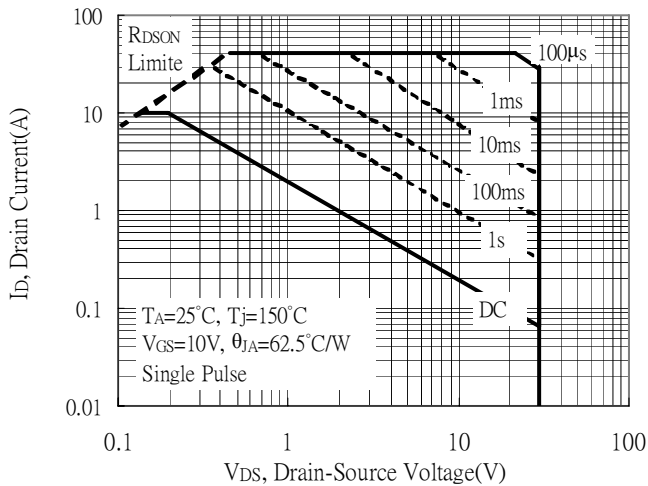
Forward Transfer Admittance vs Drain Current



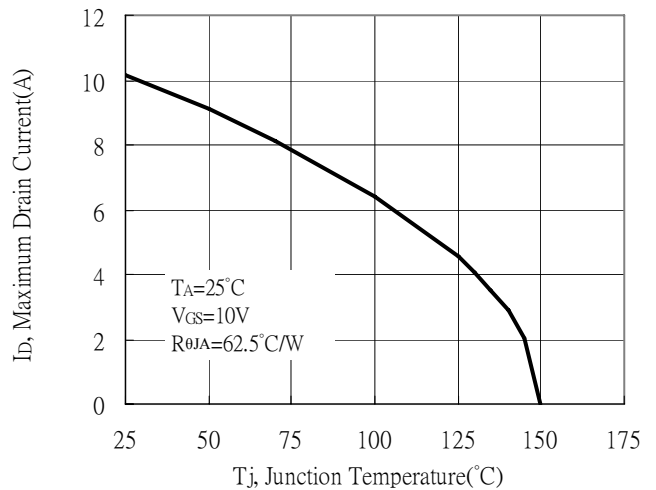
Gate Charge Characteristics



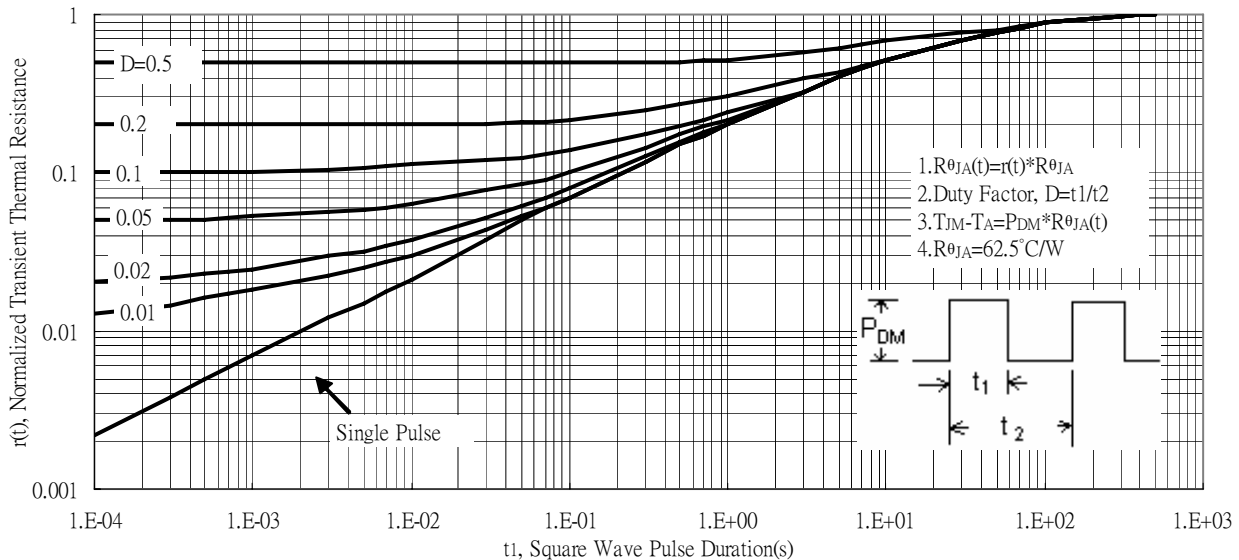
Maximum Safe Operating Area



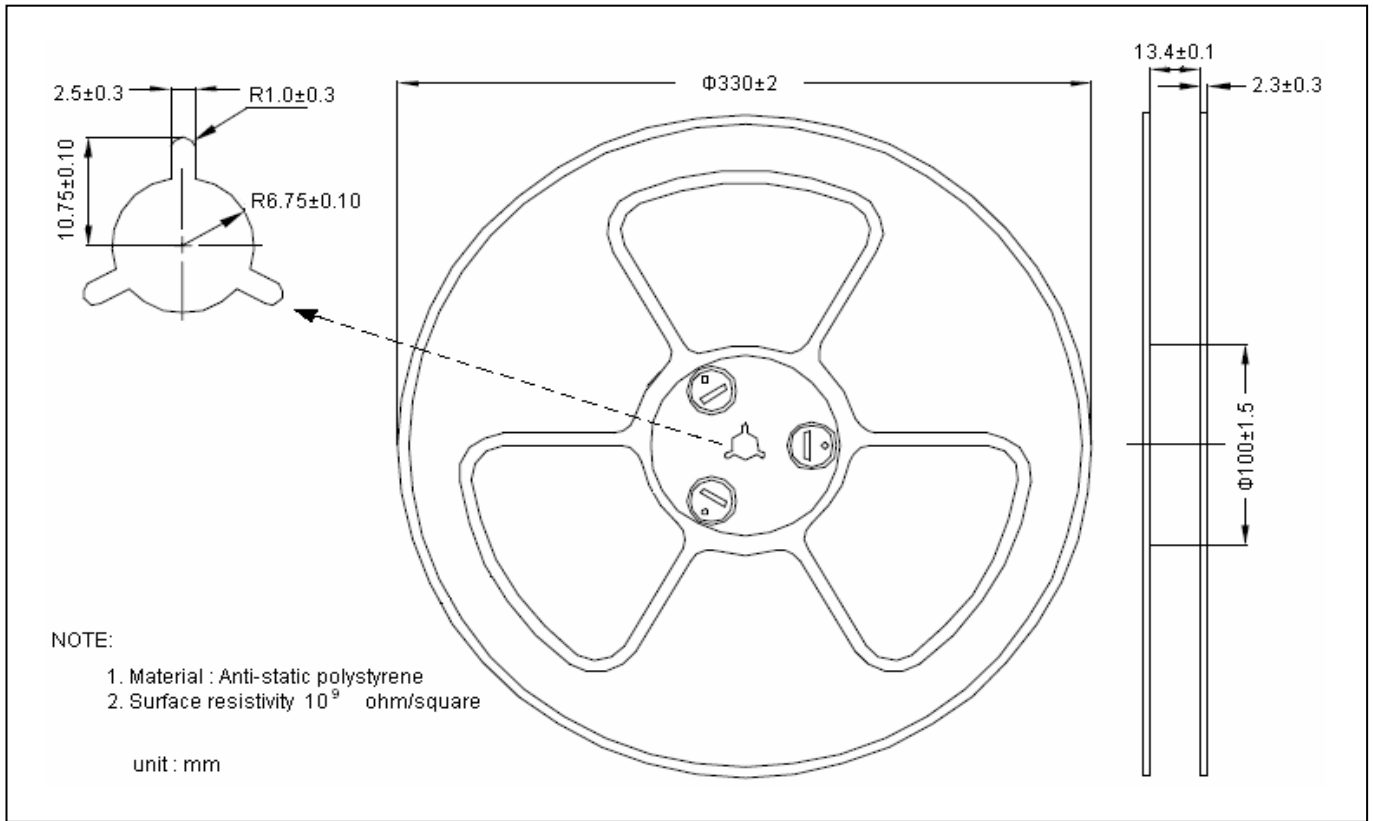
Maximum Drain Current vs Case Temperature



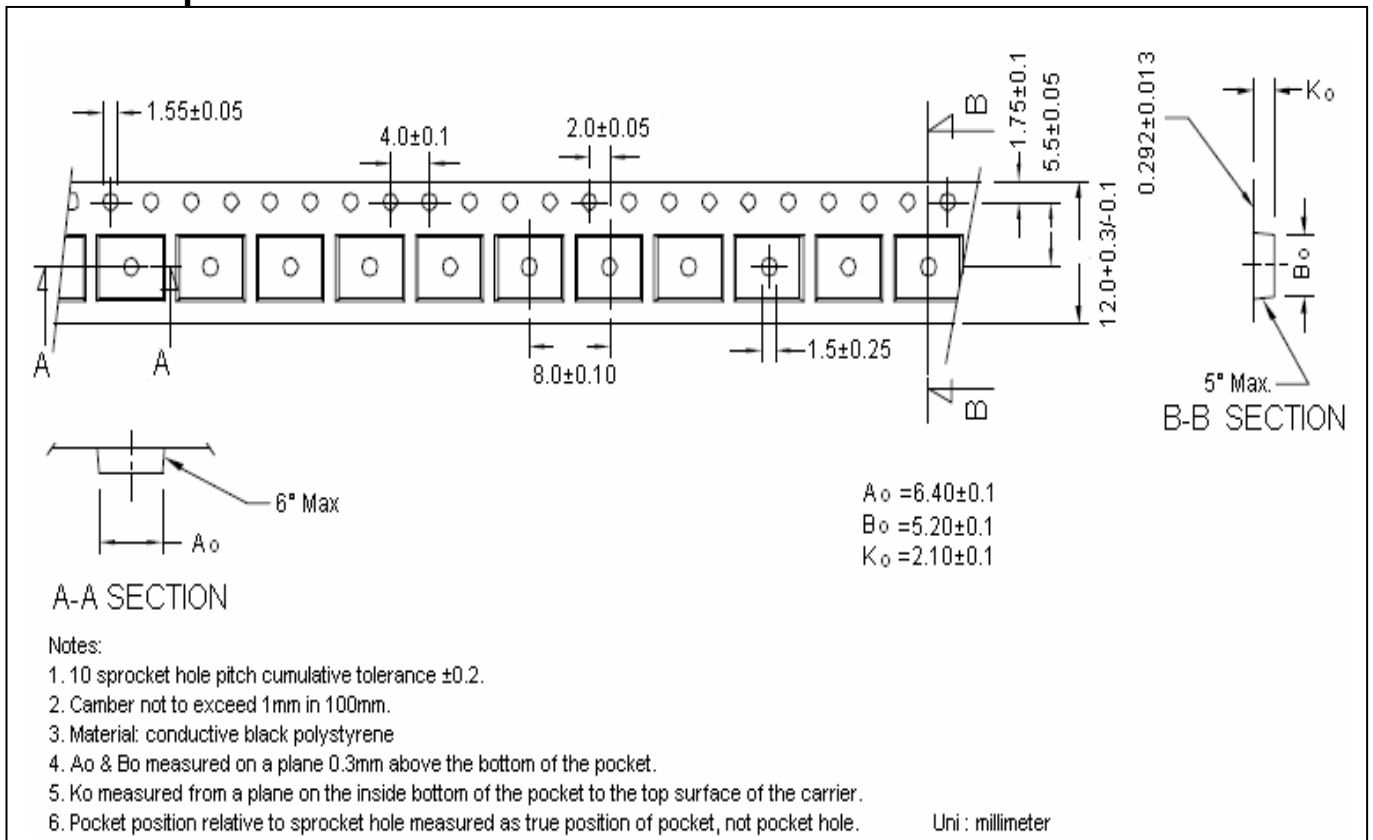
Transient Thermal Response Curves



Reel Dimension



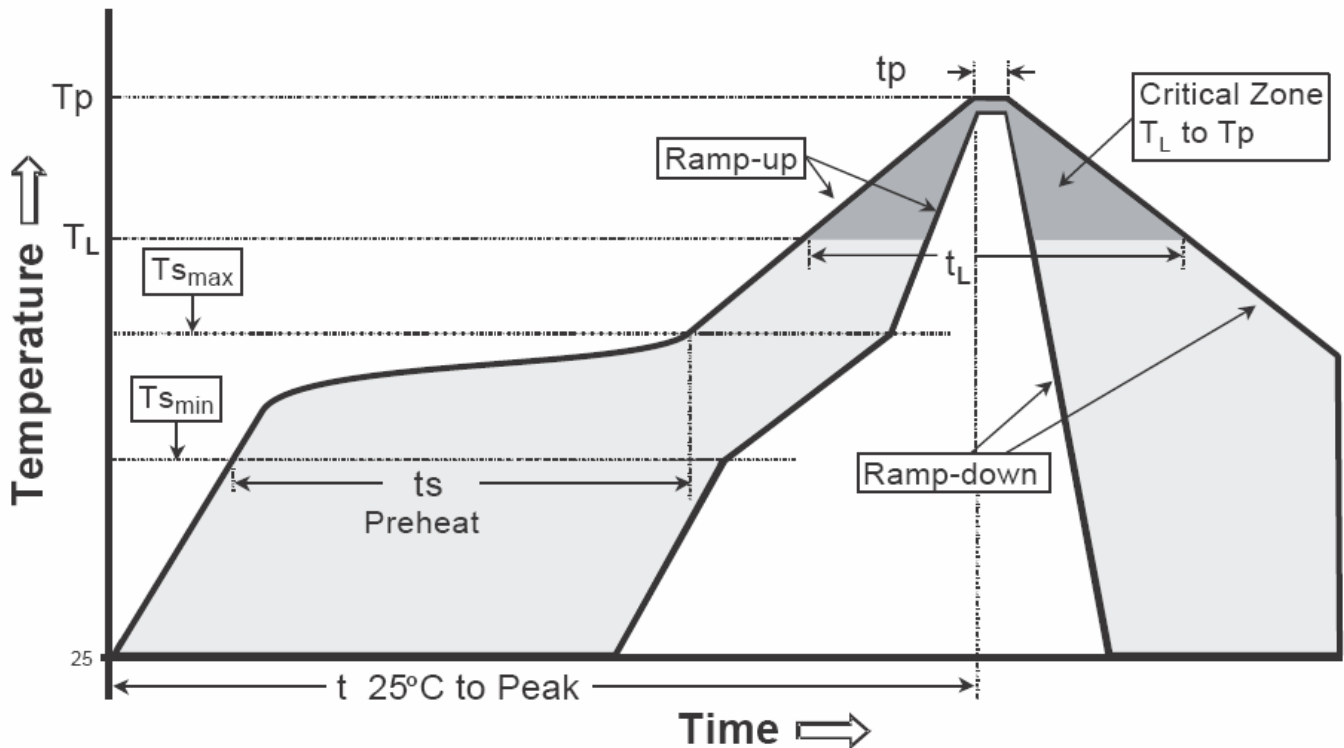
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

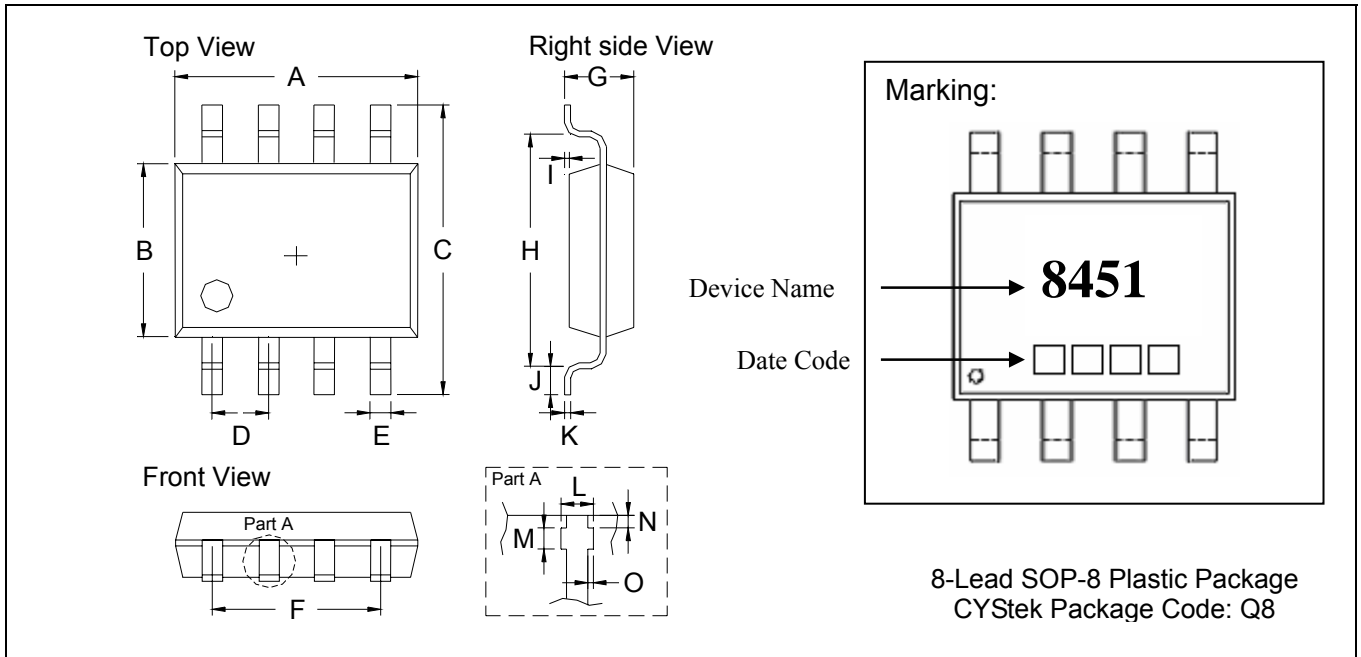
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOP-8 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1909	0.2007	4.85	5.10	I	0.0019	0.0078	0.05	0.20
B	0.1515	0.1555	3.85	3.95	J	0.0118	0.0275	0.30	0.70
C	0.2283	0.2441	5.80	6.20	K	0.0074	0.0098	0.19	0.25
D	0.0480	0.0519	1.22	1.32	L	0.0145	0.0204	0.37	0.52
E	0.0145	0.0185	0.37	0.47	M	0.0118	0.0197	0.30	0.50
F	0.1472	0.1527	3.74	3.88	N	0.0031	0.0051	0.08	0.13
G	0.0570	0.0649	1.45	1.65	O	0.0000	0.0059	0.00	0.15
H	0.1889	0.2007	4.80	5.10					

Notes: 1. Controlling dimension: millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.