FAIRCHILD
SEMICONDUCTOR®

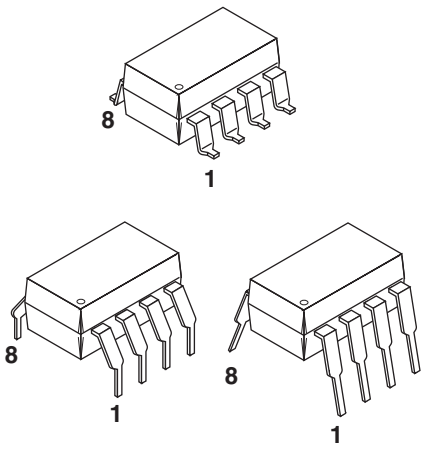
LOW INPUT CURRENT LOGIC GATE OPTOCOUPLERS

FOD2200

DESCRIPTION

The FOD2200 is an optically coupled logic gate that combine an AlGaAs LED and an integrated high gain photo detector. The detector has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pullup resistor and allows for direct drive of data busses. The hysteresis provides differential mode noise immunity and eliminates the potential for output signal chatter.

The Electrical and Switching Characteristics of the FOD2200 are guaranteed over the temperature range of 0°C to 85°C and a V_{CC} range of 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed optocouplers. Logic signals are transmitted with a maximum propagation delay of 300 nsec. The FOD2200 is useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

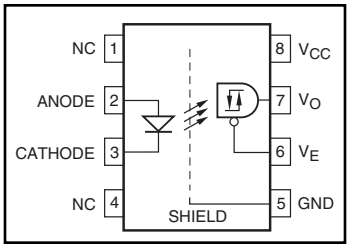


FEATURES

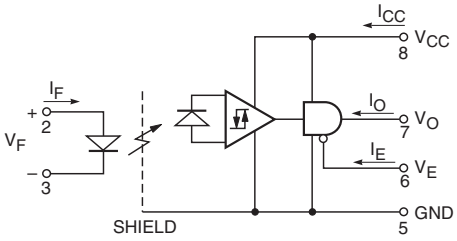
- 1 kV/μs Minimum Common Mode Rejection
- Compatible with LSTTL, TTL, and CMOS Logic
- Wide V_{CC} Range (4.5 to 20 V)
- 2.5 Mbd Guaranteed over Temperature
- Low Input Current (1.6 mA)
- Three State Output (No Pullup Resistor Required)
- Guaranteed Performance from 0°C to 85°C
- Hysteresis
- Safety Approvals Pending – UL, CSA, VDE
- V_{ISO} = 5kVRMS

APPLICATION

- Isolation of High Speed Logic Systems
- Computer-Peripheral Interfaces
- Microprocessor System Interfaces
- Ground Loop Elimination
- Pulse Transformer Replacement
- Isolated Buss Driver
- High Speed Line Receiver



Schematic



TRUTH TABLE (Positive Logic)

LED	Enable	Output
On	H	Z
Off	H	Z
On	L	H
Off	L	L

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)			
Parameter	**Symbol**	**Value**	**Units**
Storage Temperature	T_{STG}	-40 to +125	°C
Operating Temperature	T_{OPR}	-40 to +85	°C
Lead Solder Temperature (1.6mm below seating plane)	T_{SOL}	260 for 10 sec	°C
EMITTER			
Peak Transient Input Current (≤1µs PW, 300 pps)	$I_{F\ (PK)}$	1.0	A
Average Forward Input Current	I_F	10	mA
Reverse Input Voltage	V_R	5.0	V
Output Power Dissipation (No derating required up to 85°C)	P_D	45	mW
DETECTOR			
Supply Voltage	V_{CC}	0 to 20	V
Average Output Current	I_O	25	mA
Three State Enable Voltage	V_E	-0.5 to 20	V
Output Voltage	V_O	-0.5 to 20	V
Output Power Dissipation (No derating required up to 85°C)	P_D	150	mW

RECOMMENDED OPERATING CONDITIONS				
Parameter	**Symbol**	**Min**	**Max**	**Units**
Forward Input Current	$I_{F(ON)}$	1.6*	5	mA
Forward Input Current	$I_{F(OFF)}$		0.1	mA
Supply Voltage, Output	V_{CC}	4.5	20	V
Enable Voltage, Low Level	V_{EL}	0	0.8	V
Enable Voltage, High Level	V_{EH}	2.0	20	V
Operating Temperature	T_A	0	+85	°C
Fan Out (TTL load)	N		4	

*The initial switching threshold is 1.6mA or less. It is recommended that 2.2 mA be used to permit at least a 20% CTR degradation guardband.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +85°C, V_{CC} = 4.5V to 20V, $I_{F(ON)}$ = 1.6mA to 5mA, V_{EH} = 2V to 20V, V_{EL} = 0V to 0.8V, $I_{F(OFF)}$ = 0 mA to 0.1 mA Unless otherwise specified.) See Note 1.

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Min	Typ**	Max	Unit
EMITTER	(I_F = 5 mA)	V_F			1.75	V
Input Forward Voltage	T_A =25°C			1.40	1.7	
Input Reverse Breakdown Voltage	(I_R = 10 µA)	B_{VR}	5.0			V
Input Capacitance	(Pins 2 & 3) (V_F = 0, f = 1 MHz)	C_{IN}		60		pF
Input Diode Temperature Coefficient	(I_F = 5 mA)	ΔVF/ΔTA		-1.4		mV/°C
DETECTOR						
High Level Supply Current	(I_F = 5 mA) (I_O = Open, V_E = Don't care) V_{CC} = 5.5V	I_{CCH}		3.5	4.5	mA
	V_{CC} = 20V			4.0	6.0	
Low Level Supply Current	(I_F = 0) (I_O = Open, V_E = Don't care) V_{CC} = 5.5V	I_{CCL}		4.4	6.0	mA
	V_{CC} = 20V			5.2	7.5	
Low Level Enable Current	V_E = 0.4 V	I_{EL}		-0.1	-0.32	mA
High Level Enable Current	V_E = 2.7 V	I_{EH}			20	µA
	V_E = 5.5 V				100	
	V_E = 20 V			0.005	250	
High Level Enable Voltage		V_{EH}	2.0			V
Low Level Enable Voltage		V_{EL}			0.8	V

SWITCHING CHARACTERISTICS (T_A = 0°C to +85°C, $I_{F(ON)}$ = 1.6mA to 5mA, $I_{F(OFF)}$ = 0 to 0.1 mA, V_{CC} = 4.5 to 20V Unless otherwise specified.)

AC Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Propagation Delay Time to Output High Level	(Note 2, 4) (Fig. 1) With Peaking Capacitor	T_{PLH}		120	300	ns
Propagation Delay Time to Output Low Level	(Note 3, 4) (Fig. 1) With Peaking Capacitor	T_{PHL}		180	300	ns
Output Rise Time (10-90%)	(Note 5) (Fig. 1)	t_r		80		ns
Output Fall Time (90-10%)	(Note 6) (Fig. 1)	t_f		25		ns
Enable Propagation Delay Time to Output High Level	(Fig. 2)	t_{PZH}		40		ns
Enable Propagation Delay Time to Output Low Level	(Fig. 2)	t_{PZL}		50		ns
Disable Propagation Delay Time from Output High Level	(Fig. 2)	T_{PHZ}		95		ns
Disable Propagation Delay Time from Output Low Level	(Fig. 2)	T_{PLZ}		80		ns
Common Mode Transient Immunity (at Output High Level)	(T_A =25°C) (I_F = 1.6 mA, V_{OH} (Min.) = 2.0 V) V_{CC} = 5V (Note 7)(Fig. 3) $\|V_{CM}\|$ = 50 V	$\|CM_H\|$	1000			V/µs
Common Mode Transient Immunity (at Output Low Level)	(T_A =25°C) (I_F = 0 mA, V_{OL} (Max.) = 0.8 V) V_{CC} = 5V (Note 8)(Fig. 3) $\|V_{CM}\|$ = 50 V	$\|CM_L\|$	1000			V/µs

** Typical values at T_A = 25°C, V_{CC} = 5V, $I_{F(ON)}$ = 3 mA unless otherwise specified.

TRANSFER CHARACTERISTICS (T_A = 0°C to +85°C, V_{CC} = 4.5V to 20V, $I_{F(ON)}$ = 1.6mA to 5mA, V_{EH} = 2V to 20V, V_{EL} = 0V to 0.8V, $I_{F(OFF)}$ = 0mA to 0.1mA Unless otherwise specified.) See Note 1.

DC Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Output Leakage Current (V_{OUT} > V_{CC})	(V_{CC} = 4.5 V) (I_F = 5 mA) V_O = 5.5V	I_{OHH}		2.0	100	µA
	V_O = 20V			2.5	500	
Low Level Output Voltage	(V_{CC} = 4.5 V, I_F = 0 mA) (V_E = 0.4 V, I_{OL} = 6.4 mA) (Note 2)	V_{OL}		0.33	0.5	V
Input Threshold Current	(V_{CC} = 4.5 V, V_O = 0.5 V, V_E = 0.4 V, I_{OL} = 6.4 mA)	I_{FT}			1.6	mA
Logic High Output Voltage	I_{OH} = -2.6 mA	V_{OH}	2.4	V_{CC}-1.8		V
High Impedance State Output Current	V_O = 0.4 V, V_{EN} = 2 V, I_F = 5 mA	I_{OZL}			-20	µA
	V_O = 2.4 V, V_{EN} = 2 V, I_F = 5 mA	I_{OZH}			20	µA
	V_O = 5.5 V, V_{EN} = 2 V, I_F = 5 mA				100	µA
	V_O = 20 V, V_{EN} = 2 V, I_F = 5 mA				500	µA
Logic Low Short Circuit Output Current Note 10	V_O = V_{CC} = 5.5 V, I_F = 0 mA	I_{OSL}	25			mA
	V_O = V_{CC} = 20 V, I_F = 0 mA		40			mA
Logic High Short Circuit Output Current Note 10	V_{CC} = 5.5 V, I_F = 5 mA, V_O = GND	I_{OSH}	-10			mA
	V_{CC} = 20 V, I_F = 5 mA, V_O = GND		-25			mA
Input Current Hysteresis	V_{CC} = 4.5 V	I_{HYS}		0.03		mA

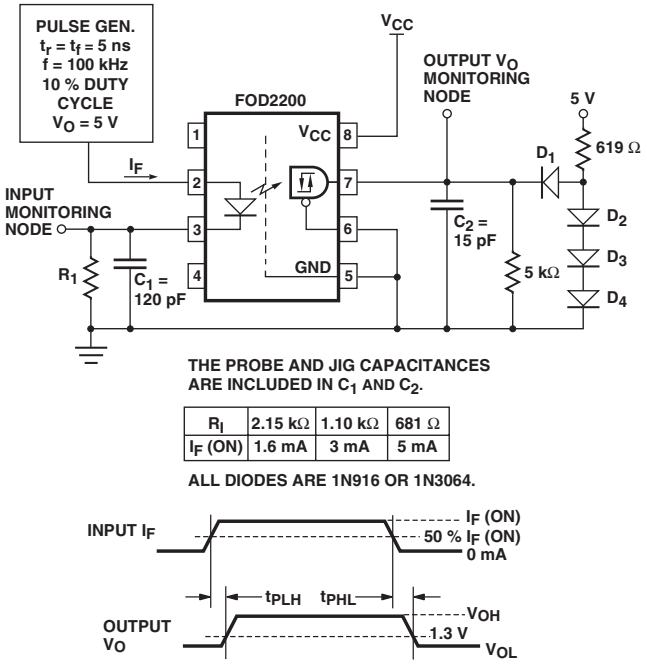
ISOLATION CHARACTERISTICS (T_A = -40°C to +85°C Unless otherwise specified.)

Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Withstand Insulation Test Voltage	(R_H < 50%, T_A = 25°C) t = 1 min (Note 9)	V_{ISO}	5000			V_{RMS}
Resistance (Input to Output)	(V_{I-O} = 500 VDC) (Note 9)	R_{I-O}		10^{12}		Ω
Capacitance (Input to Output)	(V_{I-O} = 0V, f = 1 MHz) (Note 9)	C_{I-O}		0.6		pF

** Typical values at T_A = 25°C, V_{CC} = 5V, $I_{F(ON)}$ = 3 mA unless otherwise stated.

NOTES

1. The V_{CC} supply to each optoisolator must be bypassed by a 0.1µF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.
2. t_{PLH} - Propagation delay is measured from the 50% level on the LOW to HIGH transition of the input current pulse to the 1.3V level on the LOW to HIGH transition of the output voltage pulse.
3. t_{PHL} - Propagation delay is measured from the 50% level on the HIGH to LOW transition of the input current pulse to the 1.3V level on the HIGH to LOW transition of the output voltage pulse.
4. When the peaking capacitor is omitted, propagation delay times may increase by 100 ns.
5. t_r - Rise time is measured from the 10% to the 90% levels on the LOW to HIGH transition of the output pulse.
6. t_f - Fall time is measured from the 90% to the 10% levels on the HIGH to LOW transition of the output pulse.
7. CM_H - The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the high state (i.e., $V_{OUT} > 2.0$ V).
8. CM_L - The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the low state (i.e., $V_{OUT} < 0.8$ V).
9. Device considered a two-terminal device: Pins 1,2,3 and 4 shorted together, and Pins 5,6,7 and 8 shorted together.
10. Duration of output short circuit time should not exceed 10 ms.



R_l	2.15 kΩ	1.10 kΩ	681 Ω
I_F (ON)	1.6 mA	3 mA	5 mA

Fig. 1. Test Circuit and Waveforms for t_{PLH}, t_{PHL}, t_r and t_f.

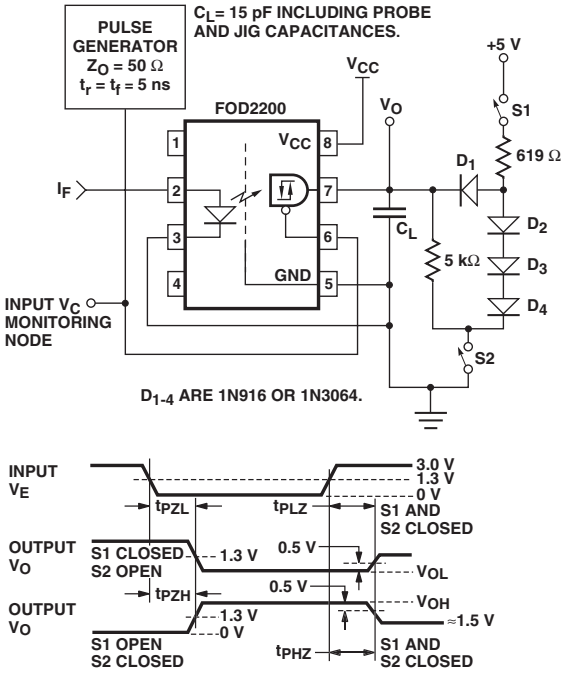


Fig. 2. Test Circuit and Waveforms for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}

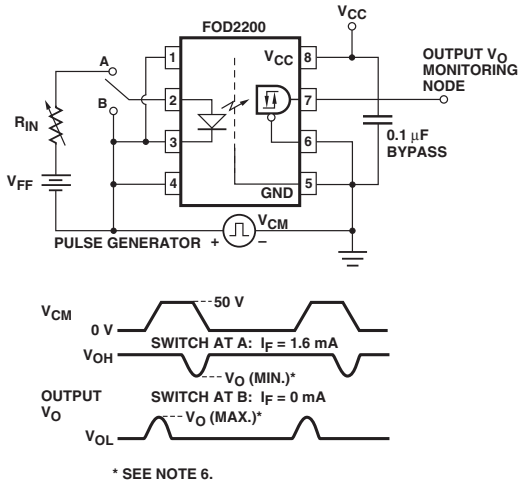


Fig. 3. Test Circuit and Typical Waveforms for Common Mode Transient Immunity

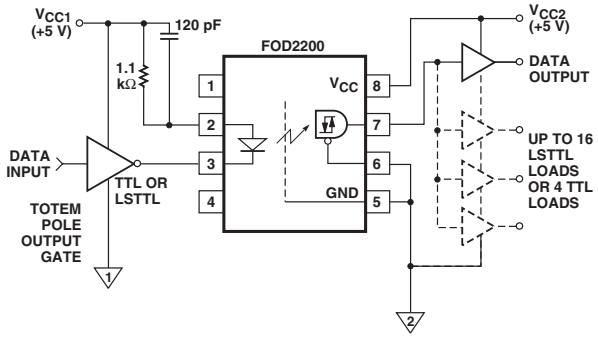


Figure 4. Recommended LSTTL to LSTTL Circuit.

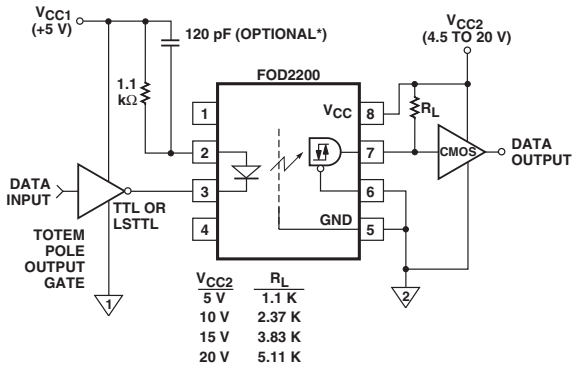


Figure 5. LSTTL to CMOS Interface Circuit.

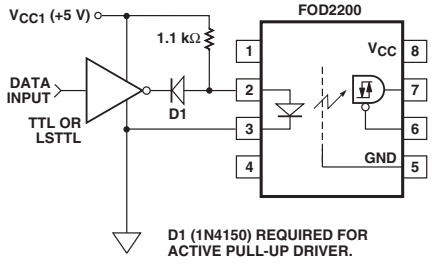


Figure 6. Recommended LED Drive Circuit.

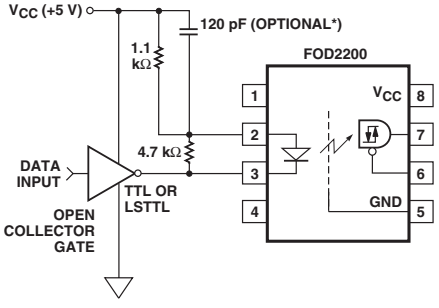


Figure 7. Series LED Drive with Open Collector Gate (4.7 kΩ Resistor Shunts I_{OH} from the LED).

***The 120pF capacitor may be omitted in applications where 500ns propagation delay is sufficient.**

TYPICAL PERFORMANCE CURVES

Figure 8. Input Forward Current vs Forward Voltage

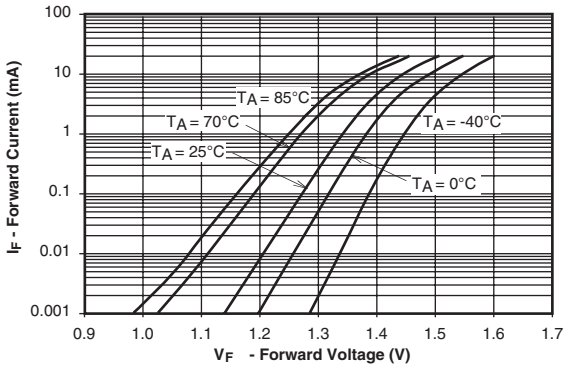


Figure 9. Output Voltage vs. Input Forward Current

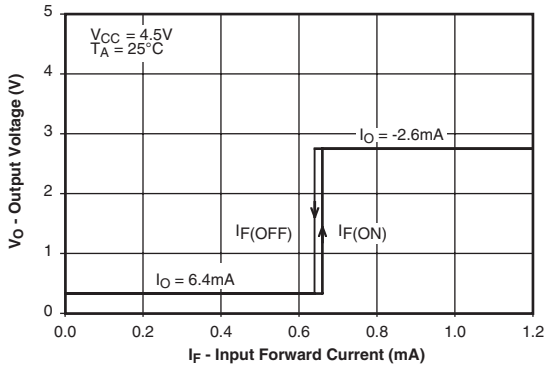


Figure 10. Input Threshold Current vs. Ambient Temperature

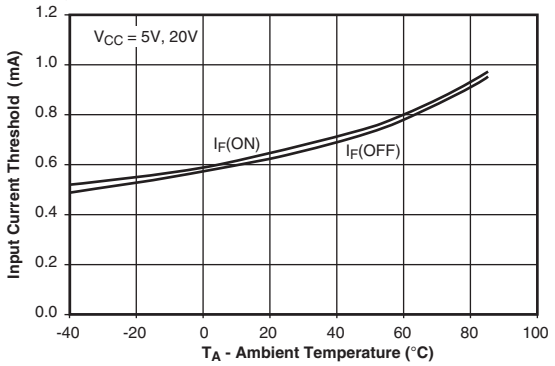


Figure 11. Logic Low Output Voltage vs. Ambient Temperature

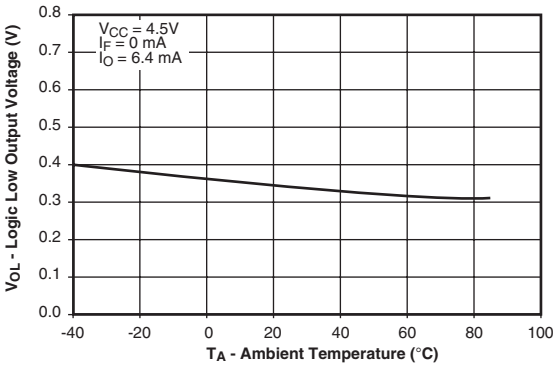


Figure 12. Logic High Output Voltage vs. Supply Voltage

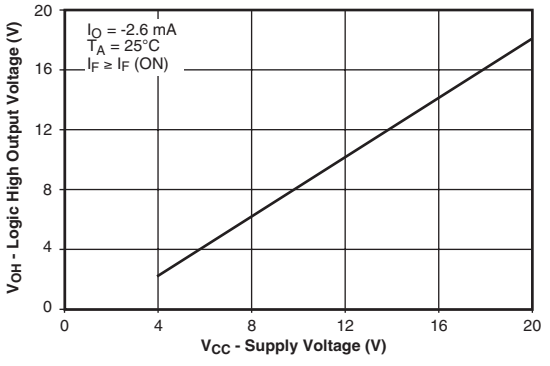
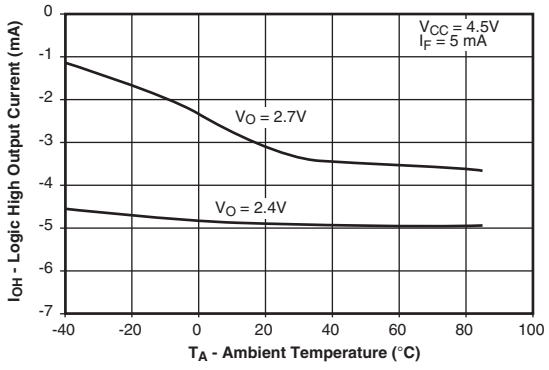


Figure 13. Logic High Output Current vs. Ambient Temperature



TYPICAL PERFORMANCE CURVES

Figure 14. Propagation Delay vs Ambient Temperature

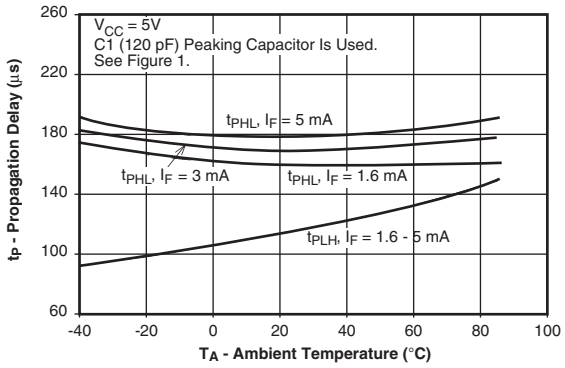
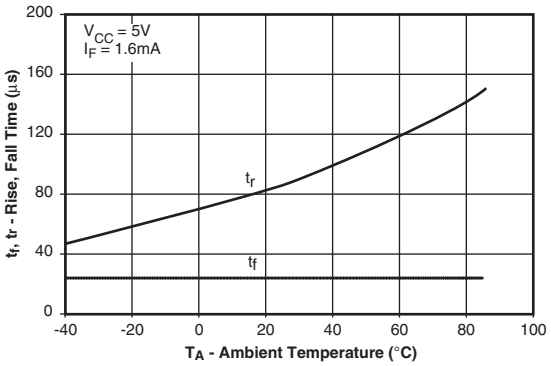
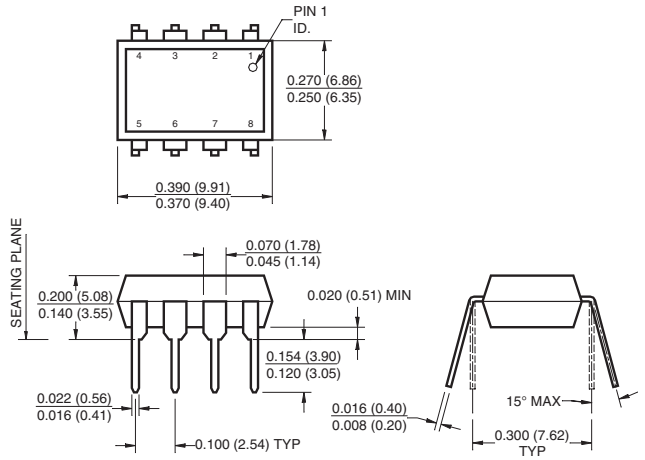


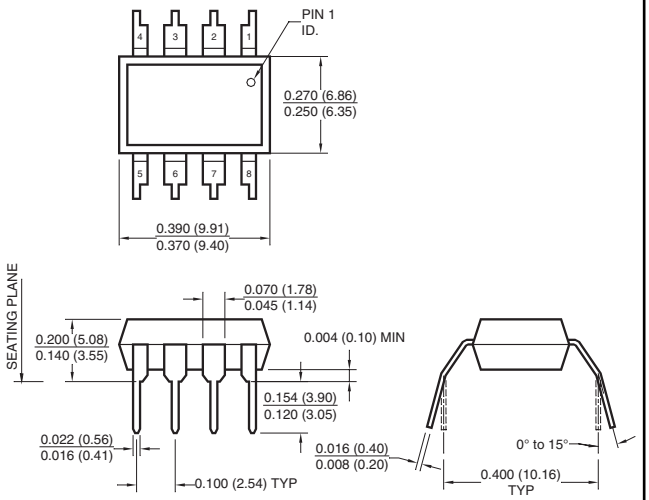
Figure 15. Rise, Fall Time vs Ambient Temperature



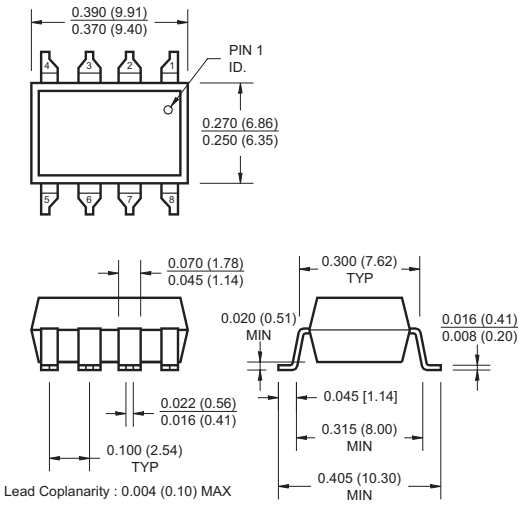
Package Dimensions (Through Hole)



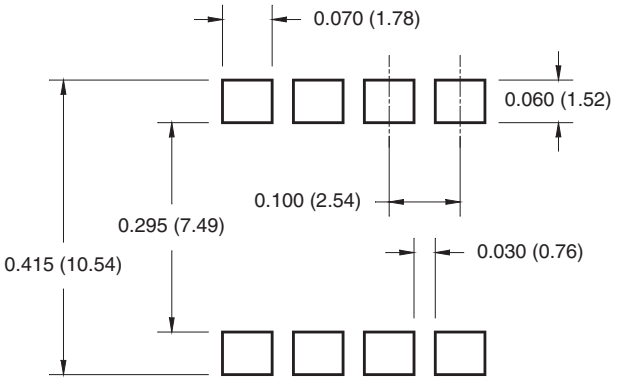
Package Dimensions (0.4"Lead Spacing)



Package Dimensions (Surface Mount)

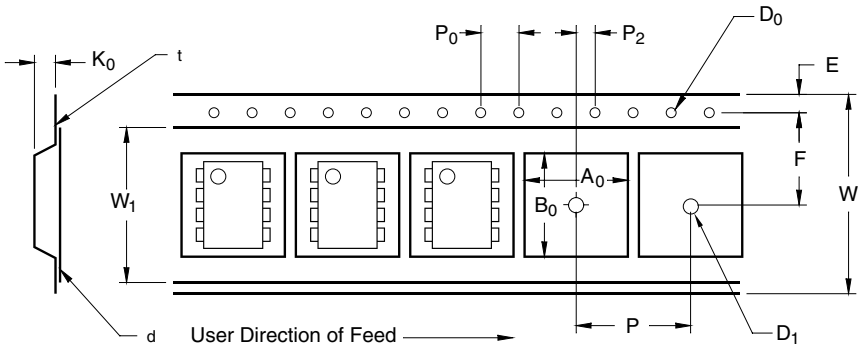


8 - Pin Dip



NOTE
All dimensions are in inches (millimeters)

Carrier Tape Specifications



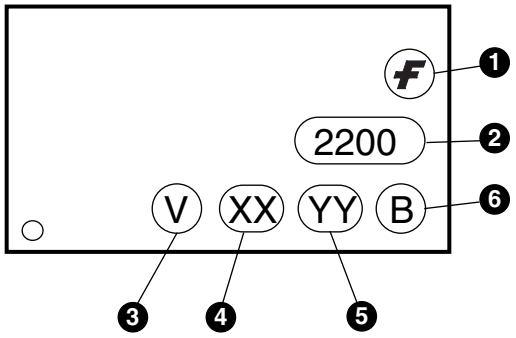
Description	Symbol	Dimension in mm
Tape Width	W	16.0 ± 0.3
Tape Thickness	t	0.30 ± 0.05
Sprocket Hole Pitch	P_0	4.0 ± 0.1
Sprocket Hole Diameter	D_0	1.55 ± 0.05
Sprocket Hole Location	E	1.75 ± 0.10
Pocket Location	F	7.5 ± 0.1
	P_2	4.0 ± 0.1
Pocket Pitch	P	12.0 ± 0.1
Pocket Dimensions	A_0	10.30 ±0.20
	B_0	10.30 ±0.20
	K_0	4.90 ±0.20
Cover Tape Width	W_1	1.6 ± 0.1
Cover Tape Thickness	d	0.1 max
Max. Component Rotation or Tilt		10°
Min. Bending Radius	R	30

ORDERING INFORMATION

Example: FOD2200 X

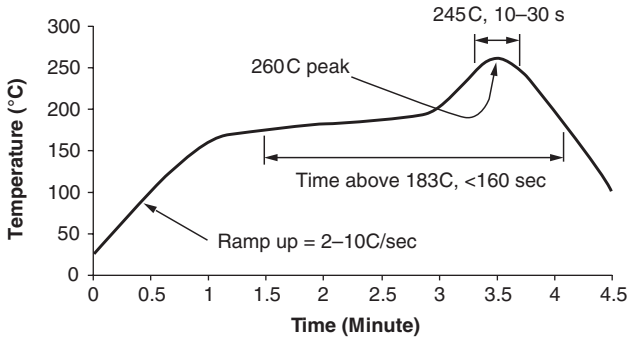
X	
Packaging Option	
S:	Surface Mount Lead Bend
SD:	Surface Mount, Tape and Reel
T:	0.4" Lead Spacing
V:	VDE 0884
TV:	VDE 0884, 0.4" Lead Spacing
SV:	VDE 0884, Surface Mount
SDV:	VDE 0884, Surface Mount, Tape and Reel

MARKING INFORMATION



Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	Two digit year code, e.g., ‘03’
5	Two digit work week ranging from ‘01’ to ‘53’
6	Assembly package code

Reflow Profile



- Peak reflow temperature: 260C (package surface temperature)
- Time of temperature higher than 183C for 160 seconds or less
- One time soldering reflow is recommended

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.